

Silicon Dioxide Contact Window Disfiguration Due to Oxide Decomposition During the Baking Step

Miloš Popadić*, Lis K. Nanver, and Yann Civale

Abstract—At elevated temperatures Si reacts with SiO₂ to form a volatile SiO. This process affects edges of contact windows in SiO₂. In this paper a systematic analysis of the effect of a baking step on contact windows is presented. Formation of cavities at contact window edges and lateral widening of contact windows have been observed. Linear time dependence and temperature dependence according to the Arrhenius equation of lateral widening of contact windows were found. The effect of the baking step on contact windows cannot be neglected when the baking temperature equals or exceeds 900 °C.

Index Terms—To be determined.

I. INTRODUCTION

IN a variety of IC processes a Si wafer with a surface oxide layer and with contact windows to the Si through the oxide is exposed to an elevated temperature. One example is Si CVD epitaxial growth or dopant deposition inside the CVD epitaxial reactor, for which the wafer surface needs to be clean and oxide free. The last step that ensures this is a bake inside the CVD reactor that precedes the epitaxial growth or dopant deposition.

In such steps, however, the free edges of the Si/SiO₂ interface are affected. Depending on the pre-baking temperature, an undercut cavity at the edges of contact windows may be created which is only occasionally or partly filled with Si, or the contact windows can be significantly disfigured. This effect has, however, been mainly analyzed when utilized for complete Si surface cleaning at considerably higher temperatures [1][2].

In this paper we present a simple systematic analysis of the effect of elevated temperature on contact windows in SiO₂. By varying the process parameters of the baking step we establish a basis that provides an estimate of the extent to which the contact windows are affected.

Manuscript received October 1, 2007. This work was supported by NXP Semiconductors under PACD A5 project.

All authors are with the Delft University Technology, ECTM laboratory and the DIMES institute.

*corresponding author (e-mail: m.popadic@dimes.tudelft.nl, phone: +31152787061)

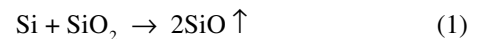
II. SAMPLE FABRICATION

In order to test the effect of the baking step on the contact openings to the Si in SiO₂, a set of samples was prepared among which the process parameters were systematically varied.

Samples were fabricated as follows: first, the wafer surface was oxidized to obtain a desired oxide thickness in the range of 20 nm to 100 nm, or a layer of LPCVD TEOS SiO₂ was deposited. Then, the contact windows were opened by wet etching in the buffered HF 1:7 solution. Afterwards, the wafers were cleaned and baked in the ASM's Epsilon one epitaxial reactor. Prior to the loading of the wafers into the epitaxial reactor, native oxide was removed in the 0.55% HF solution. This step reduced the oxide thickness by approximately 10 nm in cases of thermally grown oxides, or by approximately 70 nm in cases of LPCVD TEOS deposited oxides. The baking step in the epitaxial reactor was performed in H₂ ambient at reduced pressure of 60 Torr. The baking temperature was varied in the range of 900 °C to 1150 °C, and the baking time was also varied. The ramp-up rate of the temperature was kept constant at 10 °C/s, while the ramp-down rate was determined by the cooling speed of the reactor by the hydrogen flow after the heater is switched off.

III. OXIDE DECOMPOSITION

At elevated temperatures silicon dioxide decomposes and desorbs, and evidence that the reaction



is responsible for the decomposition was first proposed by [3], and confirmed by [2]. This process takes place at Si/SiO₂ interfaces but is especially pronounced at the edges of the interfaces where SiO as a volatile reaction product can freely escape and need not diffuse through SiO₂. This leads to lateral widening of openings in SiO₂, or in cases of complete SiO₂ coverage first holes in SiO₂ are formed, and then such holes grow laterally [2][3].

As Si is consumed in the reaction (1), Si wafer surface initially becomes uneven during the decomposition process, but ultimately, due to Si surface diffusion, becomes atomically flat and suitable for epitaxial growth [1]. Therefore, this process can be successfully used for Si surface cleaning prior to epitaxial growth, but in cases when the epitaxial growth is desired inside contact windows in the SiO₂, or such contact

windows are exposed to elevated temperatures in a different process, significant contact window disfiguration can happen.

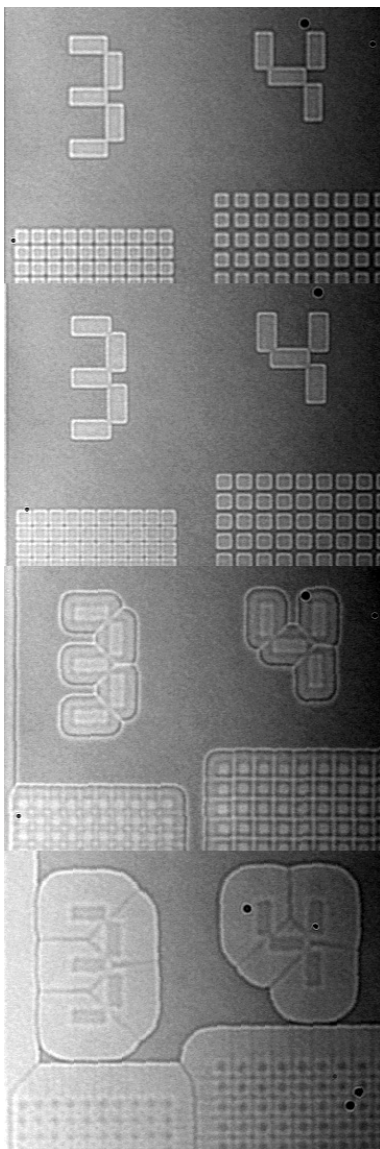


Fig. 1. Time evolution of the disfiguration of the contact openings in a 20 nm thick SiO₂, at 1150 °C. Baking times from top to bottom are 1 s, 6 s, 35 s and 120 s. Lateral widening due to SiO₂ decomposition is evident. Shape of contact windows prior to baking remains visible as the Si surface remains uneven.

IV. RESULTS

Time evolution of the disfiguration of the contact openings (COs) in a 20 nm thick SiO₂, at 1150 °C, over the first 120 s is presented in Fig. 1. Lateral widening of COs can be observed. In addition, the position of original COs is still visible, since in our experiments the combination of the baking temperatures and baking times was insufficient for the Si surface flattening to be completed. It is evident that such a baking step would be unacceptable in many an IC fabrication process. On simple rectangular structures CO sizes were measured. By subtracting the expected size according to the mask defined size and the

expected underetch during the CO opening, values for lateral widening of COs were obtained (Fig. 2). Time dependence of the lateral widening is clearly linear. This allows us to introduce the lateral widening rate, which in case of the 20 nm thick oxide and the baking temperature of 1150 °C amounts to 75 nm/s. The offset of the dependency presented in Fig. 2 which indicates that a certain non-zero widening exists even with 0 s baking time can be attributed to the widening during the temperature increase to 1150 °C and the succeeding temperature decrease.

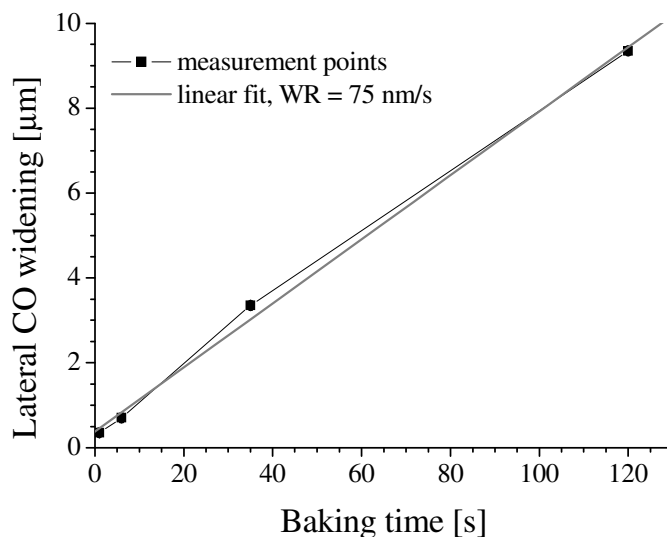


Fig. 2. Time dependence of the lateral widening of contact openings in a 20 nm thick thermal oxide at 1150 °C. The dependency is clearly linear, with a widening rate of 75 nm/s. The offset at 0 s baking time is due to widening during heating and cooling.

Lateral widening rate is strongly temperature dependent. Temperature evolution of the disfiguration of the COs in a 20 nm thick SiO₂ during 120 s over the temperature range from 950 °C to 1150 °C is presented in Fig. 3. Corresponding lateral widening and the widening rate dependence on temperature is presented in Fig. 4. The widening rate temperature dependence very accurately follows the common dependency given by the Arrhenius equation

$$WR = Ae^{\frac{E_a}{kT}}, \quad (2)$$

where $E_a = 4$ eV is the activation energy obtained from our results.

Accurate insight into the disfiguration process at lower temperatures cannot be obtained by visual microscopy. The effect of a baking step at 900 °C during 30 min can be observed on a cross-sectional TEM image of the contact window (Fig. 5). In the example of contact window corner presented in Fig. 5a it is observed that the cavity created by oxide decomposition is filled with Si, as opposed to Fig. 5b. This effect is common and is enabled by the high surface diffusivity of Si at elevated temperatures. For many device

applications, the existence of such a filled or empty cavity can be detrimental or unacceptable. In those cases, the baking temperature or the baking time need to be further reduced.

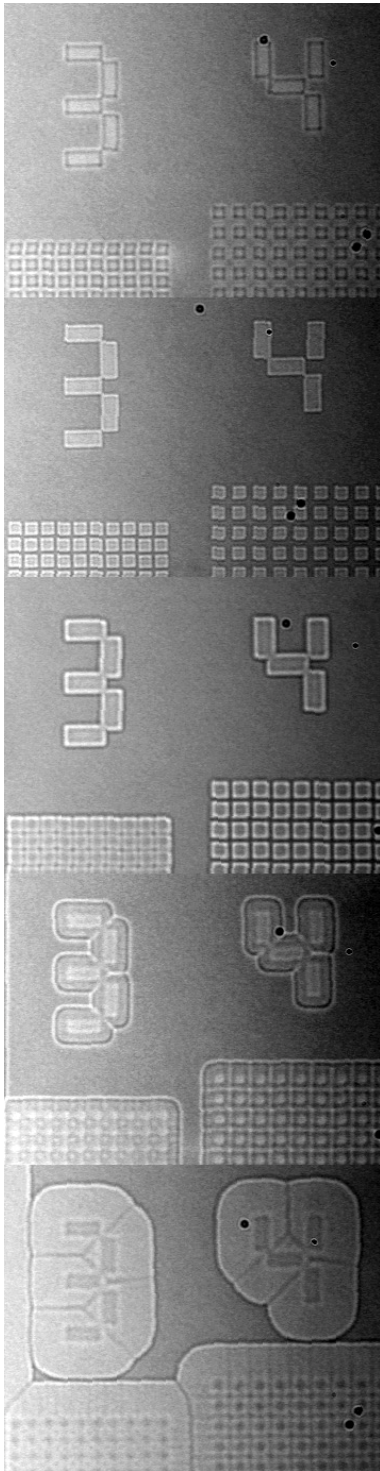


Fig. 3. Temperature evolution of the disfiguration of the contact openings in a 20 nm thick during 120 s. Baking temperatures from top to bottom are 950 °C, 1000 °C, 1050 °C, 1100 °C, and 1150 °C.

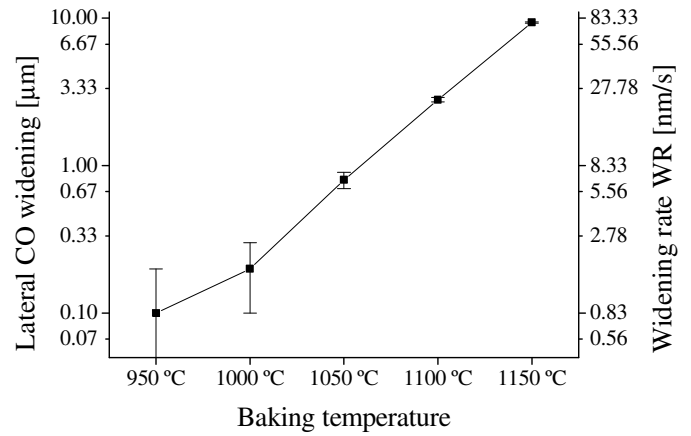


Fig. 4. Temperature dependence of the lateral widening of contact openings in 20 nm thick thermal oxide during 120 s. Based on the linearity presented in Fig. 2, lateral widening was also translated to a widening rate. Temperature dependency of the widening rate follows the common Arrhenius equation (2).

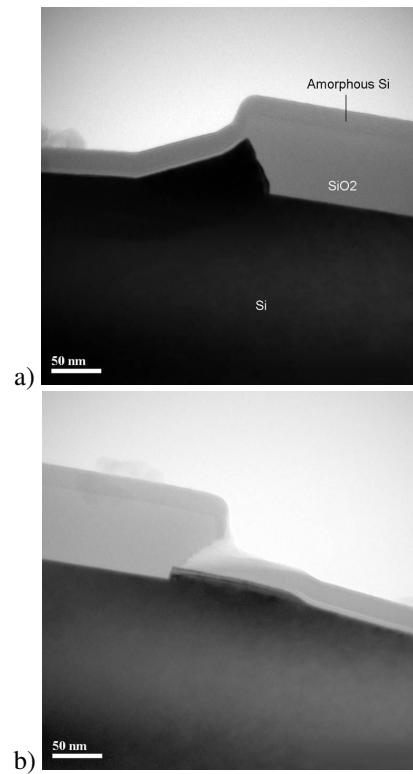


Fig. 5. Cross-sectional TEM images of the edges of contact windows in the SiO₂. A cavity in the oxide created during the baking step by Si reacting with SiO₂ to produce a volatile SiO can be observed. Baking was done for 30min at 900 °C in H₂ at 60 Torr. In fig. a) this cavity is filled with Si.

Lateral widening is also dependent on the SiO₂ thickness. A comparison of samples with different oxide thicknesses exposed to the baking step of 1150 °C for 120 s is presented in Fig. 6. By comparing the samples with 20 nm and 100 nm thick thermal oxides it is evident that the lateral widening is dependent on the oxide thickness, and the comparison of the samples with 100 nm thermal oxide and 400 nm LPCVD TEOS indicates that COs in the LPCVD TEOS widen faster

than in the thermal oxide. It is shown in [2] and [4] that properties of the Si/SiO₂ interface, such as defect density, play an important role in determining the reaction speed.

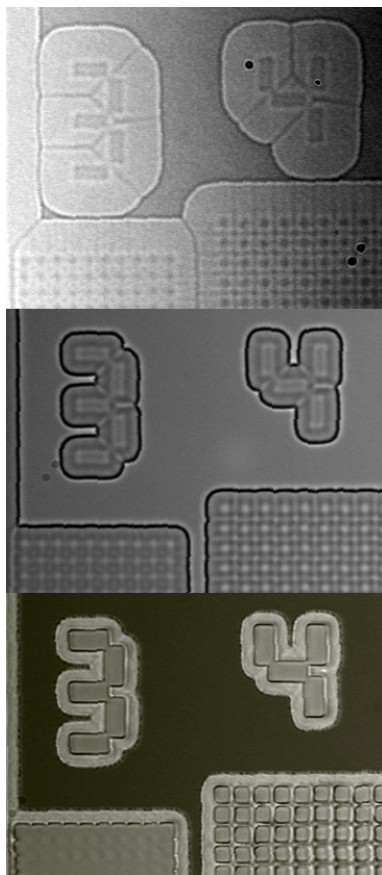


Fig. 6. Disfiguration of the contact openings for different SiO₂ thicknesses after baking at 1150 °C for 120 s. Oxides used from top to bottom are 20 nm thick thermal oxide, 100 nm thick thermal oxide and 330 nm thick LPCVD TEOS.

Furthermore, the effect of the same baking step on the sample with 10 nm of thermal oxide is presented in Fig. 7, but on a region which initially contained no contact windows. This shows that the oxide decomposition process is not necessarily restricted to lateral contact window widening. Such “expanded holes” were observed also with 20 nm thick oxides, but are considerably less frequent. It was demonstrated in [4] that voids at the Si/SiO₂ interface start growing at defect sites, and that this can be prevented by introducing a small amount of O₂ during the high-temperature step, which would re-oxidize the SiO.

At low doping levels, the lateral widening does not depend on the type of Si wafer doping (p-type or n-type). The influence of doping at higher doping levels was not investigated.

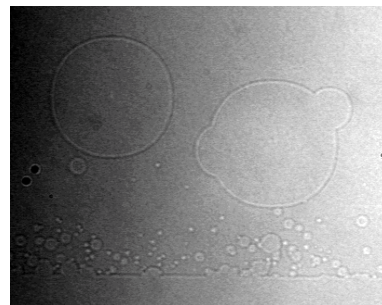


Fig. 7. The effect of baking at 1150 °C for 120 s on 10 nm thick thermal oxide, seen on a region different from Fig. 1, Fig. 3, and Fig. 6. Holes in the oxide are created.

V. CONCLUSION

A systematic analysis of the influence of elevated temperatures on contact windows in SiO₂ has been presented. Silicon dioxide reacts with Si to form volatile SiO, which leads to lateral contact window widening or to the formation of cavities at the contact window edges. The process cannot be neglected at temperatures of 900 °C or higher. The lateral widening of contact windows is linearly dependent on the baking time and follows the Arrhenius equation for the baking temperature dependence. This simple overview provides a reasonable estimate of the effect under different process conditions, and therefore an applicability prediction in the process design stage. In the specific example of the baking step used prior to CVD epitaxial growth, the baking temperature can be reduced by using a Marangoni drying system after the native oxide removal that precedes the CVD epitaxial growth.

REFERENCES

- [1] M. Mayusumi, M. Imai, S. Nakahara, K. Inoue and H. Habuka, “Morphology of Silicon Oxide Film on Silicon Wafer Surface during Its Removal Process in a Hydrogen Ambient”, *Jpn. J. Appl. Phys.* vol. 40, pp. 6556-6560 (2001)
- [2] Y. Kobayashi, Y. Shinoda, and K. Sugii, “Thermal Desorption from Si(111) Surfaces with Native Oxides Formed During Chemical Treatments”, *Jpn. J. Appl. Phys.* vol. 29 no. 6, pp. 1004-1008 (1990)
- [3] R. Tromp, G. W. Rubloff, P. Balk, and F. K. LeGoues, “High-Temperature SiO₂ Decomposition at the SiO₂/Si Interface”, *Phys. Rev. Lett.* vol. 55 no. 21, pp. 2332-2335 (1985)
- [4] G. W. Rubloff, K. Hofmann, M. Liehr, and D. R. Young, “Defect Microchemistry at the SiO₂/Si Interface”, *Phys. Rev. Lett.* vol. 58 no. 22, pp. 2379-2382 (1987)