

Analysis of Si-Ti and Si-TiN interface after 400°C alloying

G. Lorito, H.Schellevis and L. K. Nanver

Abstract —In the present work, we have studied the 400°C alloyed Si-metal interface when using different metals. In addition to layers of Al/Si(1%) and pure Al, we have analyzed metal stacks of Ti or TiN in combination with Al/Si(1%). We have also investigated the case in which a chemical vapour deposited arsenic monolayer is interposed at the interface between the Si and the metal.

Index Terms— Schottky barrier, bipolar transistors, metal spikes, silicon precipitates, electromigration, titanium and titanium nitride, arsenic monolayer.

I. INTRODUCTION

THE use of Schottky-junction collector-contacts instead of the traditional ohmic contacts has been recognized as a potentially performance enhancing feature in several bipolar transistor advanced designs [1][2][3][4], namely the so called NPM's and PNM's. In such devices, the usual schematization of a bipolar transistor as two p-n diodes back-to-back is modified in a p-n diode (i.e. the E-B junction) back-to-back with a Schottky diode (i.e. the B-C junction). In addition to the obvious simplification of the fabrication process, the use of a Schottky junction as collector can improve both DC and AC device operations [4]. However, the resulting performance is affected by the Schottky barrier height (SBH), which in part is determined by the contacting metal. Indeed, for a given E-B junction, an important requirement is to keep low the base leakage which translates in the need of a high SBH at the collector side. Therefore, while for the PNM's the standard Al/Si(1%) can be efficiently used since it provides a SBH around 0.9-1.0 eV on the n-doped base [5], in the case of NPM's other metals are necessary. For instance, a good option is to form the Schottky junction on the p-doped base using Ti or TiN. In Fig. 1, the I-V characteristics of p-Schottky diodes made with Al/Si (1%), Ti and TiN are compared. The silicon doping at the interface with metal is around 10^{17} cm⁻³. As it can be seen, Ti and TiN give a very low reverse saturation current, I_S , which, according to the relation [6]

$$\phi_B = \frac{kT}{q} \ln \left[A_h^* T^2 \frac{A}{I_S} \right], \quad (1)$$

means a SBH, ϕ_B , around 0.5-0.6 eV on p-type silicon. In (1), T is the absolute temperature, k is Boltzmann's constant, q is the electron charge, A_h^* is the effective Richardson constant for holes (≈ 32 Acm⁻²K⁻²) and A is the contact area.

Nevertheless, besides influencing the SBH, the use of a certain metal has consequences on the subsequent alloying step in the sense that undesirable effect such as metal spikes

into the silicon and silicon precipitates (Figs. 2a and 2b) might occur. Indeed, metal spikes increase the leakage current while silicon precipitates enhance electromigration mechanisms at high current regime.

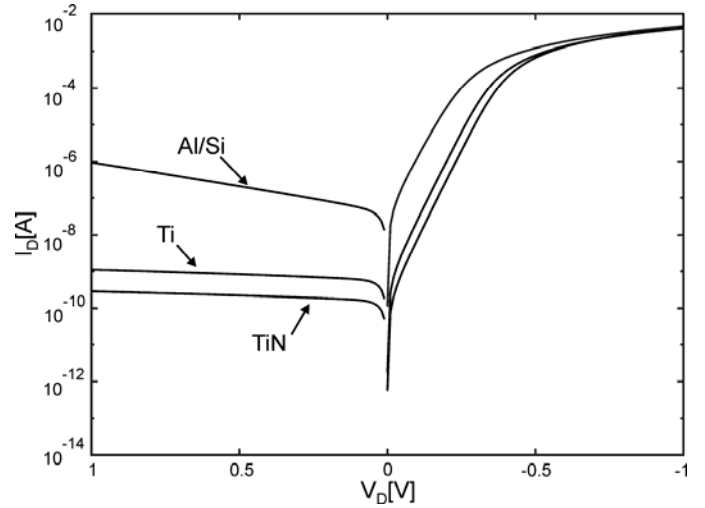


Fig. 1. I-V characteristics of p-Schottky diodes for different metals. The contact area is $40 \times 1 \mu\text{m}^2$.

In the present work, we have investigated the 400°C alloyed unimplanted Si interface metallized with different metals. In addition to layers of Al/Si (1%) and pure Al, we have analyzed metal stacks using Ti or TiN in combination with Al/Si(1%). We have also investigated the case in which a chemical vapour deposited arsenic monolayer is interposed at the interface between the Si and the metal.

II. EXPERIMENTAL MATERIAL

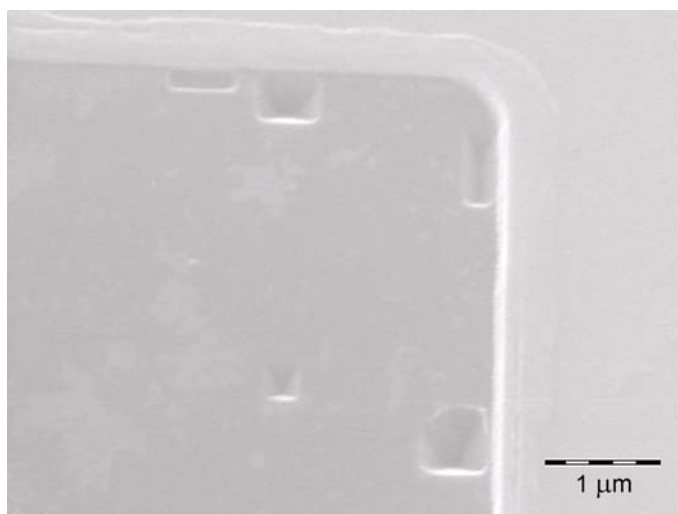
We have sputtered at 350°C several metal stacks, combining Ti or TiN layers with Al/Si(1%), in contact windows opened into 100nm Si-oxide on undoped silicon. In more detail, we have considered the metal stacks schematically depicted in Fig 3. Just before the metallization, the wafers have been dipped in HF 0.55% bath for 4 min. After the metal sputtering, we have performed a 30 min alloying step at 400°C. Then the metal has been removed by a HF 0.55% etch using an additional etching step with NH₄OH-H₂O₂-H₂O for the wafers with TiN. The SEM images of the contact openings are shown in Figs. 4 and 5. We have also carried out an experiment in which a monolayer of As has been deposited at the Si-interface before the metallization with both pure Al and Al/Si(1%). The resulting silicon interfaces after the standard 30 min alloying

at 400°C are shown in Figs. 6a and 6b. In this case the metal has been removed using a H₃PO₄-HAc-HNO₃-H₂O solution.

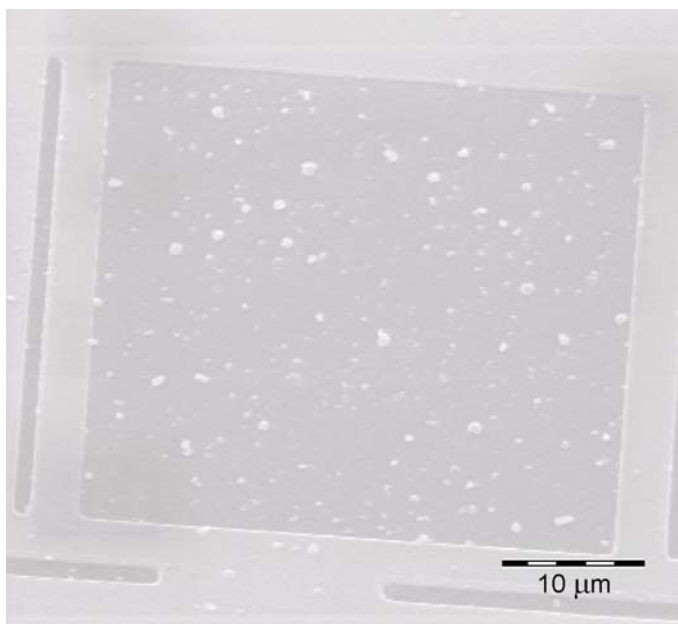
III. DISCUSSION

As well known, the use of Al as contacting metal requires the saturation the Al itself with a small content of Si (usually 1-2%) in order to avoid the spikes into silicon after the 400°C alloying step. The latter is necessary to realize an intimate contact between Si and metal and thus to minimize the contact resistivity. However, this solution presents the drawback of the formation of Si-precipitates when the metal cools down.

As Fig. 4a shows, the presence of a Ti layer at the interface with silicon can be very beneficial in the sense that neither spikes nor precipitates are observed. This suggests that a reaction between Ti and the Si present into the Al/Si(1%) layer



(a)



(b)

Fig. 2. Metal spikes in silicon (a) and Si-precipitates (b) after 30 min alloying at 400°C of Si-Al and Si-Al/Si(1%) structures, respectively.

takes place during the alloying process [7], avoiding the Si clustering and precipitation.

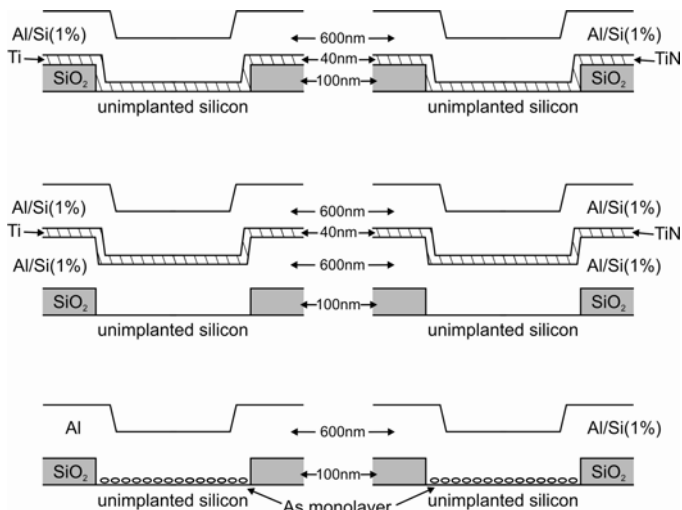
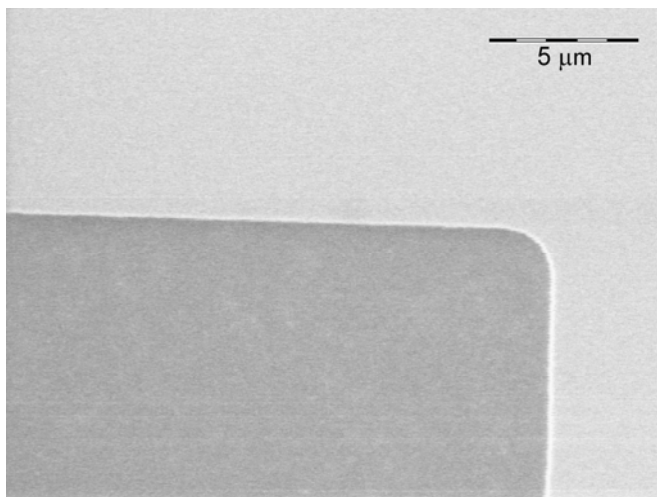
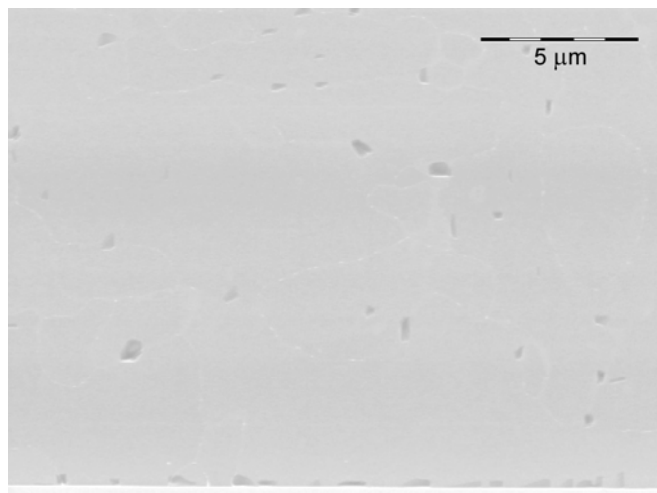


Fig. 3. Schematic pictures of the analyzed silicon-metal structures.



(a)

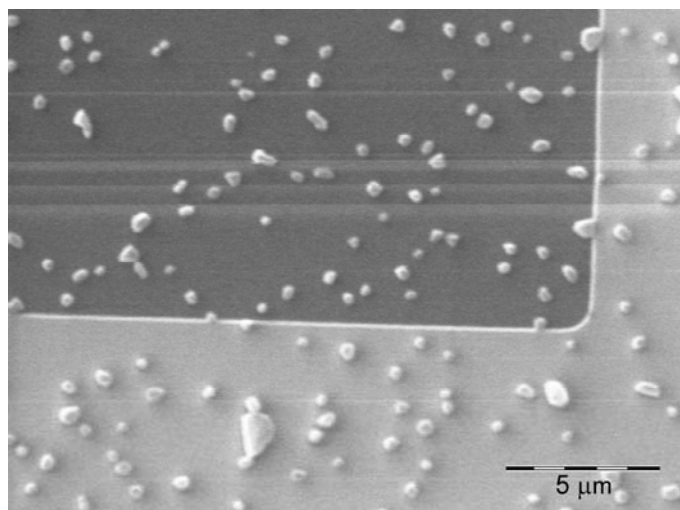


(b)

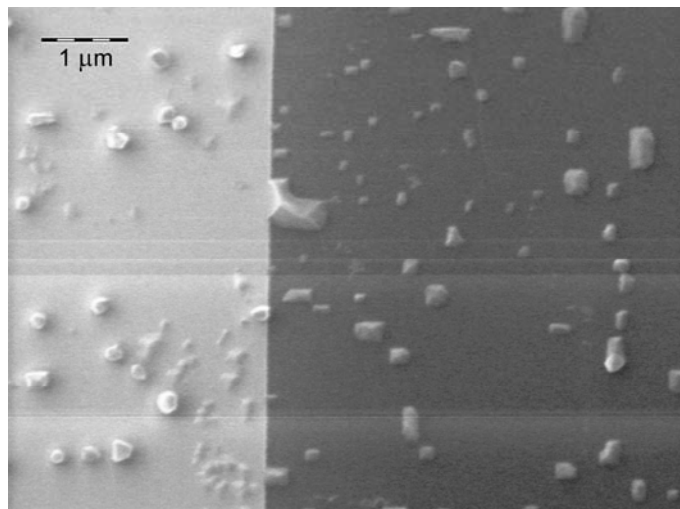
Fig. 4. SEM images of 400°C alloyed unimplanted Si-interface after metal removal in the case of Ti-Al/Si(1%) (a) and Al/Si(1%)-Ti-Al/Si(1%) (b) metal stacks.

This conclusion is also supported by Fig. 4b where the presence of the spikes into silicon can be explained by the lost of the saturating silicon content in the lower Al/Si(1%) layer due to the Si trapping action of the upper Ti layer. This capability of Ti to trap the silicon is cancelled out in TiN. Indeed, Figs. 5a and 5b show the presence of Si-precipitates when Ti is replaced by TiN.

Ultimately, Figs. 6a and 6b demonstrate that the presence of an As monolayer in between the Si interface and the metal is not effective to avoid both the spikes in the case of pure Al and the Si-precipitates in the case of Al/Si(1%).



(a)



(b)

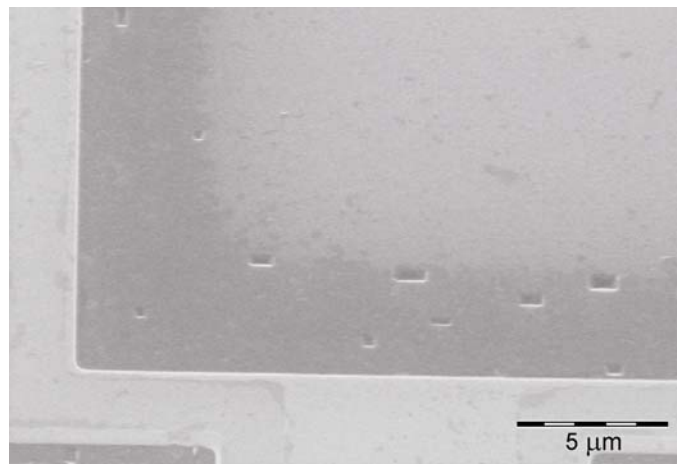
Fig. 5. SEM images of 400°C alloyed unimplanted Si-interface after metal removal in the case of TiN-Al/Si(1%) (a) and Al/Si(1%)-TiN-Al/Si(1%) (b) metal stacks.

IV. CONCLUSION

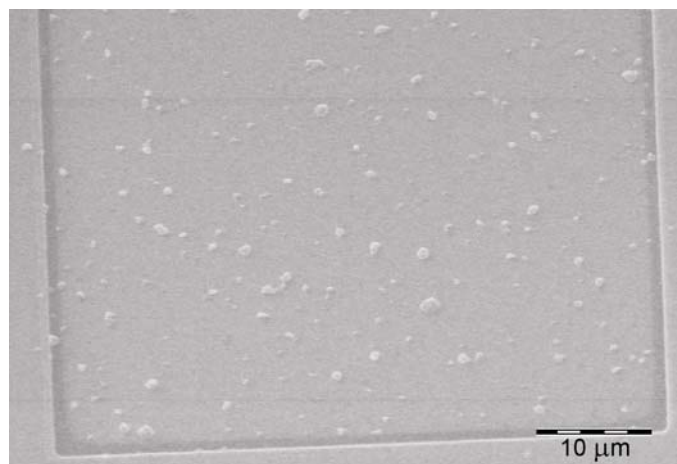
The traditional issues (metal spikes into silicon and Si-precipitates) related to the alloying process of a silicon-metal structure have been investigated in the case of 400°C alloying temperature and unimplanted silicon with several metal stacks on top. In particular, Ti and TiN have been proposed as

interfacial metals since they offer a 0.5-0.6 eV SBH on p-type silicon allowing the fabrication of very low leakage p-Schottky diodes. It has been shown that when Ti-Al/Si(1%) is used as contacting layer, Ti acts as a trap for Si during the 400°C alloying step, which results in a spike- and precipitate-free interface. However, this trapping action has not been observed when a TiN layer is used instead of Ti.

Moreover, the deposition of an As monolayer at the interface before the metallization has been proved to be not beneficial to avoid spikes and Si-precipitates.



(a)



(b)

Fig. 6. SEM images of 400°C alloyed unimplanted Si-interface after metal removal in the case of As-Al (a) and As-Al/Si(1%) (b) metal stacks.

REFERENCES

- [1] O. Nur et al., "The high-speed performance of p-Si/n-Si_{1-x}Ge_x/CoSi₂ Schottky collector HBTs", *Microelectronics Journal*, 25, 1994, pp. 399-406.
- [2] G. Lorito et al., "Offset voltage of Schottky-collector silicon-on-glass vertical PNP's", in *Proc. IEEE BCTM 2005*, pp. 22-25.
- [3] G. Lorito et al., "Reliability issues related to laser-annealed implanted back-wafer contacts in bipolar silicon-on-glass processes", in *Proc. IEEE MIEL 2006*, pp. 369-372.
- [4] M.J. Kumar and al. "A new lateral SiGe-base PNM Schottky collector bipolar transistor on SOI for non-saturating VLSI logic design," in *Proc. 16th International Conference on VLSI Design*.

- [5] Q.Ren, "Novel contacts and diodes for advanced silicon technology," Ph.D. thesis Delft University of Technology, June 2002, p. 115.
- [6] S.M. Sze, "Physics of semiconductor devices," 2nd Edition, p. 262.
- [7] D.Zhang et al., "Passivation effect of aluminum on polycrystalline silicon thin-film transistor with metal-replaced junction," *IEEE Electron Device Letters*, vol. 28, no. 2, February 2007, pp. 126-128.