

Design and Fabrication of Micromachined X-ray Sensors for Space Application

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Abstract—This paper describes the current status of the development of cryogenic X-ray sensors for space based astronomy applications by SRON in collaboration with the MESA⁺ Research Institute. Focus is given to the design and fabrication aspects of the project. Key part for the design, based on Finite Element Simulation, is the knowledge of material parameters at deep cryogenic temperatures. Measurements of these are presented. Besides the sensor array, integrated read-out structures are required. Development of these is shortly addressed.

Keywords— Microcalorimeter; cryogenic sensor; micromachining; astronomy; superconducting; MEMS; device modeling.

I. INTRODUCTION

Cryogenic imaging spectrometers most likely will have huge impact on the future of X-ray astronomy, since they combine high detection efficiency over a wide spectral band with high spectral resolution, adequate imaging and fast thermal response time. Since the initial conception of X-ray micro-calorimeters, several new types have been proposed with the Transition Edge Sensor [1] (TES) being one of the most promising today. TESs employ superconducting-to-normal phase transition thermometers that can be operated in extreme electro-thermal feedback (ETF) mode through the use of voltage bias. ETF results in stable responsivity, fast (50-100 μ s) response time, and 2 - 4 eV energy resolution in the energy band of 1 to 10 keV. Optimum response can be tuned to an energy region of interest (From sub-mm,

through visible to X-ray and gamma) by choosing an appropriate radiation absorber. Through the use of thin film deposition techniques, photo-lithography and micromachining TES based sensors can be fabricated in large pixel arrays, in practice limited by cryogenic and read-out constraints. For the next generation X-ray missions, like NASA's Constellation-X and ESA's X-ray Evolving Universe Spectroscopy mission XEUS, 32 x 32 pixel arrays are foreseen. The SRON-MESA collaboration presently optimizes 5 x 5 pixel prototype arrays. Especially the coupling of TESs with radiation absorbers in a close-packed array geometry is a topic of current investigation. TES-based micro-calorimeters have low output impedance, typically 1 - 10 m Ω , which matches extremely well with the input impedance of SQUID current amplifiers. SQUIDs can be designed with low enough noise temperature and the high bandwidth enables a multiplexing scheme for readout of multiple pixels with a single amplifier chain. The method of choice for development by the SRON-VTT [2] collaboration, Frequency Division Multiplexing, requires the use of high Q-factor, superconducting RLC filter structures, which can best be integrated on the sensor substrate.

II. TES μ -CALORIMETER BASICS

A. Operating principle

The basic physics and theoretical performance of a voltage-biased detector with a superconducting-to-

normal phase transition thermometer are well established [1, 2]. In this section we only provide the reader with the basic operating principle. Our latest work on sensor physics is published in ref. [3].

Figure 1 shows a schematic of the key components of a TES-microcalorimeter. A very simplified schematic of the biasing and readout circuit is shown in figure 2.

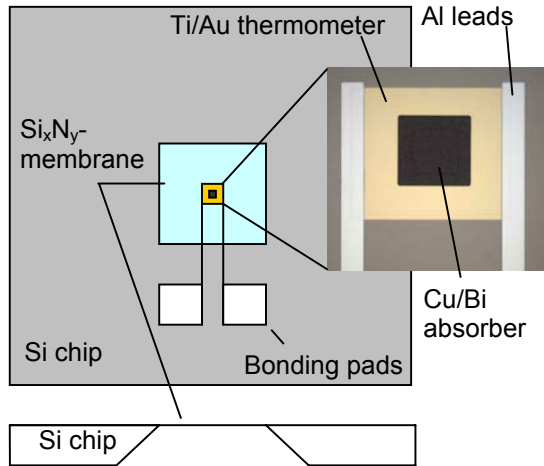


Figure 1 Schematic of a single pixel microcalorimeter (top view and cross-section). The inset is a photograph showing the lithographically fabricated thermometer and absorber.

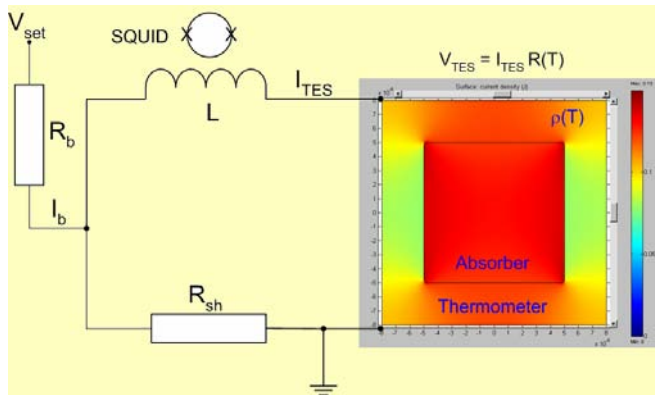


Figure 2 Schematic of the read-out circuit. The TES is represented here by a plot from a FEM simulation of the temperature dependent resistivity. The shunt resistor is much smaller than the TES resistance, providing effectively a constant voltage across the TES. The current is coupled to the SQUID based amplifier chain through an input coil.

A Cu/Bi radiation absorber is coupled to a temperature sensitive bi-layer of Ti/Au. Both structures are thermally insulated from the Si chip by placing them on a Si_xN_y membrane. The Si chip is coupled to the cold bath (~ 20 mK), provided by a $^3\text{He}/^4\text{He}$ dilution refrigerator. The Ti/Au bi-layer is a superconductor, below the critical temperature the resistance drops to zero within a few

mK. By providing a voltage bias, the absorber/thermometer assembly is heated to a temperature within the transition region (~ 100 mK). Radiation impinging on the absorber causes a small temperature rise. The resistance of the thermometer rises slightly, causing the current and heat dissipation to drop. By this electrothermal feedback the sensor is self stabilizing and the time constant to return to the set point is reduced regarding to the intrinsic C/G (heat capacity / thermal conductance) time constant. By integration of the current (difference) signal, the energy of the incoming radiation can be determined.

B. Single pixel performance

In recent years the focus has been on the optimization and the understanding of single pixel microcalorimeters. The best sensors, as produced and measured at SRON, have an energy resolution $\Delta E_{\text{FWHM}} = 3.9$ eV for 5.9 keV photons, combined with an effective time constant of 150 μs . Similar sensors equipped with a high (90%) absorption efficiency Bi absorber showed an energy resolution of 5.3 eV [4]. This level of performance is very close to the theoretical limit and is amongst the best-reported values in literature [3, 5, 6] and close to the XEUS requirements. The experience with these sensors forms the basis for the design of the array structures.

III. MICROCALORIMETER ARRAYS

A. Processing routes

In order to fulfill the performance specifications, such as energy resolution, time constant and efficiency, for each pixel, the design of the building element in a microcalorimeter array is faced with the following challenges:

- Each pixel should have the same thermal link to the cold bath, independent on the position in the array.
- The electrical and thermal cross talk between the pixels must be small enough not to degrade the energy resolution.
- Efficiency requirements lead to a close-packed design. Space must be available for electrical wiring and thermal connections.

The basic pixel design is illustrated in figure 3.

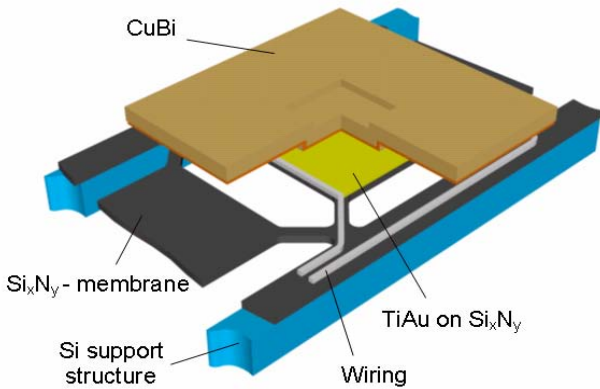


Figure 3 Conceptual design of an array pixel. The overhanging Cu/Bi absorber allows for close packing, since it creates space for slots in the Si_xN_y membrane to tune the heat conductance, and space for the connecting wiring. Mind that the aspect ratio is distorted. The lateral pixel size is about $250\ \mu\text{m}$ and the absorber thickness about $7\ \mu\text{m}$.

The two processing routes that we are investigating differ in the way the Si/ Si_xN_y supporting structure is formed. The fabrication of metal structures is identical. In the first, bulk micromachining, route anisotropic etching is used to create a Si[110] structure with deep vertical slots from the backside. The resulting beams of Si have a very low surface roughness. Measurements have shown however that the resulting thermal conductance of these beams is insufficient to provide a sufficiently low effective bath temperature to all pixels in a row. It has also been shown that a final shadow evaporated coating of Cu (typically $0.7\ \mu\text{m}$ thick) on the sides and bottom of the beams improves the thermal conduction in such a way that the bias power of typically $10\ \text{pW}/\text{pixel}$ can be conducted, while keeping the thermal gradient below $10\ \text{mK}$ in a row of 32 pixels. Figure 4 is a schematic side picture. The advantage of this processing route is the relative simplicity and proven feasibility (see the next section).

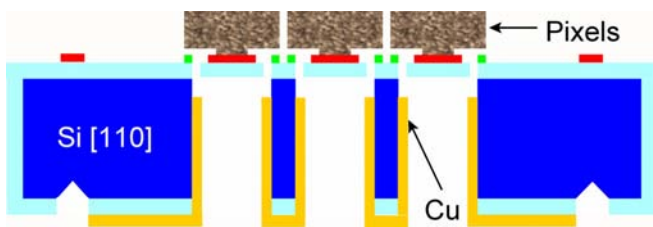


Figure 4 Schematic side view of a bulk micromachined pixel array.

An alternative processing route is based on surface micromachining. A shallow cavity underneath each membrane is created by utilizing a patterned poly-Si

sacrificial layer. The cavity is formed at the end of the production process, either by wet TMAH etching from the front side or through dry etched access holes from the backside. A schematic side view is shown below.

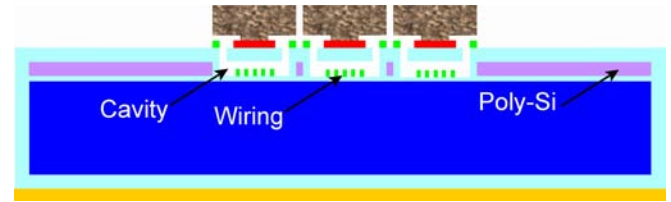


Figure 5 Schematic side view of a surface micromachined pixel array.

In comparison with the (uncoated) bulk micromachined structure the expected thermal conductance is higher, which also reduces thermal cross-talk. Furthermore, the structure is mechanically more rigid and it opens the way to bury electrical wiring under the pixel. With a given line width limitation this enables formation of a larger array. Potential problems with this processing route are related to the long (5 to 8 hours) removal step of poly-Si at high ($85\ \text{°C}$) temperature. Metal layers are prone to chemical attack and the characteristics of the Ti/Au bi-layer are changed by interdiffusion. The shift in T_c (about $20\ \text{mK}$) can be taken into account however and we found that using a coating of $5\ \text{nm}$ Ti protects all metal layers in the pixel sufficiently. Problems with sticking of the membrane to the bottom of the cavity have been solved by either forming tiny bumps under the membrane or ending the release step with a freeze drying process.

In applications where relatively large pixels are required, surface micromachined pixel arrays have the potential advantage to improve lateral uniformity of response within a pixel by creating small thermal conduction “pins” under the membrane. In large pixels response is influenced by thermal diffusion in the absorber. The feasibility of this application has been simulated by Finite Element Modeling only so far.

B. Prototype array results

Prototype 5×5 pixel micro-calorimeter arrays have been produced and tested for both manufacturing routes. In each of the arrays three pixels (side, center, and corner) are connected and operational. The other membranes are equipped with heaters, enabling operation under a condition of dissipating bias power of the whole array. Micrographs of both array types are shown in figures 6 and 7.

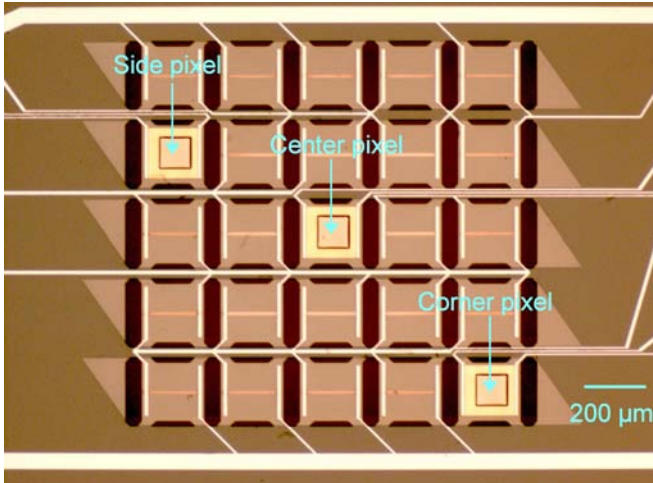


Figure 6 Annotated micrograph of a bulk micromachined 5x5 prototype microcalorimeter array. Cu-colored horizontal lines are heater strips.

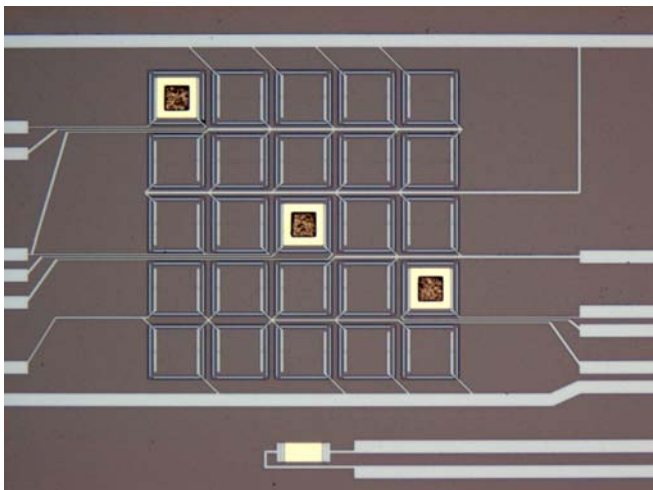


Figure 7 Micrograph of a surface micromachined 5x5 prototype microcalorimeter array. Cu heater strips (unprotected) did not survive TMAH etching. Cu absorbers are attacked too. The structure on the bottom is a thermometer for chip temperature.

As can be seen in figure 7, the surface micromachining contained problems so far. Experimental verification of an improved processing route is expected soon.

The arrays were characterized by Resistance-Temperature (R-T) traces, Current-Voltage (I-V) traces and pulse response under voltage bias for 5.9 keV X-rays. R-T traces are shown in figure 8, I-V traces in figure 9. A reasonable uniformity of response was observed. The I-V traces reveal a good temperature coefficient of resistance α of about 70 – 100 under bias conditions. The bias power in the transition equals about 2 – 4 pW/pixel, depending on the geometry of etched slots. This is considerably lower than expected on base

of measurements on single pixels on large closed membranes (e.g. section II-B). An extensive study was done to the thermal conductance of Si_xN_y membranes, using results of microcalorimeter structures and special teststructures, containing tiny heaters and thermometers. Effects of base substrate (Si[110] or [100]) and various processing conditions were investigated, but until now no conclusive explanation has been found. The geometry of the pixels is now being adapted in order to tune the bias power to about 10 pW, required for the desired time constant of 100 μs .

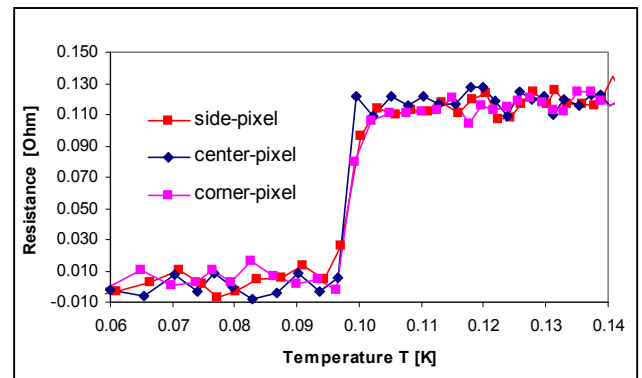


Figure 8 R-T curves for the 3 pixels, shown in figure 6.

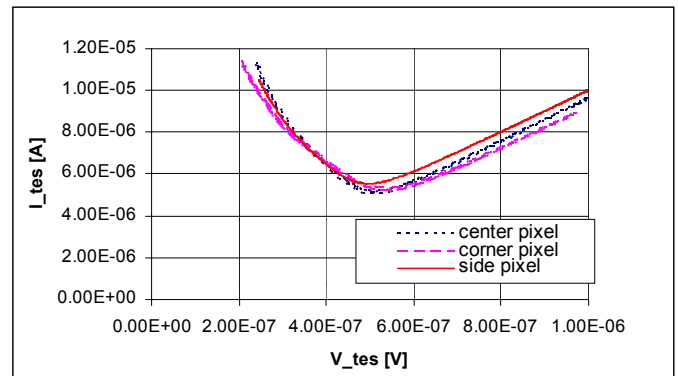


Figure 9 I-V curves for the 3 pixels, shown in figure 6.

X-ray energy resolution measurements were performed on several pixels of the bulk micro-machined arrays. The response time of the pixels varies from 0.2 to 3 ms for membrane legs with a width ranging from 200 to 15 μm , respectively. The best energy resolution measured for a few pixels equals 6 eV FWHM with excursions up to 30 eV FWHM. It is not clear so far why the measured resolution is worse than the 4 - 5 eV FWHM resolution measured quite reproducibly on single pixels. It most probably finds its origin in deteriorated experimental conditions. Work has started to improve the EM-shielding in our experimental set-up and we are in the process to move to fully differential cabling and electronics.

IV. FINITE ELEMENT MODELING

A single pixel microcalorimeter can well be modeled in one dimension with a set of coupled differential equations for the heat flow balance and the electrical circuit. Analytical expressions can be derived for the small signal response and energy resolution, based on several noise limitations, see e.g. [1, 3]. Pulse response for a large signal can be calculated by numerical integration of the differential equations.

For modeling the response of large pixels, where heat diffusion within a pixel becomes important, and the response and cross-talk in array structures, these one-dimensional models are insufficient. Two- or even three-dimensional models have to be solved with a Finite Element approach. We have built several models with commercial FEM software [7]. In the major part of our array structure the vertical dimensions (and thereby the diffusion times) are much smaller than the lateral dimensions. A 2-D approach saves numerous computing resources and the accuracy is more limited by the input material parameters. It was verified by comparison with 3-D models that in most cases also the heat flow in the bulk Si support structure can be described by a 2-D approximation.

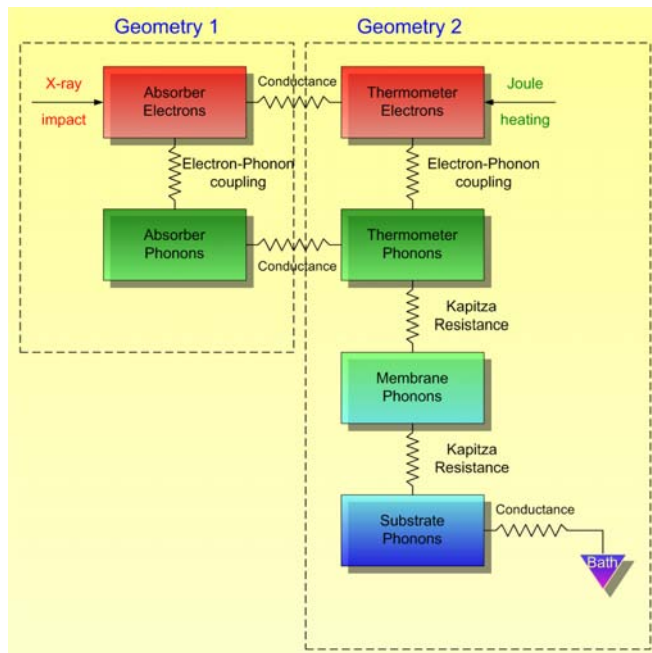


Figure 10 Thermal model of a microcalorimeter pixel. Within the blocks the 2-D heat flow equation is solved. Between the blocks within geometry a point wise coupling is applied, simulating heat exchange by electron-phonon coupling or Kapitza resistance. Joule heating is calculated in the electrical domain, the scheme was presented in fig. 2

The model for a calorimeter pixel is build up in several coupled 2-D layers, representing the energy flow by different physical processes, see figure10. The mushroom-like absorber part, see figure 3, was modeled in a separate 2-D geometry. Heat exchange by phonon- and electron conduction with the thermometer part on the membrane in geometry 2 was modeled by a point to point conductive coupling between the two geometries.

The current distribution in the thermometer layer and absorber “foot” is calculated by solving a 2-D Ohm’s law. The total current is coupled to the outside electrical circuit, represented by a 1-D ordinary differential equation, see figure 2. We exploit here the unique multiphysics properties of the FEMLAB software.

The model is first solved in stationary mode, dictated by the bias voltage and the bath temperature. The response to an X-ray impact can then be calculated by solving the time dependent equations with an approximated delta-pulse heat input in a small region in the absorber. Not only the resulting electrical pulse in the read-out circuit, but also the total heat flow through the sensor structure can be studied. An example of the simulated temperature distribution after impact of a 6 keV X-ray photon is shown in figure 11.

The accuracy of the predicted response is largely determined by the knowledge of various material parameters at deep cryogenic temperatures (around 100 mK). The past two years experiments were done with detector related teststructures, in order to get a grip on thermal conductivity and interface conductivity (also known as Kapitza resistance). We have investigated:

- Electron-phonon coupling in absorber materials (Cu, Bi, Au).
- Kapitza coupling between thermometer and Si_xN_y membrane.
- Thermal conductivity of Si_xN_y membranes, see also section IIB.
- Kapitza coupling between the membrane and the Si substrate.
- Phonon conduction in etched beams of Si
- Coupling between the Si chip and the sample holder, with and without a Cu thermalization layer.

Test structures contained small heaters and thermometers on the basis of SIN (Superconductor-Insulator-Normal metal) tunnel junctions or Ti/Au superconducting thermal “switches”. The data was analyzed with FEM models of the test structures. Most of the data is available in internal reports. Some results were published in conference proceedings [8, 9].

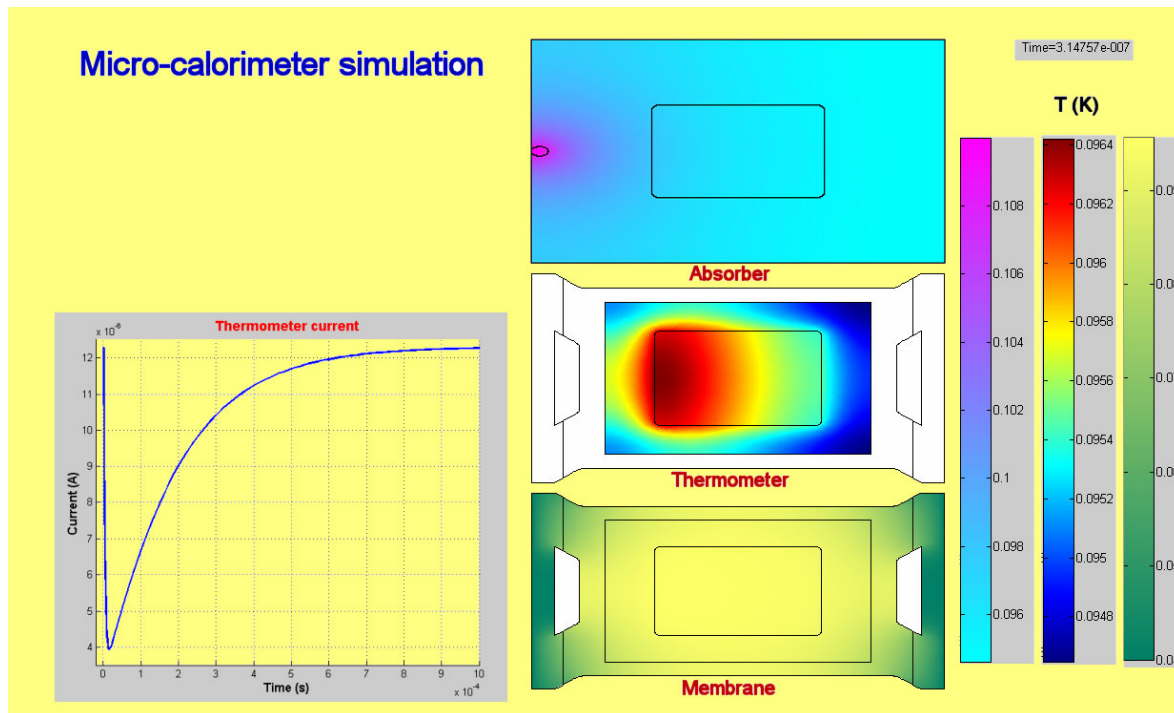


Figure 11 Sample calculated response of a calorimeter pixel to the impact of a 6 keV X-ray photon. The left graph shows electrical current as a function of time. The center pictures represent the temperature distribution 0.3 μ s after impact in the various calculation layers. Mind the different temperature scales (right) for the layers.

On the basis of the measured data, new designs have been made for prototype 5x5 arrays with all the specifications required by the XEUS mission. After successful test a decision will be made which processing route to follow for the transfer to 1000 pixel prototypes. On the basis of present fabrication technology and the thermal data this transfer is feasible.

V. ELECTRICAL READ-OUT STRUCTURES

It can be estimated that read-out of a 1000 pixel array with a SQUID based amplifier chain for each pixel would lead to unacceptable high heat load through the wiring to the cold stage. So read out schemes that reduce the amount of wiring and the number of powered-on SQUIDs will be required to increase uninterrupted observation periods. SRON has chosen to develop frequency-domain-multiplexing (FDM) [10, 11] for the XEUS application. FDM exploits the TES as a modulating element, by applying an AC bias voltage instead of the commonly applied DC bias. With the pixels biased at individual bias frequencies, the signals become separated in frequency space and can be amplified by a single SQUID amplifier.

FDM requires an LC (inductor-capacitor) blocking filter for each pixel, integrated on the detector wafer or mounted in close proximity. Because of the required voltage bias, both structures should be superconducting or contain an effective series resistance of smaller than about 1 m Ω .

A. Superconducting coils

The type of coils that we have chosen is planar coils of the “spiral-on-washer” type, schematically drawn in figure 12.

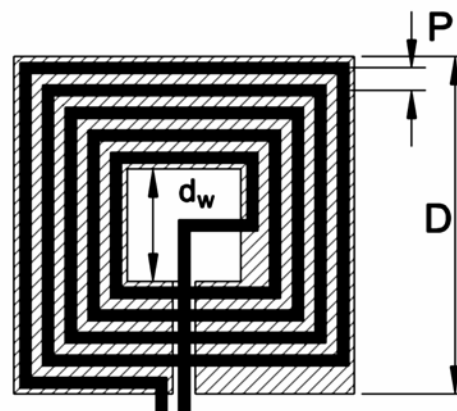


Figure 12 Schematic layout of planar inductor.

The inductance can be approximated by:

$$L = 1.25 \mu_0 d_w n^2$$

with n the number of windings and d_w the inner diameter of the washer. It is easy to show that the optimum inductance per area for a given period P of the windings is obtained when d_w equals 1/3 of the outer diameter. A small area is important, since we need many elements and preferably a large distance between elements to reduce electrical cross-talk by mutual inductance. We are currently optimizing the fabrication process, with respect to minimum obtainable period P , insulation of the return path and step coverage. We are testing the inductance of various designs and the mutual inductance at various separations. An example of one of the fabricated structures is displayed in figure 13.



Figure 13 Micrograph of the outer area of an 25 turn, 5 μm pitch coil with inner diameter 125 μm. Spiral = 45 nm Al, insulation 130 nm SiO, washer and return 180 nm Nb. Nominal value of $L = 123$ nH.

B. Capacitors

Superconducting capacitors with the required properties are not commercially available, so we are developing a process for them too. For the desired bias frequency f (1 to 10 MHz) we need a capacitance value in the range of 2.4 to 240 nF. One of the causes for an effective series resistance (ESR) is dielectric loss in the capacitors. For an ESR of ~ 1 mΩ, the quality factor $Q = 1/(2\pi f C R_{ESR})$ must be in the range 670 to 6700. In order to keep the size of the capacitors small dielectrics with a high dielectric constant are preferred. Experiments on Ta₂O₅ and Nb₂O₅ however showed insufficient Q factors of 71 [SRON] and 333 [12], respectively. Recently, experiments on (too small) capacitors with a (LP-CVD)Si_xN_y dielectric showed a Q factor of 2800. Another potential dielectric is Al₂O₃. We are presently pursuing

fabrication processes for both options, for Si_xO_y based on LP-CVD, for Al₂O₃ based on RF-sputtering. A problem with LP-CVD nitride capacitors is unwanted reaction of the base electrode, because of the high growth temperature. Finding the right protection layer is a key challenge. Because of the relatively low dielectric constant, for both routes the drive to very thin dielectrics is large, to avoid large size capacitors. We are currently working with 4 x 4 mm² size, which is estimated to be the largest practical size for the XEUS application. Problems with leakage because of thickness inhomogeneity and surface defects and on the crossing point of base and top electrode are processing challenges. For the last reason a base electrode process with a very shallow edge (~ 3 μm width) was developed by making use of a lift-off process with a large overhanging photoresist profile.

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