

A 2nd order Sigma-Delta ADC as an Interface Circuit for SOI Accelerometers

Yikun Yu, Stefan Butselaar and Kofi Makinwa

Abstract—This paper presents a fully-differential 2nd order sigma-delta analog-to-digital converter (ADC) for use as an interface circuit for silicon-on-insulator (SOI) accelerometers. The ADC is designed and fabricated in the 1 μ m 5V SOI-CMOS ABCD-3 process provided by Philips Semiconductors. The simulated dynamic range is 84dB (minimum capacitance resolution of 64aF) in a 2 kHz signal bandwidth from –40 to 150 °C. The chip area is 1.5mm² and its power consumption is 2.5mW.

Index Terms—sigma-delta ADC, interface circuit, SOI accelerometer, MEMS, autozeroing

I. INTRODUCTION

LOW-cost micro-machined (MEMS) accelerometers are widely used in applications ranging from GPS-augmented inertial navigation systems to automotive airbags, etc [1]. Such accelerometers have been implemented using a variety of surface [5] and bulk [4] micromachining technologies. Traditionally, surface-micromachined accelerometers offer the opportunity to integrate the sensor and interface circuitry on a single chip, while bulk-micromachined devices attain higher sensitivity and lower mechanical noise floor due to their large proof mass. The combination of bulk micromachining and single chip integration is ideal for low-cost accelerometers.

Fig 1 shows a silicon-on-insulator (SOI) accelerometer [2] being developed for this purpose. The electronic circuits are processed on the top silicon layer of a SOI wafer, and the silicon handle wafer (substrate) is etched down to the buried oxide layer to form an accelerometer.

The aim of this work is to design readout and signal-processing circuits for SOI accelerometers. This paper presents a fully-differential 2nd order sigma-delta analog-to-digital converter (ADC) as interface circuit. The sigma-delta ADC [6] is used due to its wide dynamic range, inherent

linearity and relaxed accuracy requirements on the analog circuits. The fully differential circuit reduces the common mode errors such as substrate and power supply noise. The interface circuit is designed and fabricated in the 1 μ m 5V SOI-CMOS ABCD-3 process provided by Philips Semiconductors. The simulated dynamic range is 84dB (minimum capacitance resolution of 64aF) in a 2 kHz signal bandwidth from –40 to 150 °C. The chip area is 1.5mm² and its power consumption is 2.5mW.

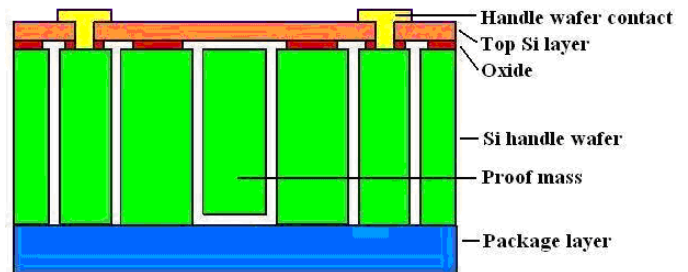


Fig 1 An SOI accelerometer

II. ADC ARCHITECTURE

A. Accelerometer model

Fig 2 shows the schematic of a fully differential capacitive accelerometer [3]. C_{s1} , C_{s2} , C_{s3} and C_{s4} are the sensing capacitors between the proof mass fingers and the four sensing electrodes. In the presence of external acceleration A_{ext} , the proof mass moves along the sense axis with respect to its frame ($X = Y - Z$) and changes C_{s1-4} . Here C_s is the total sensor capacitance and ΔC_s is the change of sensing capacitance that can be measured using electronic circuitry.

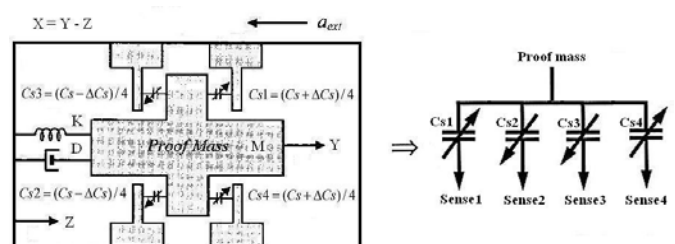


Fig 2 Fully differential capacitive accelerometer

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B. Second-order Sigma-delta ADC

Sigma-delta ($\Sigma\Delta$) ADCs combine sampling rate well above the Nyquist rate with negative feedback and digital filtering in order to trade-off resolution in time with that in amplitude.

Fig 3 shows the architecture of the 2nd-order sigma-delta ADC intended as an interface circuit for accelerometers. The sensor is directly connected to the 1st integrator [8]. The 1st integrator also acts as a capacitance-to-voltage converter that converts the sensor signal into a voltage. A clock frequency of 600-kHz is required for 16-bit accuracy in a 2-kHz signal bandwidth. Detailed design of the sigma-delta ADC will be described in the next section.

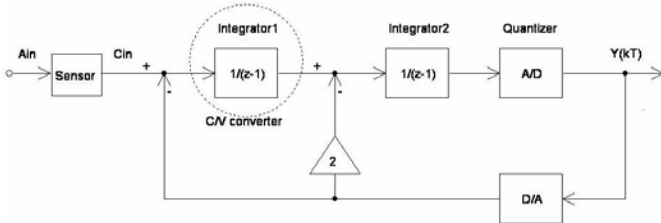


Fig 3 $\Sigma\Delta$ ADC for accelerometers in which the 1st integrator acts as a C/V converter

III. ADC CIRCUIT DESIGN

A. The 1st Integrator

The 1st integrator is very important. First, it directly interfaces with the sensor by functioning as a capacitance-to-voltage converter. In addition, the noise and distortion of the ADC is determined primarily by the noise and distortion of the 1st integrator. The noise and distortion from the 2nd integrator and comparator, referred back to the ADC input, are attenuated by the gain of the 1st integrator, which is large in the signal bandwidth [6].

Fig 4(a) shows a fully differential switched-capacitor (SC) charge integrator. The common-electrode of sensing capacitors C_{s1-4} , which is the proof mass, is always connected to DC voltage source $0.5 \cdot V_{ref}$ [3]. The integrator has two non-overlapping clock phases: the pre-charge phase P1 and the charge-integration phase P2. During P1, the right electrodes of C_{s1-4} track V_{ref} , ground, V_{ref} and ground, respectively. During P2, the right electrodes of C_{s1-4} connect to the op-amp input. The common-mode charges from C_{s1-4} cancel each other, which not only set the input common-mode voltage of the op-amp to $0.5 \cdot V_{ref}$, but also reduce requirement of common-mode rejection ratio (CMRR) of the op-amp. And the differential charges from C_{s1-4} , due to the change of sensing capacitance ΔC_s , go to the integrator output and change the op-amp output voltage by:

$$\Delta V_{out} = \frac{\Delta Q}{C_{int1,2}} = \frac{V_{ref}}{2} * \frac{C_{s1} - C_{s2} - C_{s3} + C_{s4}}{C_{int1,2}} = \frac{V_{ref}}{2} * \frac{\Delta C_s}{C_{int1,2}} \quad (1)$$

Circuit noise in the $\Sigma\Delta$ ADC includes quantization noise and electronic noise from switches and operational amplifiers. To qualify the effects of electronic noise of the 1st integrator, all the electronic noise is first referred to at the integrator's output. Then they are converted to an equivalent capacitance resolution ΔC_s by dividing by the transfer function (1).

In contrast to other sources of circuit noise, the op-amp flicker noise is dominant at low frequencies and cannot be reduced by increasing the over-sampling ratio. There is a 3dB improvement for every doubling of transistor gate area. However, a much more efficient method to reduce flicker noise, which is naturally compatible with switched-capacitor circuits, is to employ an autozeroing operation in the 1st integrator.

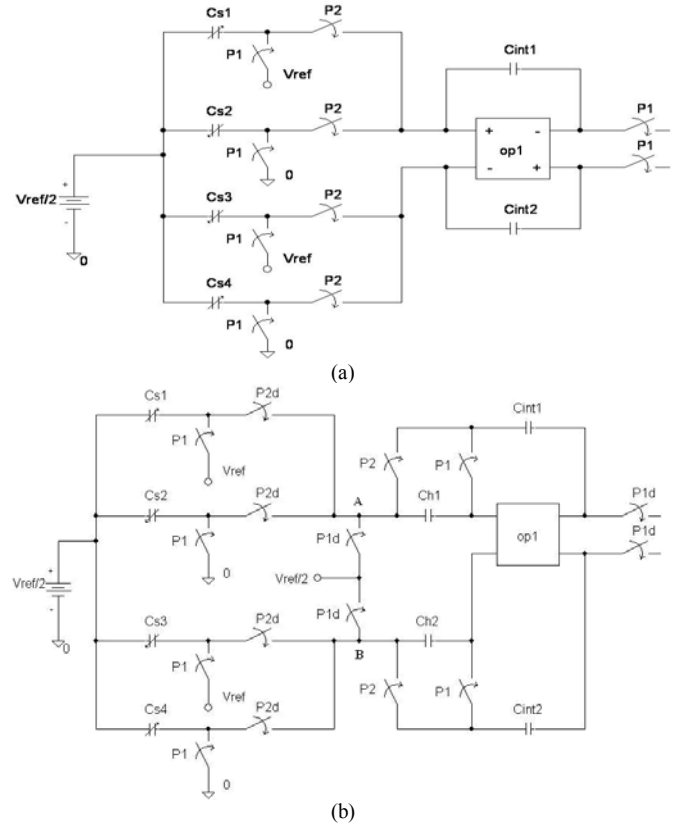


Fig 4(a) A fully differential SC charge integrator; (b) The integrator with autozeroing

The principle of autozeroing involves subtracting a recent sample of a time varying noise from the same noise [7], thus canceling dc and low frequency noise. Fig 4(b) shows the 1st integrator with autozeroing by using two extra offset-storage capacitors C_{h1} and C_{h2} . During P1, C_{s1-4} are pre-charging the same as in Fig 4(a). The left electrodes of C_{h1-2} (node A and B) are connected to DC voltage source $V_{ref}/2$. Due to negative feedback and large op-amp dc gain, the flicker noise voltage V_n is stored onto C_{h1-2} . During P2, the voltages that stored on C_{h1-2} remain unchanged and cancel the present flicker noise. Thus the flicker noise voltage appears at

node A and B is $V_n \cdot (1-z^{-1})$. Due to the large over-sampling ratio, it is negligible during the signal charge integration.

The circuit noise simulation was performed in SPECTRE® using periodic steady state (PSS) and periodic noise (PNOISE) analyses [9]. In the simulation, the total sensor capacitance $C_s = 8\text{pF}$, $C_{h1-2} = 2\text{pF}$, clock frequency $f_s = 1\text{MHz}$ and signal bandwidth $f_B = 2\text{kHz}$. Fig 5 shows a comparison of the total output noise voltage of the 1st integrator with or without autozeroing. Without autozeroing, the flicker noise (35uV) is obviously dominant in the signal bandwidth and limits resolution. The autozeroing operation cancels flicker noise effectively, and thus the switch noise (kT/C noise) and the op-amp thermal noise become dominant. There is 12dB improvement in the capacitive resolution due to the autozeroing operation.

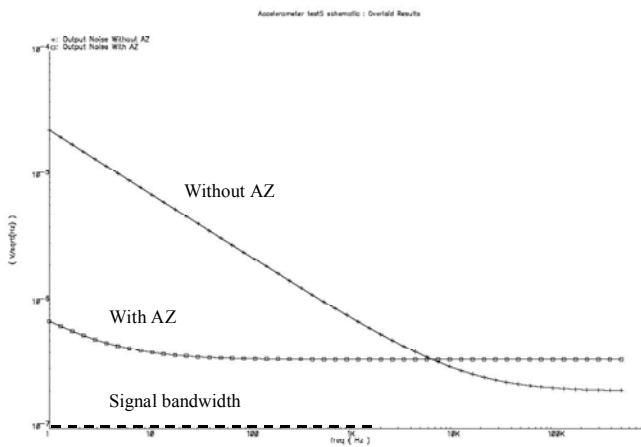


Fig 5 A comparison of the total output noise voltage in the 1st integrator with or without autozeroing

Fig 6 shows the 1st integrator with a 1-bit DAC added to Fig 4. The left electrodes of the feedback C_{fb1-2} are always connected to DC voltage source $0.5 \cdot V_{ref}$. During P1, the right electrodes of C_{fb1-2} track V_{ref} and ground respectively. During P2, the right electrodes of C_{fb1-2} connect to the op-amp input. The differential reference charges go out of C_{fb1-2} . The comparator decision $Y+$ and $Y-$ decide whether C_{int1} and C_{int2} receive a positive or negative reference charge. If $Y+$ is high (and $Y-$ is low), C_{int1} receives a positive reference charge and C_{int2} receives a negative reference charge. If $Y+$ is low, the charge delivery is swapped.

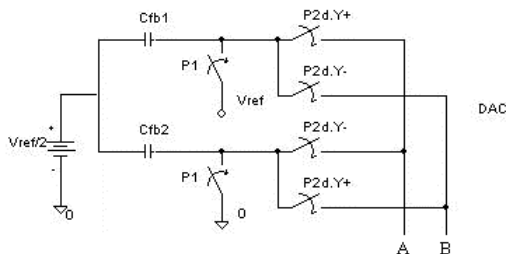


Fig 6 The 1-bit DAC

B. The 2nd Integrator

The 2nd integrator is less challenging than the 1st integrator and is skipped here for the sake of brevity. For low power consumption, its capacitors are 2.5 times smaller than those used in the 1st integrator.

C. The op-amp

Fig 7(a) shows the op-amp used in the integrators. A PMOS folded cascode op-amp is used in this design due to its high dc gain, high speed and large output range [10]. Fig 7(b) shows the common-mode feedback (CMFB) circuit for the op-amp by using switched-capacitors [10]. V_{bias} is the bias voltage for the tail current source N_{3-4} . V_{ref} is the desired output common-mode voltage of the op-amp. Switched-capacitor C_1 functions as a resistive divider. If V_{out1} and V_{out2} are not centered at V_{ref} , the switched capacitors C_1 will adjust the gate-voltage of N_3 and N_4 (V_{ctrl}) to provide the correction. C_2 perform a hold function. C_1 and C_2 sized to be comparable to the transistor parasitics. The main feature of this CMFB circuit is its larger output range than other approaches, e.g. by using CMOS transistors in the linear mode or by using an additional op-amp [10].

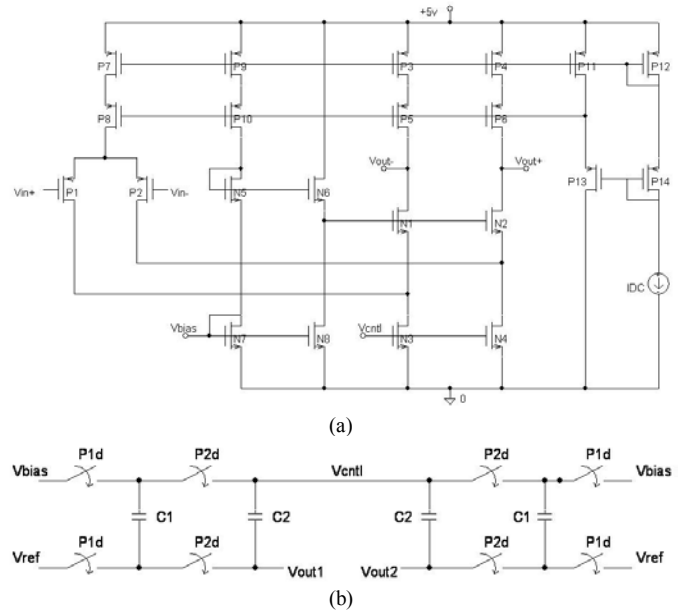


Fig 7(a) PMOS folded-cascode op-amp and bias circuits; (b) Common-mode feedback using switched-capacitors

D. Comparator

The performance of the modulator is relatively insensitive to comparator offset and hysteresis, since their effects are attenuated in the signal bandwidth by the 2nd-order noise shaping the same as the quantization noise. A simple regenerative latch without preamplification or offset cancellation fulfills the comparator requirements [6].

IV. SIMULATION RESULTS

The ADC shown in Fig 3 was simulated using device-level models. The input signal is $\Delta C_s = 0.25\text{pF}$ at 500Hz.

Fig 8 shows the two-level digital bit-stream at the output of the ADC in time domain. The duty cycle of the output pulse follows the input signal ΔC_s .

Then the output bit-stream was windowed by a Hann window and the FFT is used in post-processing. A dc offset of 10mV was added at the input of the 1st op-amp.

Fig 9 shows the output spectrum of the ADC in frequency domain with autozeroing in the 1st integrator. The signal amplitude of -12dBR at 500Hz is shown. The 2nd order quantization noise shaping of 40dB per decade is also shown and most of the quantization noise power is moved to higher frequencies outside the signal bandwidth. The signal to noise-and-distortion ratio (SNDR) is 95dB. The FFT bin at the lowest frequency is due to frequency smearing of dc offset by Hann window and its power is -109dBR . In contract, its power is -38dBR without autozeroing. This shows that the autozeroing operation effectively reduces op-amp dc offset together with flicker noise.

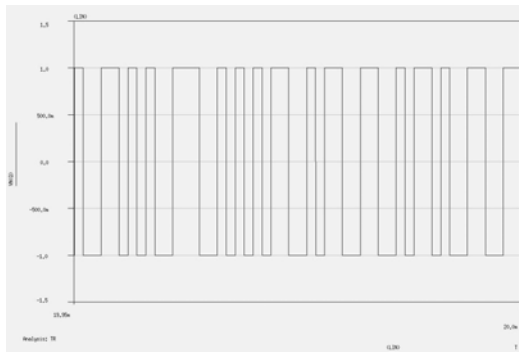


Fig 8 Output digital bit-stream in time domain

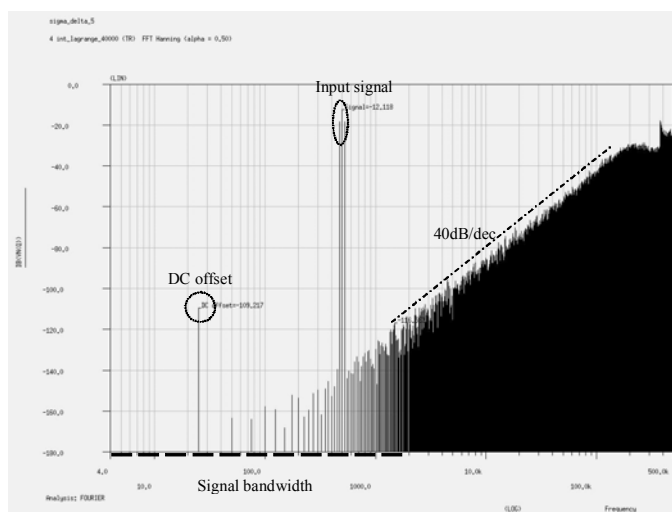


Fig 9 Output spectrum of the ADC with autozeroing

The ADC has good performance over supply voltage range of 4.75 to 5.25V, temperature range of -40 to 150 °C and process spread in simulation. The dynamic range is 84dB

(minimum capacitance resolution of 64aF) in a 2 kHz signal bandwidth from -40 to 150 °C. The chip area is 1.5mm^2 and its power consumption is 2.5mW.

V. CONCLUSION

This paper has presented a fully-differential 2nd order sigma-delta ADC for use as an interface circuit for SOI accelerometers. The sensor was directly connected to the 1st integrator and autozeroing operation was used to cancel flicker noise and thus achieve higher resolution. The ADC provides high resolution (14-bit) with low power consumption (2.5mW) and is suitable for automotive applications.

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