

A Low-Power Small-Area 1-bit Full Adder Cell in a 0.35 μm CMOS Technology for Biomedical-Oriented System-on-Chip Applications

Alexander Mora-Sanchez, and Wolfgang H. Krautschneider

Abstract—In this paper a low-power small-area 1-bit CMOS-based adder cell is being introduced. It needs only 14 transistors and relies on low-power XOR/XNOR cells, transmission function logic and pass-gate logic cells to compute the sum and carry-out bits with rail-to-rail output swing. The proposed adder cell, which has been designed and laid out according to the layout requirements of a 0.35 μm 3.30 V CMOS technology, consumes 45% less power and occupies 47% less area than the 28-transistor standard cell provided by the technology supplier, making it attractive for being used in low-power applications, such as in a biomedical-oriented system-on-chip design.

Index Terms—System-on-chip, full adder, short-circuit power, dynamic power.

I. INTRODUCTION

THE demand of high-performance low-power microelectronic-based circuits for biomedical applications grows continuously in order to boost the development of innovative medical devices and medical technologies, which are actually indispensable for delivering high-quality healthcare [1]. In contrast to that proposed in [2], a biomedical-oriented system-on-chip (SoC) that encapsulates a number of subsystems (e.g. analogue front-ends, analogue-to-digital converters, dedicated digital filters, a digital signal processor and related memory) for the acquisition, digitisation and processing of biosignals (e.g. electrocardiographic signals) will help develop less power consuming (i.e. battery powered), more compact and more versatile systems. Consequently, low-power design and small-area circuits are mandatory for the design of such SoC.

Because addition operations are extensively used in digital signal processing, a low-power small-area 14-transistor 1-bit adder cell with rail-to-rail output swing is presented. The cell is designed and laid out in a 0.35 μm 3.30 V CMOS technology and is meant to replace the 28-transistor 1-bit standard CMOS adder [3] provided by the technology

supplier. Several few-transistor-count adder cells have been proposed in the literature [4]-[5], but have the disadvantage of demanding more than 14 transistors, which negatively impact the area of the cell, or of not producing full swing output signals, which worsens the noise margin and the driving capability of the cell, and makes subsequent buffering stages dissipate considerable amounts of power.

This paper is organised as follows: Section II addresses the principle of operation of the proposed 14-transistor adder cell; functional verification of the proposed 1-bit adder, including a comparison against the cells reported in [4]-[5] and the 28-transistor standard CMOS adder, is done through simulations, the results of which are discussed in Section III; in Section IV the design flow for the creation of the customised digital cell that can be used in the computer-assisted synthesis, and floorplanning, placement and routing (FPR) flows of digital designs is reviewed; conclusions are given in Section V. This paper complements also the work presented in [6] about low-power analogue-to-digital conversion for SoC applications.

II. PRINCIPLE OF OPERATION OF THE PROPOSED 1-BIT ADDER

A 1-bit adder cell is a digital circuit that takes three 1-bit inputs A , B , and C_{in} , to produce two output bits S and C_{out} , according to the following Boolean equations:

$$\begin{aligned} S &= A \oplus B \oplus C_{in} \\ C_{out} &= A \cdot B + C_{in} \cdot (A \oplus B), \end{aligned} \quad (1)$$

which represent the result of the binary sum of the operands A , B , and C_{in} . Recognising the sources of power dissipation of a particular MOS circuit implementation of (1) is important in order to design efficiently the full adder cell at the transistor level. According to the formula [7]

$$P = V_{dd} \cdot f_{clk} \cdot \sum_n \alpha_n \cdot C_n + V_{dd} \cdot \sum_n I_{sc,n}, \quad (2)$$

the power P consumed in a digital CMOS circuit depends on the supply voltage V_{dd} , the clock frequency f_{clk} , the internal node switching activities α_n , the internal node capacitances C_n , the internal short-circuit currents $I_{sc,n}$, and the number of internal nodes n . The first term in (2) is referred to as dynamic

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power, the second term, as short-circuit power. Thus, if the 1-bit adder cell is to be designed efficiently, assuming that V_{dd} and f_{clk} are fixed parameters and that the switching activity is controlled at the architectural level, the circuit implementation has to have as few transistors (preferably with minimum feature size), circuit nodes and direct paths between the power supply and ground as possible. The former indication aims at decreasing the amount of capacitive loads (i.e., at decreasing the dynamic power component) whereas the latter, the short-circuit currents (i.e., the short-circuit term). Note that these measures also help decreasing the physical size of the cell. To avoid increasing the short-circuit power in subsequent buffering stages, the adder cell must deliver full swing outputs.

In order to address the indications cited above, the approach of [8] is followed. It states that (1) can be rewritten as

$$S = H \oplus C_{in} = H \cdot \overline{C_{in}} + \overline{H} \cdot C_{in} \quad (3)$$

$$C_{out} = A \cdot \overline{H} + C_{in} \cdot H,$$

where

$$H = A \oplus B; \quad (4)$$

therefore, the adder can be divided into three modules, as seen in Fig. 1. On the one hand, *module-2* is efficiently devised using the transmission function implementation of an XOR gate shown in Fig. 2(a), which allows the module to have minimum transistor count, provide a full output swing, and consume the lowest average power. On the other hand, *module-3* is efficiently implemented as a pass-gate 2-to-1 multiplexer with H acting as the “select” input. Hence, *module-3* is able to provide rail-to-rail outputs. Its schematic is depicted in Fig. 2(b).

Concerning the conception of the *module-1*, it is desirable that H and its complement feature a full swing to enhance the signal integrity characteristics of these signals and to assure a rail-to-rail swing at the S output. This can be done if *module-1* is realised as suggested in [5] and shown in Fig. 2(c). The cross-coupled PMOS transistors perform a pseudo-XOR operation, since they disable themselves for $A=B=“1”$. Besides, they are not able to fully pass a logic “0”. Similarly, the cross-coupled NMOS transistors are not able to fully pass a logic “1”, performing a pseudo-XNOR operation, since they disable themselves for $A=B=“0”$. It is precisely the function of the additional NMOS and PMOS transistors, which are connected in a positive-feedback configuration, to circumvent these problems. When $A=B=“1”$ occurs, the node H is driven to a full logic “0”, and its complement to full logic “1”, through the action of the cross-coupled NMOS transistors and the positive-feedback. Likewise, for the combination $A=B=“0”$, the cross-couple PMOS transistors initially passes a signal close to ground at node H , and the positive-feedback action produces a full logic “0” and a full logic “1” at node H and its complement, respectively.

Hence, the proposed low-power small-area 1-bit adder cell

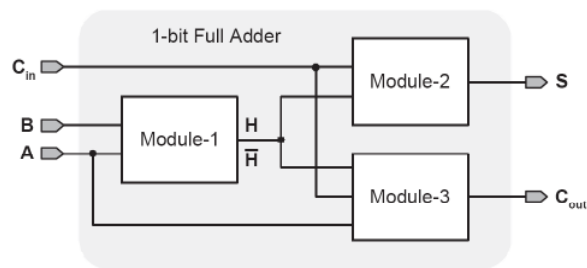
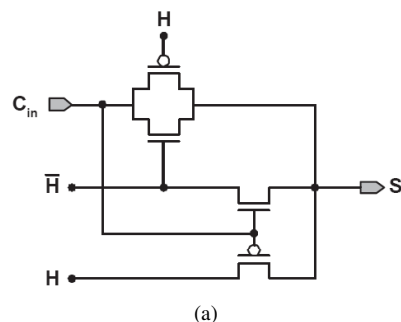
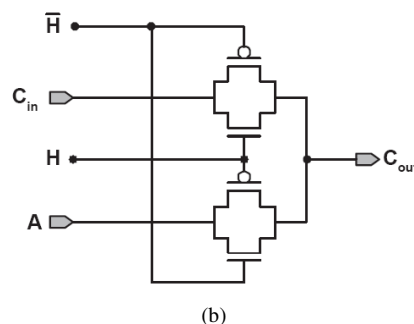


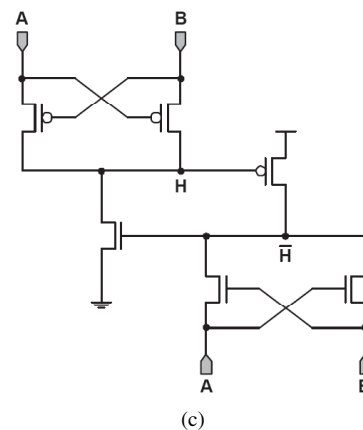
Fig. 1. Modularization of the 1-bit full adder.



(a)



(b)

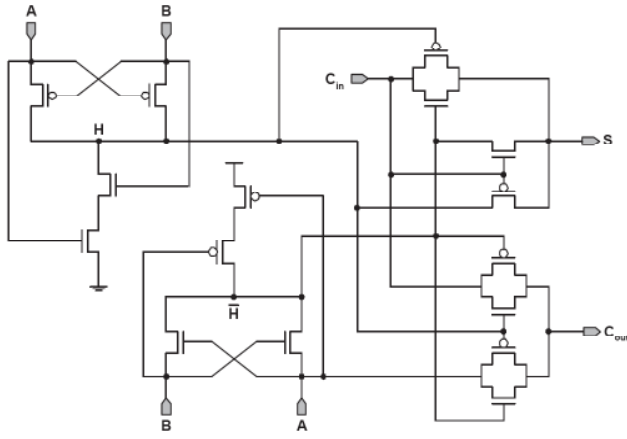


(c)

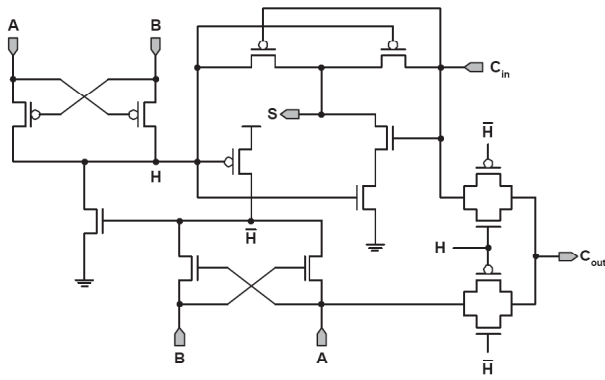
Fig. 2. Realization of (a) *module-2*, (b) *module-3*, and (c) *module-1*.

is made up of the modules presented in Fig. 2, and can be considered as the optimum ensemble out of the low-power (LP) full adder found in [4] and the N-Cell1 adder found in [5]. The schematic views of the LP, the N-Cell1 and the proposed cell are drawn in Fig. 3.

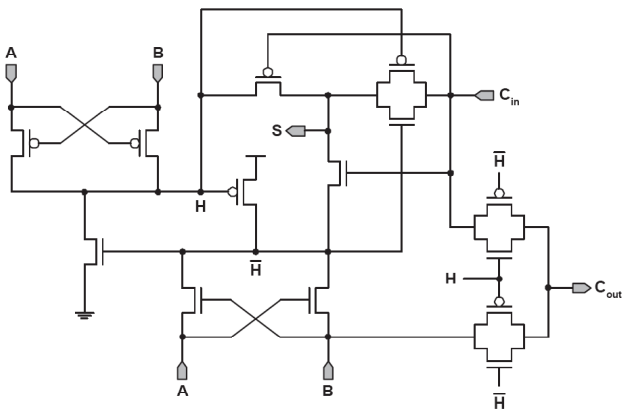
Many other 1-bit adder cells reported elsewhere [9] prove to have more transistors and consume more power at the



(a)



(b)



(c)

Fig. 3. Transistor-level implementation of the (a) LP, (b) N-Cell1, and (c) proposed 1-bit adders.

reference switching frequency of 50 MHz. Novel low-power adder cells claim to use 14 [10], 12 [11] or even 10 transistors [12]; however, the way they present their simulation results is quite ambiguous due to the fact that the output voltage levels of the cells are known to be severely degraded [9] and they do not take into account that this makes the short-circuit currents

TABLE I
SUMMARY OF PRE-LAYOUT SIMULATION RESULTS

Cell	N°. of transistors	Full swing outputs	Power drawn by (in μW @ 50 MHz)	
			Cell	Output buffers
Standard	28	Yes	12.48	30.43
LP	16	Yes	8.27	31.35
N-Cell1	14	No	3.90	57.22
Proposed	14	Yes	3.84	32.06

TABLE II
POST-LAYOUT SIMULATION RESULTS

Cell	Area	Power (@ 50 MHz)	Delay (ns)
Standard	$13.0 \mu\text{m} \times 21.0 \mu\text{m}$	13.93 μW	0.55
Proposed	$13.0 \mu\text{m} \times 11.2 \mu\text{m}$	7.63 μW	1.20

of subsequent buffer stages greatly increase. For this reason, these novel cells are deemed to be inefficient in terms of power consumption compared to the proposed adder cell.

III. SIMULATION ENVIRONMENT AND RESULTS

The simulation environment emulates a very-likely operating scenario, wherein inverters (buffers) drive the cell's inputs whereas the S and C_{out} outputs are loaded with an inverter, each of which drives a lumped capacitance. The simulations are carried out with Cadence Spectre.

Functional verification is done by applying to the inputs A , B , C_{in} , a Matlab-generated 3-bit pattern with all possible 64 transitions (since each input exhibits 4 possible transitions, namely, "0" \rightarrow "0", "0" \rightarrow "1", "1" \rightarrow "1", and "1" \rightarrow "0"). This also permits to look for the worst-case timing. Functional verification has been run on the structures of Fig. 3 for a $0.35 \mu\text{m}$ 3.30 V CMOS technology, assuming a 50 MHz switching frequency and using feature sizes close to minimum (transistor aspect ratio is smaller than 1.43). A snapshot of the waveforms generated by the N-Cell1 and the proposed adders is appreciated in Fig. 4. As expected, the results showed that all cells satisfied (1). Note that the S output signal of the N-Cell1 adder is not rail-to-rail though.

Estimations of the power dissipation are conducted by applying a Matlab-generated random sequence of 1000 bits to each input, where the "0" and "1" are generated with equal probability [9]. The switching frequency of the pattern as well as its transition times are set in Matlab. The average power of the cells is then computed with Spectre. Power estimations have been computed on the pre-layout versions of the structures of Fig. 3 as well as on the 28-transistor standard CMOS 1-bit adder found in the $0.35 \mu\text{m}$ technology digital library, assuming a switching frequency of 50 MHz, and a lumped capacitance of 100 fF. The results are contained in Table I.

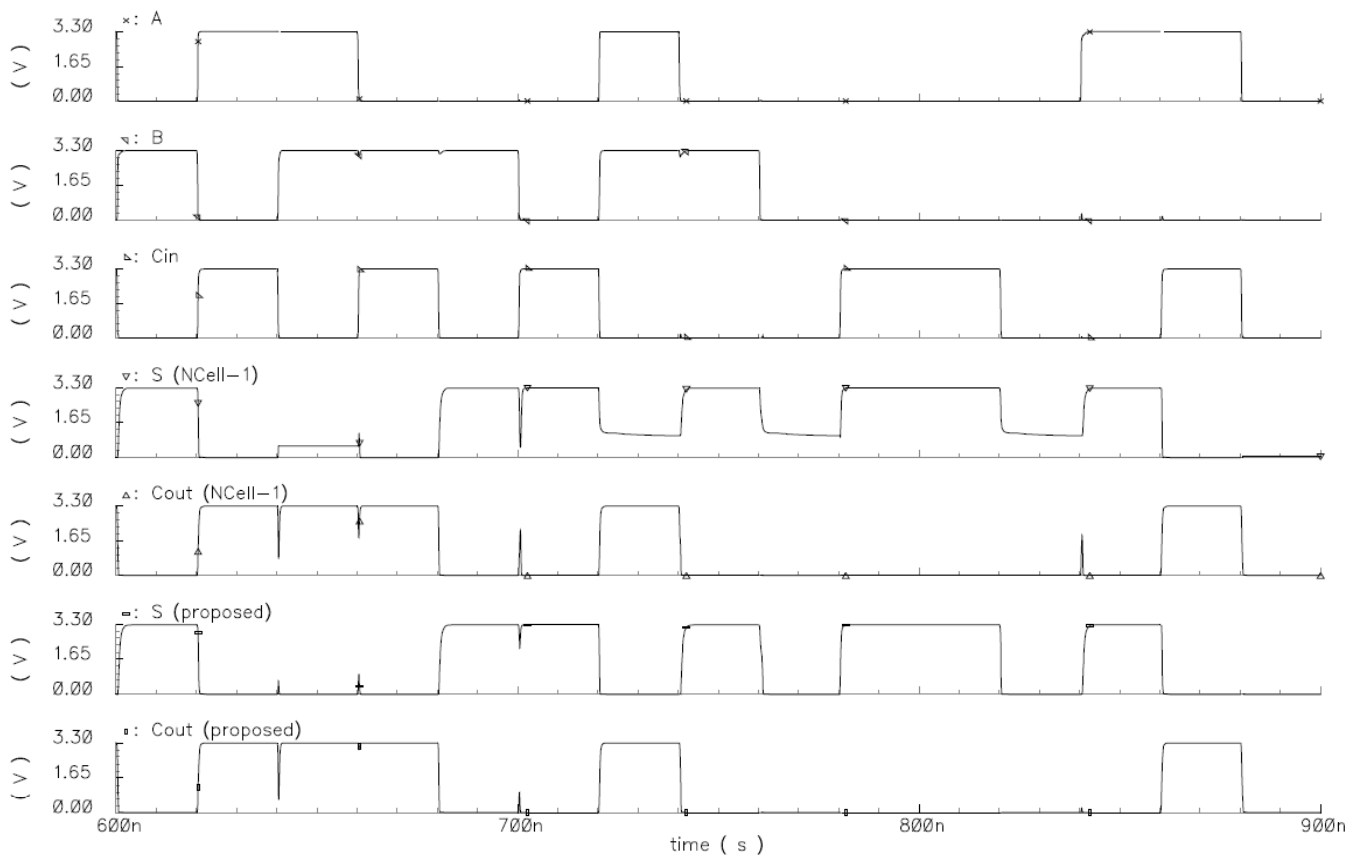


Fig. 4. Snapshot of the waveforms generated by the NCell-1 and the proposed adder. The waveforms of the LP adder (not shown) simply follow those of the proposed adder.

Table I shows that the N-Cell1 and the proposed adder are good candidates for small-area design; but, it is the proposed cell who achieves full swing outputs, consumes itself the lowest power and makes the output buffers it drives dissipate far less power than those driven by the N-Cell1 adder. Therefore, it is the proposed cell the one that satisfies the small-area and low-power requirements demanded in SoC-based applications.

Functional verification and power estimations have been also carried out after backannotating post-layout parasitic information on both the proposed cell and the standard CMOS cell. Post-layout simulation data are shown in Table II, the actual cell layout, in Fig. 5. The proposed cell is 47% smaller and dissipates about 45% less power. Nevertheless, it is slower than the standard adder by a factor of 2. This, however, does not represent a problem since many biomedical signals are low-bandwidth.

IV. DESIGN FLOW OF THE CUSTOMIZED DIGITAL CELL

A Cadence-based design flow has been followed after proving the feasibility of the proposed cell in order to include it in the synthesis and FPR flows of major digital circuits. The main steps are:

- Schematic entry with Virtuoso Schematic Composer.
- Layout completion with Virtuoso Layout-XL Editor.

- Generation of the *lib*- and Timing Library Format (TLF) files containing timing characterisation data. The Cadence Open Command Environment for Analysis (OCEAN) tool is well recommended for this task.
- Creation of the abstract view with Cadence Abstract Generator. This view, seen in Fig. 6, is created based on the layout view and is used to generate the Library Exchange Format (LEF) file containing the cell's physical data.

The resulting *lib*-file is used by Synopsys tools (i.e. Design Compiler, Prime Time) to perform logical synthesis and/or static timing analysis of the gate-level synthesised circuits. Subsequently, the LEF file, which contains the basic physical information to instruct the FPR tool about the cell dimensions, pins location and metal obstructions; as well as TLF file, are used to run the FPR flow in Cadence Silicon Ensemble.

V. CONCLUSIONS

A 14-transistor low-power small-area 1-bit full adder cell in a 0.35 μm 3.30 V CMOS technology has been proposed. Compared to the standard 28-transistor CMOS adder found in the technology library, it occupies about half the size and saves about 45% of power. Therefore, the proposed cell is suitable for being used in low-power SoC-based applications.

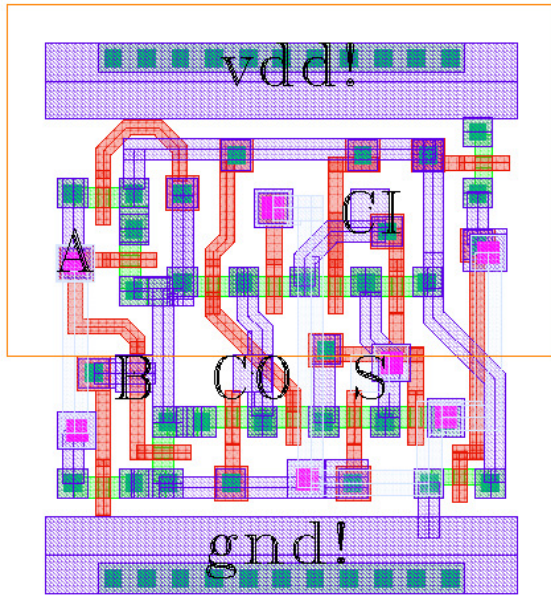


Fig. 5. Layout view of the proposed adder cell (height = 13.0 μm , width = 11.2 μm).

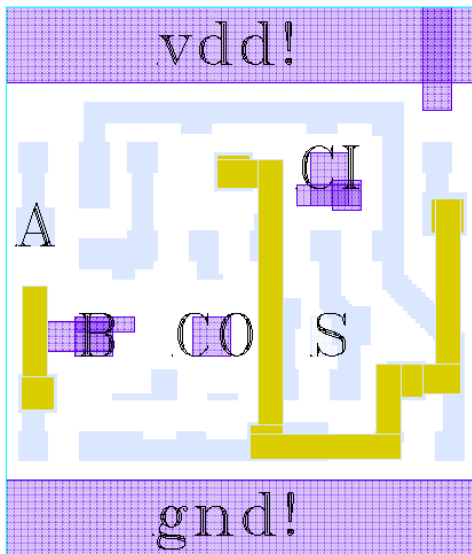


Fig. 6. Abstract view of the proposed adder cell.

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