A High Resolution IF-to-Baseband Continuous-Time ΣΔ Modulator for AM/FM/IBOC Radio Receiver

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Abstract—**A single bit 5th order complex continuous-time sigma-delta IF-to-baseband modulator with integrated mixer for AM/FM/IBOC car radio receiver is presented. The input intermediate frequency (IF) is 10.7MHz and the sampling frequency is 41.7MHz. In AM mode (3kHz BW) the achieved dynamic range is 110dB. In FM mode (200kHz BW) the achieved dynamic range is 88dB. For IBOC (In-Band On-Channel) reception the SFDR is greater than 70dB in a 500kHz BW. The modulator is implemented in a 1P 5M 0.18μm CMOS process with an active area of 3.6 mm^2. It consumes 190mW from a 1.8V supply.**

Keywords— **Analog-digital conversion, Continuous-Time Sigma-Delta modulation, CMOS analog integrated circuits, AM/FM radio receivers, IF mixer.**

I. INTRODUCTION

The current generation of DSP based AM/FM radio receivers (figure 1) rely on analog-to-digital converters (ADC) and digital signal processing to achieve high quality reception. However, analog signal processing and conditioning are still necessary to relax ADC specifications [1, 2]. Two external AM and FM channel filters are used to limit the bandwidth of the IF signal delivered to the ADC, while an automatic gain control (AGC) loop relaxes the ADC's dynamic range (DR) requirements. If the AGC loop, the variable gain amplifier (VGA) and the AM filter are to be eliminated, an ADC with wider dynamic-range and higher linearity is required (figure 2). Such an ADC would simplify the design of the radio receiver, decrease overall power consumption and reduce the cost of the radio receiver.

The development of a high resolution IF-to-baseband ΣΔ ADC (figure 2) is the first step towards a RF-to-baseband ΣΔ ADC. This ADC would enable the development of very versatile "software radio" solutions.

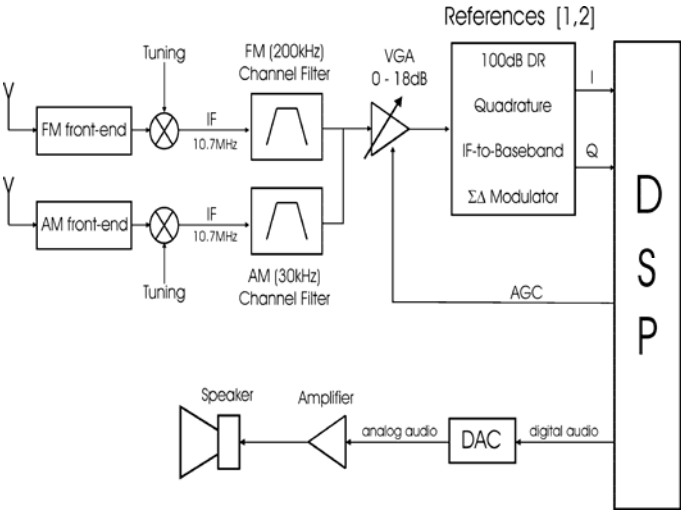

Figure 1. Current generation of DSP based AM/FM radio receivers.

In this article, the design of a high-resolution continuous-time IF-to-baseband ΣΔ modulator with integrated mixer for IF analog-to-digital conversion [3] is presented (figure 2). This modulator combines the anti-aliasing suppression of a continuous-time (CT) loop filter with the low jitter sensitivity of a switched-capacitor (SC) DAC implementation [4].

This paper is organized as follows. Section II presents and discusses state-of-the-art and the new receiver architecture for DSP based AM/FM radio. The chosen ΣΔ modulator architecture is discussed in Section III. Section IV presents the building blocks circuits. In Section V, we show some experimental results. The final comments are given in Section VI.

II. RECEIVER TOPOLOGIES

Figure 1 show the architecture of the current generation of AM/FM radio receivers [1, 2]. Two radio front-ends mix both AM and FM signals to a 10.7MHz IF. The IF signals are filtered by external AM and FM channel filters (30kHz and 200kHz BW) and amplified by a high-linearity/low-noise 0-18dB VGA. The same ADC is used in all operating modes, and has a DR of 100dB for AM and 78dB for FM reception. However, the VGA consumes a few hundred miliwatts, while the AM filter is quite costly. To eliminate both, the modulator's DR must be increased by 18dB (the same DR of the VGA). This implies that the total in-band noise power of the ΣΔ modulator must be reduced by the same factor.

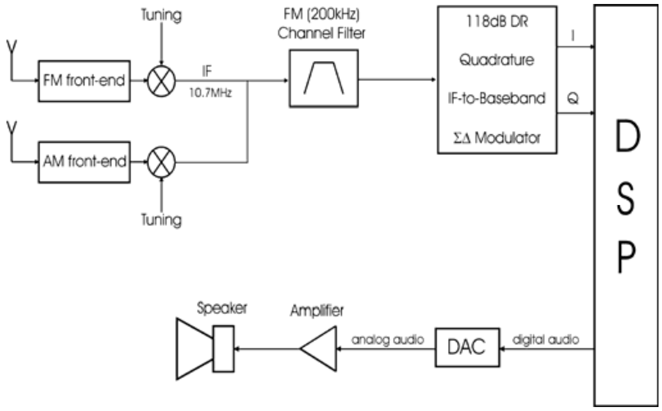

Figure 2. New receiver architecture for AM/FM radio.

Figure 2 shows a receiver with the 118dB ADC. This specification demands an ADC with higher power consumption and larger chip area than the previous implementations [1, 2]. Different front-ends are still needed for AM and FM reception. A VGA is not necessary anymore and a single FM channel filter (200kHz BW) is used. The input of the IF-to-baseband ADC is a single FM channel (figure 3a) or over 20 AM channels (figure 3b). Another channel selection filter (500kHz BW) is necessary for IBOC (In-Band On-Channel) reception. IBOC is a standard for digital audio broadcasting. Digital information is transmitted as sidebands adjacent to the traditional analog FM channels. Figure 3c shows the FM band IBOC frequency spectrum.

The high-resolution IF-to-baseband ADC that enables the receiver topology shown in figure 2 is the subject of the following sections in this article. The next section presents the ΣΔ modulator architecture chosen for this ADC implementation.

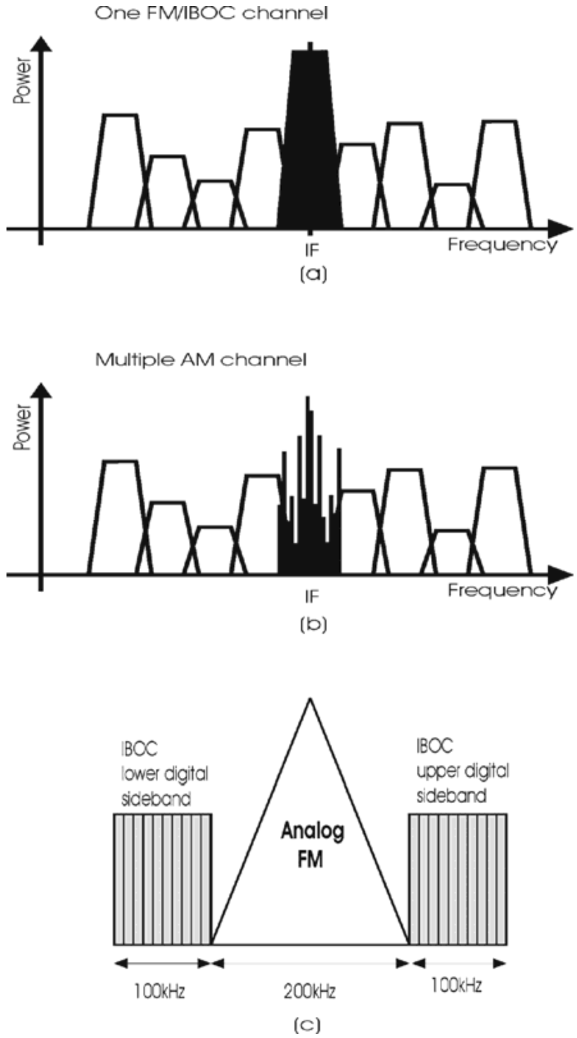

Figure 3. High-resolution IF ADC input spectrum in FM (a) and AM (b) modes. FM band IBOC bandwidth (c).

III. ΣΔ MODULATOR ARCHITECTURE

Figure 4 shows a block diagram of the conversion system with continuous-time (CT) modulators and integrated passive mixers [1], for in-phase (I) and quadrature-phase (Q) demodulation, in a near zero-IF quadrature configuration. The high-resolution IF-to-baseband ADC (figure 2) converts the 10.7 MHz IF analog signal to a digital baseband output around 275KHz. The 10.425 mixing frequency is generated on-chip (divided by 4) from the 41.7MHz sampling frequency provided by an off-chip clock generator.

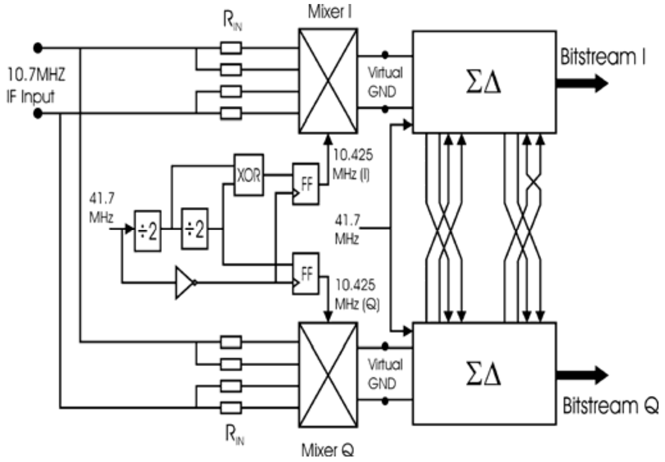

Figure 4. IF-to-baseband conversion system

The in-band quantization noise must be reduced by the same 18dB factor as the thermal noise. A fifth order loop filter with real and complex conjugate poles (figure 5) provides the required quantization noise attenuation inside the signal band [4]. These poles provide additional loop filter gain within the signal bandwidth and introduce notches in the noise shaping of the modulator (figure 6). The complex notches appear across the single-sided signal band for lowest possible in-band quantization noise, the real notches appear on the edge of the signal band for further reduction of the in-band noise and to minimize the quantization noise leakage from the image band to the signal band [4, 5]

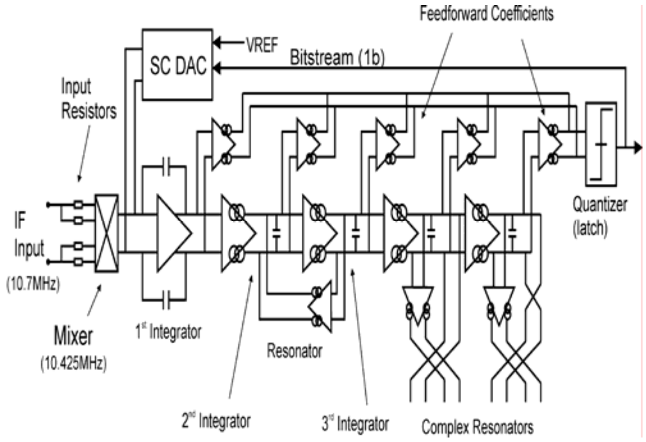

Figure 5. Single bit 5^{th} order CT ΣΔ modulator.

The first integrator is implemented with an opamp and a feedback RC network for maximum linearity. The other integrators are implemented by G_m-C stages. The feedforward and resonator coefficients are implemented by transconductors. In practice the quality factor of the resonators is limited. The resonators' reduced gains and passive components spread cause deviation of the position of the notches. However, the impact of these non-idealities is small since the overall noise in the band of interest is dominated by circuit thermal noise from the input stage and the feedback DAC. A 1 bit quantizer is used together with a 1 bit inherently linear SC DAC.

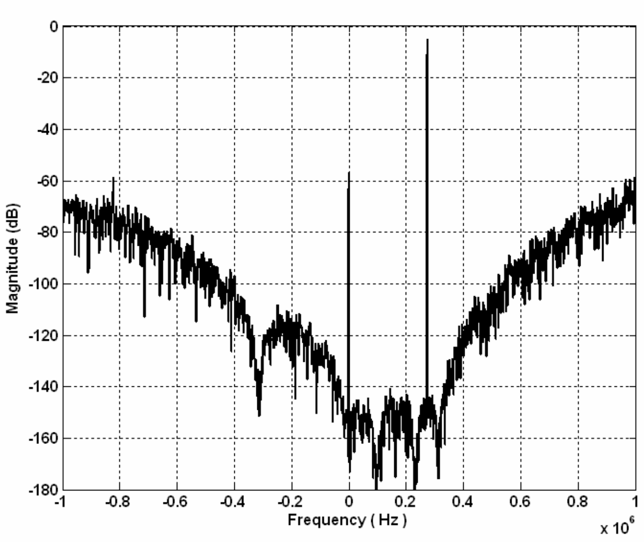

Figure 6. Complex baseband spectrum of the output bitstream (I+jQ) for -6dB input. Simulation – 42000pts.

IV. BUILDING-BLOCK CIRCUITS

The most important circuit building-blocks are the input IF mixers, the loop filter's operational transconductance amplifiers (OTAs), the quantizer and the switched-capacitor (feedback) DAC. They are described in the following sub-sections:

A. *Input IF Mixers*

The passive mixers (Figure 7) are implemented with NMOS switches placed in between the input resistances and the virtual ground input nodes of the CT ΣΔ modulator, which are driven by complementary non-overlapping clock phases [3]. The power consumption of these mixers is negligible and high-linearity is obtained because the on-resistance of the switches is quite small compared to the input resistances. To overcome the effect of double sampling of the quantization noise, each switch is connected to its own input resistors [1]

B. *Loop Filter and Quantizer*

The modulator's first opamp circuit (figure 8) is a single stage telescopic OTA with regulated NMOS and PMOS cascodes to achieve a DC gain of 95 dB (gain boosting). It is biased at relatively high current in order to have a large transconductance (g_m) and low input referred thermal noise. The common-mode control transistors are stacked on top of the PMOS tail current-source and are biased on the triode region.

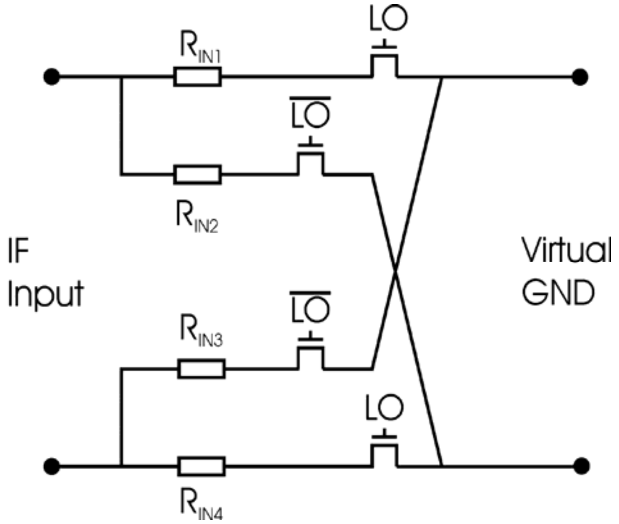

Figure 7. Input IF mixer and input resistors.

The high-order integrators' circuits (figure 9) are implemented as folded cascoded OTAs with a degeneration resistance in between the sources of the input transistors to increase the linear input range and regulated NMOS and PMOS cascodes at the output. Triode biased transistors are employed again on the common-mode control circuitry.

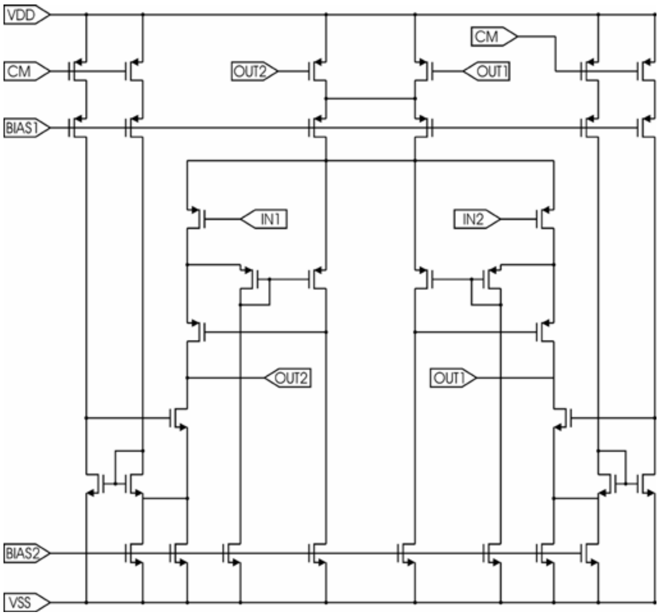

Figure 8. First opamp, a telescopic gain-boosted ota.

NMOS in n-well capacitors are used in this design. These devices have well defined absolute values, good matching and enough linearity. Floating capacitors are implemented with two gate-connected devices, biased to the analog supply (VDDA) via a diode, and the n-well terminals are the floating terminals [7].

The feedforward coefficients are implemented as MOSFET-only transcoductors [8] with current output. They are all connected to the current input summing-node of the single bit quantizer. An internal latch performs the current-to-voltage conversion. The latch output is then fed into an inverter stage, producing true digital output, which is stored in a latch. All quantizer control signals are provided by an internal DLL.

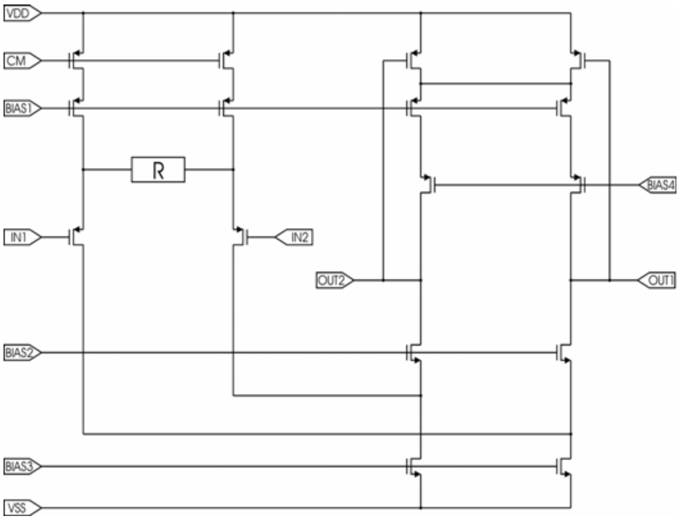

Figure 9. High-order opamps, a resistor degenerated folded-cacoded OTA.

C. *Switched-Capacitor DAC*

In order to achieve better clock jitter immunity, the 1-bit feedback DAC was designed as a switched-capacitor (SC) network. The SC DAC (Figure 10) is implemented with NMOS in n-well floating capacitors and MOS switches [7]. In the first clock phase, the capacitors are charged to ½ V_{REF} by closing switches S1 and S3 (switches S2 open). In the second clock phase, switches S2 are closed (switches S1 and S3 open) and the capacitors are discharged in a data-dependent way by closing switches D or DN. The DAC output current is subtracted from the input current at the virtual ground node and integrated on the capacitors of the first integrator.

To reduce charge injection, S1 opens slightly before S3, and S2 opens slightly before D or DN. To limit peak current through the DAC capacitors and prevent slewing of the first OTA, resistors are placed between the capacitors and the data independent switches S1/S2. Due to the peak currents during the DAC discharge, the virtual ground nodes are very noisy. To achieve the required linearity, the first OTA transconductance should be high enough to cope with these high currents (6mA). A trade-off exists between jitter immunity and the current consumption of the first OTA.

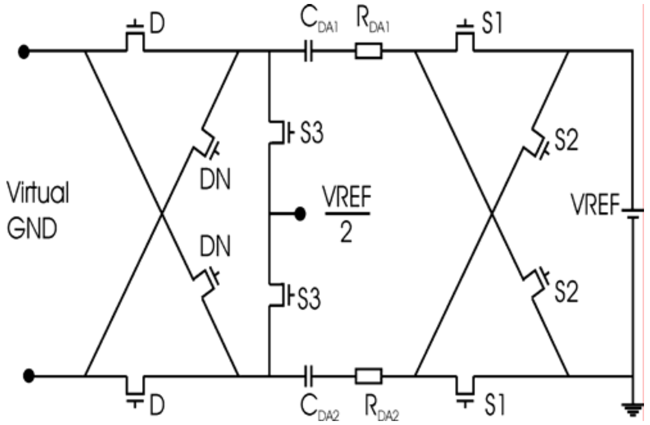

Figure 10. Switched-capacitor (SC) 1b feedback DAC.

V. EXPERIMENTAL RESULTS

The prototype chip in figure 11 is fabricated in a 1P 5M digital 0.18µm CMOS process. The IC includes a clock divider, a DLL, two V_{REF} buffers, and LVDS transmitters. The DLL generates delayed clocks to control the quantizer and the V_{REF} buffers generate 1.6V from a stable external 1.2V reference. The 41.7MHz clock is provided externally. The modulator operates from a 1.8V supply and consumes 190mW (I+Q). The active area is 3.6 mm^2.

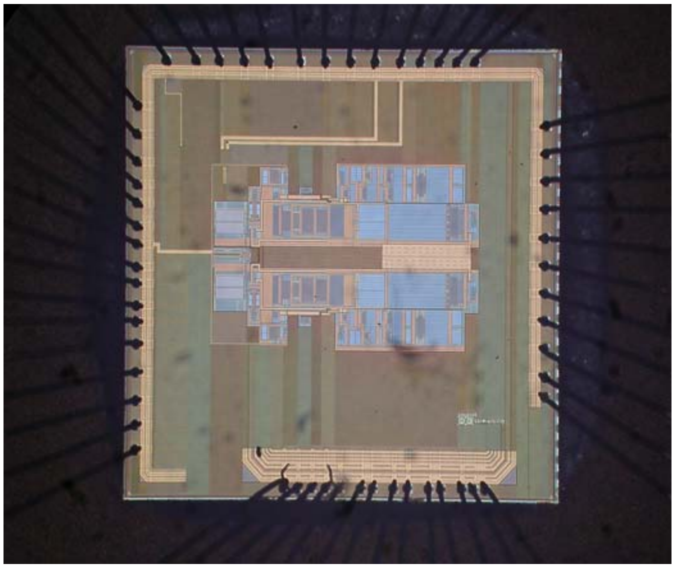

Figure 11. IF ADC 0.18µm CMOS prototype IC micrograph.

The FFT of the complex modulator output bitstream (I+jQ) is shown in figure 12 for an idle input. The baseband spectrum is covered by a higher noise floor and several spurious tones can be seen within the signal band. It is not possible to notice the noise shaping provided by the loop filter integrators and the 320kHz real resonator inside the 175–375kHz signal band (compare with figure 6).

To better understand the reason for the high noise level inside the signal band a measurement with a small DC input voltage was performed. For this experiment the sampling frequency (f_S) is set to be 42MHz.

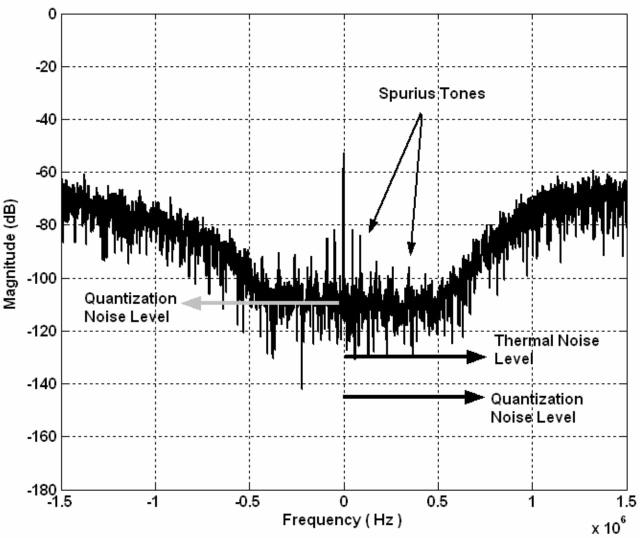

Figure 12. Complex baseband spectrum of the output bitstream (I+jQ) for idle input. Measurement – 42000pts.

The results are shown in figure 13. At frequencies near half of the sampling frequency ($f_S/2$) a single tone at -20dB is present (top plot). The presence of strong tones at high frequencies at the output spectrum of single bit ΣΔ modulators is well known [9].The frequency location of this tone depends on the DC offset applied at the input of the ΣΔ modulator. In this case it is located at 20.8MHz (200KHz below $f_S/2$). The bottom part of figure 13 shows the baseband spectrum for the same DC input. A low frequency tone is clearly located at 400kHz. The frequency of this tone is exactly twice the 200kHz distance between the high frequency tone (20.8MHz) and $f_S/2$ (21MHz).

The down conversion of the high frequencies spectrum (tones and noise floor) to baseband can be explained by two basic mechanisms: modulation of the bitstream by a leakage tone at $f_S/2$ inside the DAC or 2^{nd} harmonic distortion.

In the first situation the multiplication of the bitstream by $f_S/2$ causes the demodulation of the spectrum located at ($f_S/2 – f_X$) to a baseband frequency f_X. That is not the case of our measurements.

In the second situation, asymmetries within the ΣΔ modulator and the sampling at f_S by the quantizer are the cause of the higher noise floor. The 2^{nd} harmonic distortion of a ($f_S/2 – f_X$) tone is located at ($f_S – 2f_X$). Due to the internal sampling (f_S), the ($f_S – 2f_X$) tone is aliased back to a baseband frequency $2f_X$. This mechanism explains the measurements presented in figures 12 and

13. The high noise level and the spurious tones inside the signal band are due to the down conversion of the spectrum near $f_S/2$. As a consequence, the modulator's peak SNR and DR are lower than expected by design and simulations. Even so, the IF-to-baseband ΣΔ modulator presented in this paper is functional. The achieved dynamic range is 10dB better than in previous implementations [1, 2].

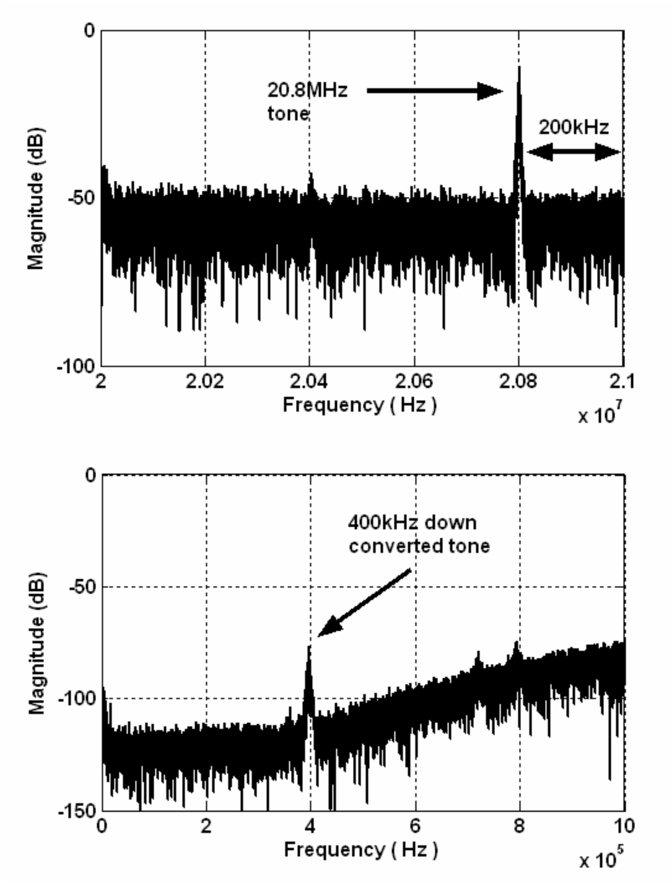

Figure 13. High frequency (near $f_S/2$) spectrum (top). Baseband spectrum (bottom). Output bitstream from the Q modulator (420000pts FFT).

The peak SNR is 102dB in AM mode (3kHz BW) and 80dB in FM mode (200 kHz) and is measured for a full scale (FS) input. The dynamic range (DR) is 110dB and 88dB in AM and FM modes respectively. The SFDR is greater than 70dB for IBOC reception (500kHz BW).

VI. COMMENTS

The high-resolution IF-to-baseband ΣΔ modulator presented in this paper was designed to achieve an 118dB DR in AM mode. This specification demands an ADC with higher power consumption and larger chip area than the previous implementations [1, 2]. Such an ADC would enable the implementation of an AM/FM car radio without an AGC loop and without the external AM channel filter (figure 2). Both cost and system complexity of the receiver would be reduced. Furthermore, the elimination of the VGA also improves the radio's noise figure, increases its sensitivity and reduces its overall power consumption. The prototype chip is functional. It achieves a DR of 110dB in AM mode and 88dB in FM mode.

Due to down conversion of the quantization noise near half of the sampling frequency to baseband, it was not possible to meet the DR design specifications. However, the mechanism that explains the higher noise level inside the signal band is fully understood (Section V).

REFERENCES

[1] Q. Sandifort, L.J. Breems, C. Dijkmans, H. Schuurmans, "IF-to-Digital Converter for FM/AM/IBOC Radio", *ESSCIRC'03.* Proceedings of the 29th European Solid-State Circuit Conference, Sep. 2003, pp. 707–710.

[2] E.J. van der Zwan, K. Philips and C.A.A. Bastiaansen, "A 10.7-MHz IF-to-baseband Sigma Delta A/D conversion system for AM/FM radio receivers", *IEEE J. Solid-State Circuits*, vol. 35, pp. 1810–1819, Dec. 2000.

[3] L.J. Breems, E.J. van der Zwan, E.C. Dijkmans and J.H. Huijsing, "A 1.8mW CMOS ΣΔ Modulator with Integrated Mixer for A/D Conversion of IF Signal", *IEEE J. Solid-State Circuits*, vol. 35, pp. 468–475, Apr. 2000.

[4] K.Philips, "A 4.4mW 76dB Complex ΣΔ ADC for Bluetooth Receivers", Digest of Technical Papers, ISSCC 2003, page(s):64 - 478 vol.1

[5] Jantzi, S.A.; Martin, K.W.; Sedra, A.S., "Quadrature Bandpass ΔΣ Modulation for Digital Radio", *IEEE J. Solid-State Circuits*, vol. 32, pp. 1935–1950, Dec. 1997.

[6] M. Ortmanns, Y. Manoli, and F. Gerfers, "A Continuous-Time Sigma-Delta Modulator with Reduced Jitter Sensitivity", *ESSCIRC'02.* Proceedings of the 28th European Solid-State Circuit Conference, Sep. 2002, pp. 287–290.

[7] R.H.M. van Veldhoven, "A Triple-Mode Continuous-Time ΣΔ Modulator with Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA200/UMTS Receiver", *IEEE J. Solid-State Circuits*, vol. 38, pp. 2069–2076, Dec. 2003.

[8] F. Krummenacher and N. Joehl, "A 4-MHz CMOS Continuous-Time Filter with On-Chip Automatic Tuning", *IEEE J. Solid-State Circuits*, vol. 23, pp. 750–758, Jun. 19983.

[9] S. Norsworthy, R. Schreier and G. Temes, "Delta-Sigma Data Converters – Theory, Design and Simulation", IEEE Press, 1997.