Lithographic Alignment Offset Compensation for Substrate Transfer Processes

H.W. van Zeijl, J. Su, J, Slabbekoorn and F. G. C. Bijnen.

***Abstract*—Novel technologies like substrate transfer technology can introduce severe topography on otherwise flat silicon wafers. Since optical lithography is usually performed on ultra flat wafers, the alignment system is not optimized for high topography wafers. In this work, an experimental procedure is presented to measure the alignment offset of an ASML PAS5000/50 waferstepper on high topography wafers. Furthermore, a model of the alignment system is developed that describes the experimental results. The fitted model parameters can be used to further optimize the alignment performance on high topography wafers.**

***Index Terms*—Alignment system, overlay, substrate transfer technology, waferstepper.**

I. Introduction

Lithography is one of the key enabling process steps in the fabrication of integrated circuits and micro electronic mechanical systems (MEMS), and the ongoing miniaturization has led to increased overlay and resolution requirements. Today, wafersteppers and waferscanners are the industry lithographic workhorses that can meet these requirements routinely in a production environment. Advanced lithography requires ultra flat substrates since the focal depth of the lithographic system is limited (< 1 μm). Therefore, the alignment systems are usually not optimized to cope with large focal offsets and non flat wafers.

The drive to increase the performance of microelectronic and MEMS devices had led to the introduction of novel process technologies in the production environment. Not always, these novel technologies are fully compatible with the lithographic processes. Novel process steps, like substrate transfer technology [1], may introduce severe wafer un-flatness or a large focal offset between alignment marker and image plane which can affect the alignment accuracy. In this work, we characterized the performance of the alignment system of an ASML PAS5000/50 waferstepper on wafers with a large topography and focus offset between alignment marker and image plane.

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H. W. van Zeijl, J. Su and J. Slabbekoorn are with the Delft Institute of Microelectronics and Submicrontechnology (DIMES) / Delft University of Technology, Delft, The Netherlands. Phone: +31 152 784949, fax: +31 152 22163, e-mail: henkz@dimes.tudelft.nl.

F. G. C. Bijnen is with ASML Special Applications, De Run 6501, 5504 DR Veldhoven, The Netherlands.

II. Overlay

In semiconductor lithography the pattern overlay is the displacement between the patterns of one process level to those of another after they have been lithographically aligned to each other. The routine characterization of overlay errors is extremely useful to ensure that the performance of a waferstepper is always optimal. Therefore, overlay to reference grid measurements is a standard overlay test procedure available, on most wafersteppers.

The measurement principle is based on the capabilities of a waferstepper to align very precise on dedicated targets on the wafer, so-called alignment markers. With two or more of these targets on the wafer, often referred to as primary alignment markers, an X-Y coordinate system is established on the wafer. The position of other alignment markers on the wafer is measured by the waferstepper alignment system using the X-Y coordinate system as a reference, therefore the coordinate system is often referred to as the reference grid.

The overlay performance of the ASML PAS5000/50 waferstepper used in the present work is measured according to the overlay test procedure for this type of waferstepper. This procedure and the determined performance of the stepper are described in the following. On a 100 mm wafer two primary alignment markers are etched in the silicon. These primary alignment markers are used to establish the wafer coordinate system or reference grid over the wafer as shown in fig.1.

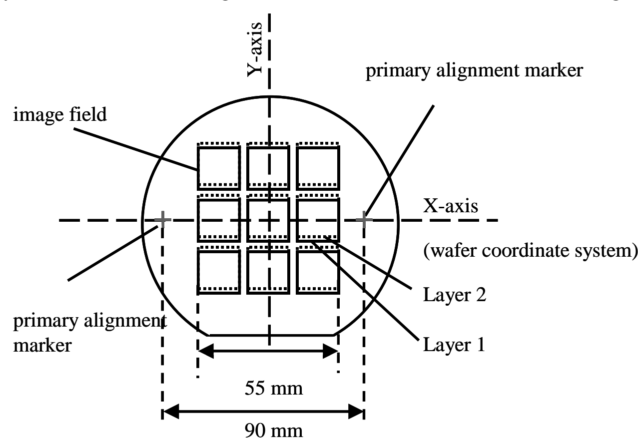


Fig. 1. Wafer layout of the standard overlay test pattern on an ASML PAS5000/50 waferstepper. Position measurements on two primary markers are used to define the reference grid. Layer 1 is exposed using the reference grid while layer 2 is exposed with a programmed offset.

After coating with photoresist, 9 image fields are exposed using a reticle with an array of 11 x 11 markers in the 15 x 15 mm^2 image field. This defines layer 1. Next, the wafer is reloaded and using the same reticle a second layer, layer 2, is exposed with a programmed shift. A wafer reload means that the wafer coordinate system is established again by the alignment on the primary alignment markers. Consequently, the reference grid of layer 1 differs slightly from the reference grid of layer 2.

The wafer is developed and reveals the images of the markers in the photoresist. Then it is again loaded in the waferstepper to measure the positions of all the markers in the image fields relative to the wafer coordinate system. Two different overlay calculations are now possible: firstly layer 1 to layer 2 and secondly layer 1 (or layer 2) to reference grid.

The relative overlay of layer 1 to layer 2 is the measured difference in the positions of corresponding markers in the respective layers corrected for the programmed shift. For the system used in the present work, a deviation of 28 nm (3σ = 38 nm) in the X direction and 18 nm (3σ = 42 nm) in the Y direction is measured. These numbers reflect the accuracy and reproducibility of the XY-stage and the alignment system.

As discussed, the alignment is based on measurement of the position of primary alignment markers. In conventional front-side wafer lithography, these markers are embedded in an optically flat substrate. Furthermore, the alignment markers and the device layers are on the same level. However, substrate transfer also affect the areas that carries the alignment markers, this has consequences for the alignment accuracy and therefore also for the overlay accuracy.

III. Substrate Transfer Technology

Dual side processing is one of the process steps that can improve the device performance, for example, back-side wafer collector contacts reduce the collector resistance [2] or backside MOS gates [3] reduce the off-current. The back-side of the device becomes accessible for processing if the device-layer is flipped over onto a new substrate; the so called Substrate Transfer Technology. The substrate transfer process, together with the integration of alignment markers in the process is given in fig. 2.

As in conventional front-side wafer processing, the alignment marker for the substrate transfer process is made on the front-side wafer surface (fig. 2a). The front-side part of the devices is processed on an SOI wafer and the front-side wafer interconnect metal remains on the alignment marker to enhance its reflectivity (fig. 2b). After wafer bonding with glue, the substrate silicon is removed, for example by a wet chemical etch using the buried oxide as an etch stop (fig. 2c). The alignment markers are buried under the device silicon, and for thin transparent epitaxial layers, alignment through the silicon is possible. However, when during the further processing an optical opaque film like metal is deposited, optical access to the alignment marker must be re-established by a non-critical silicon etch selective to the device dielectric as given in fig. 2d.

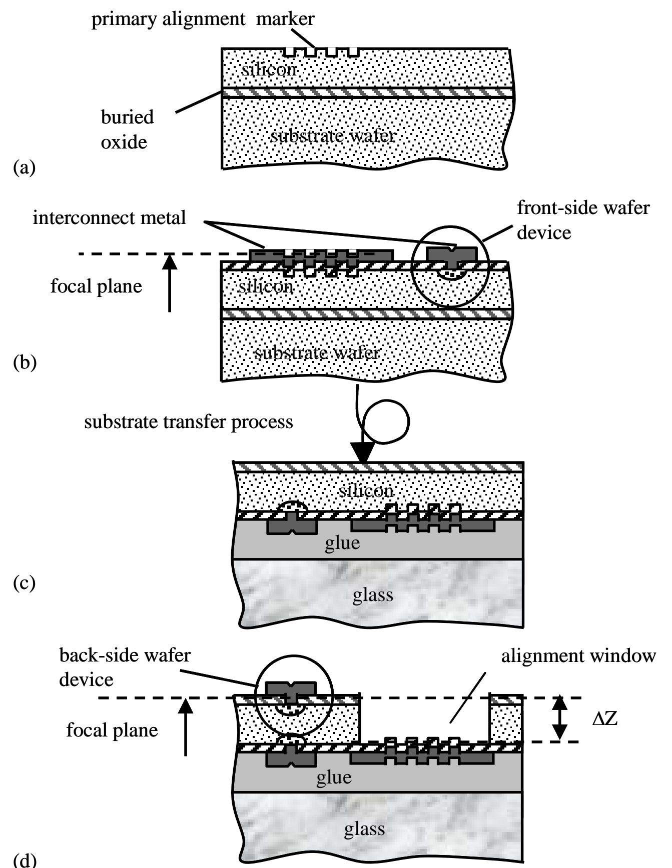


Fig. 2. Substrate transfer process overview, the process flow is explained in the text.

After substrate transfer, the back-side wafer alignment marker differs on three major points compared with the front-side wafer alignment marker:

- the levels of the device layer and the alignment markers does not necessarily coincide,
- the alignment marker is mirrored after substrate transfer,
- the tilt of the alignment marker is changed, this can introduce an alignment offset.

The first issue is a direct consequence of dual side processing. Before the substrate is transferred, the alignment markers and front-side wafer device layers are on the same level. However, after substrate transfer, the alignment markers are on the front-side wafer level while further lithographic processing is performed on the back-side wafer level. Consequently, the level of the alignment markers and back-side wafer processing are shifted in the vertical direction (Z-direction) over a distance determined by the thickness of the transferred film (ΔZ). Generally, for alignment and exposure, the wafer surface is used as a reference for the focus system, but after substrate transfer, the alignment marker is not necessarily in focus (fig. 2d). Whether this has consequences for the functionality of an alignment system is discussed in section IV.

Secondly, the back-side wafer image is mirrored with respect to the front-side wafer image, consequently the alignment markers are mirrored. But using mirror symmetric alignment markers [4], the back-side wafer lithography is virtually similar to the front-side wafer lithography.

Thirdly, as the device layer is transferred onto a new substrate, the topography of the new substrate is most likely different. The thickness non-uniformity of the glue determining the topography after substrate transfer is shown in fig. 3, substrate transfer can result in severe non-flat wafers. Consequently the tilt of the alignment marker after substrate transfer is different compared with the tilt before substrate transfer (fig. 4). The effect of marker tilt on the alignment accuracy is discussed in the next section .

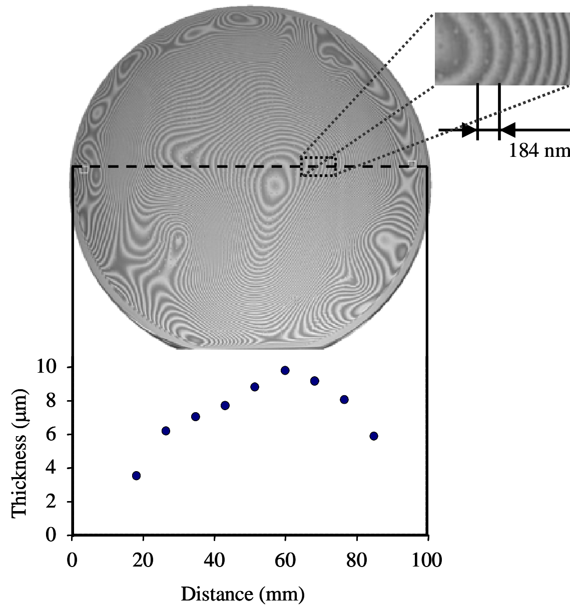


Fig. 3. Optical fringe pattern that indicates the glue thickness after substrate transfer. Each fringe represents a thickness difference of 184 nm. The glue thickness is measured across the wafer, on locations given by the dashed line and shown in the graph.

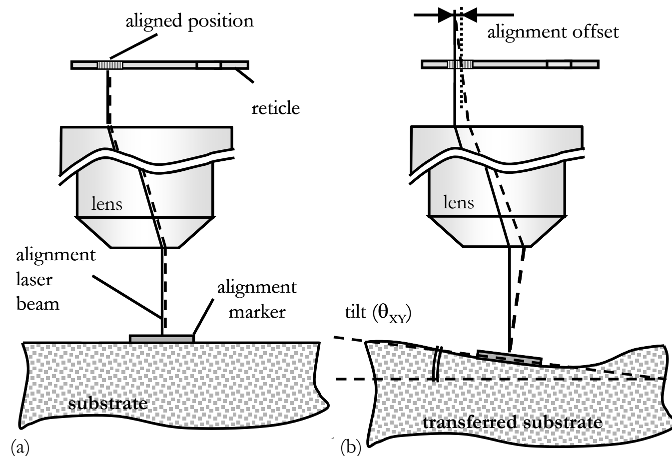


Fig. 4. The influence of wafer topography on the tilt of an alignment marker in (a) the substrate is optically flat, in (b) the alignment marker is tilted.

IV. Waferstepper alignment systems

Several categories of alignment detection schemes are used today. The most widely used are either based on contrast detection (bright field/dark field) or phase grating diffraction schemes.

A. *Dark field / bright field alignment systems*

The principle of bright field /dark field alignment systems is based on optical pattern recognition. A specifically designed alignment marker is illuminated by a light source, while a CCD camera captures the reflected light through the waferstepper lens. The focal depth of today's high NA imaging lenses is limited to a fraction of a micron. Consequently, the focal depth of a TTL alignment system is also limited which reduce the alignment accuracy after substrate transfer.

The waferstepper lens is focused on the device layer by a very precise auto focus system. However if a focus offset between the alignment marker and the device layer exists, the alignment marker is out of focus, which can hamper an accurate alignment. Re-focus on the alignment target is possible but the Z-travel of the focusing system may be limited. Furthermore a large Z-displacement of the wafer stage can introduce an unknown shift in the XY-plane. Moreover, a focus search is time consuming and limits the throughput of the exposure tool.

B. *The diffraction grating based alignment system*

The diffraction grating based alignment systems analyses the phase information [5]. The alignment marker, a diffraction grating etched in the wafer surface, is illuminated by a coherent monochromatic light source, for example a HeNe laser (fig. 5a). This alignment marker consists of 4 gratings, two gratings for alignment in the X-direction and two gratings for alignment in the Y-direction, the layout of the ASML alignment marker is seen in fig. 5b. A spatial filter blocks the 0, 2nd and higher orders of diffraction. The 1st and -1st order diffraction patterns are captured by the lens of the waferstepper and interfere in the focal plane at the reticle level (fig. 5c).

Each grating produces an interference pattern that illuminates a corresponding grating on the reticle. During an alignment scan the wafer is moved in X or Y direction. The interference pattern will also move and the light transmitted by the corresponding X or Y grating on the reticle is therefore a function of wafer displacement. This intensity-displacement relationship is used to align the wafer to the reticle. Although the reflected 0-order beam is blocked, the measured position of the alignment marker can be considered as the intersection of the hypothetical 0-order beam path with the reticle focal plane.

The starting point for this hypothetical 0-order beam is the center point of the alignment marker. The pitch of the interference pattern is only determined by the angle between the +1st order and -1st order diffracted beams. A variation in focus of ΔZ at wafer level ($\Delta Z'$ at reticle level) will not change

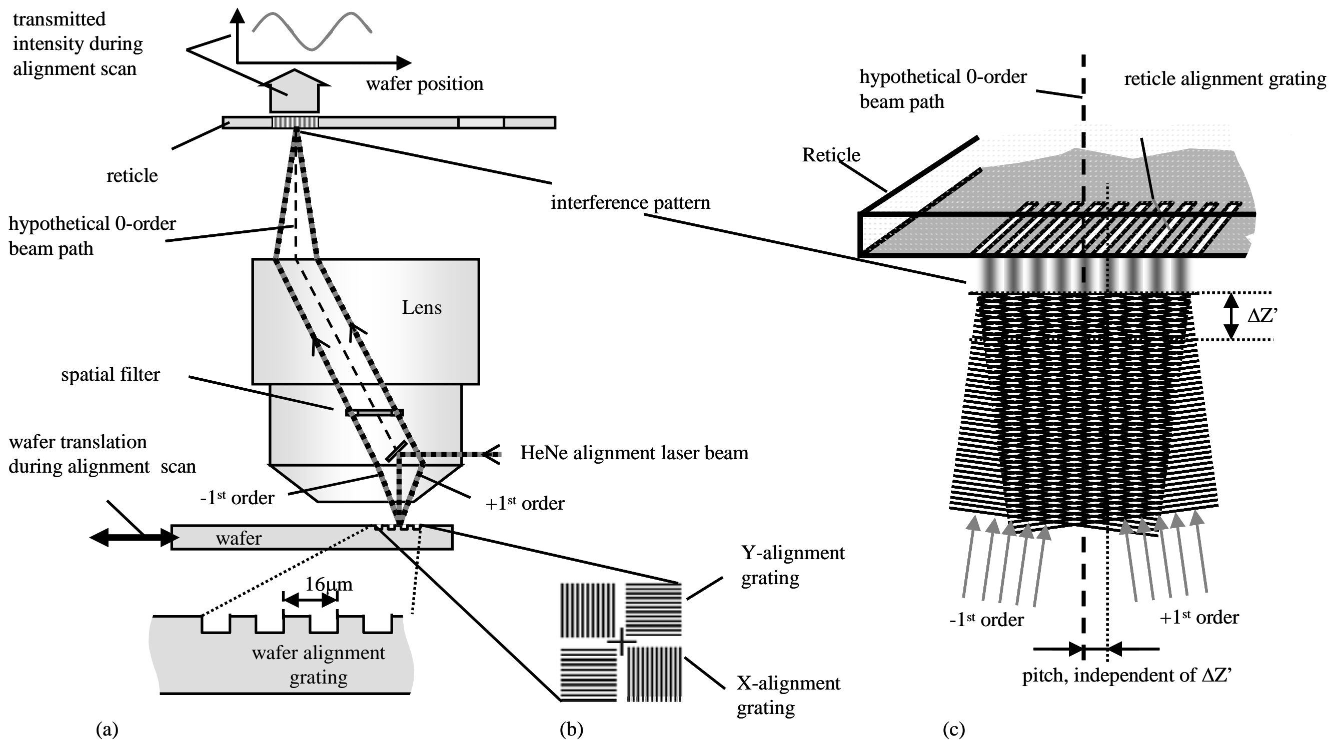


Fig. 5. Operating principle of a diffraction grating alignment system (a) as implemented in the ASML PAS5000/50. In (b) the layout of a standard ASML alignment marker is given. The reflected +1st and -1st order forms an interference pattern in the reticle plane

this angle. Thus, the pitch of the diffraction pattern at the reticle plane is insensitive for focus variations. As a result, a diffraction based alignment system is, in first approximation, insensitive for a focus. The functionality of the alignment system has been proven for a focus offset of 525 μm (the wafer thickness of a 100 mm wafer) [6].

V. Experimental

The silicon wafers used for device fabrication are usually optically flat. For advanced lithography, throughout the processing, a die scale flatness of 250 nm or better (peak to valley) is preferred [7]. However, as a relative thin device layer (1-5 μm) is transferred onto a new substrate, the topography of the new substrate will be transferred to the device layer. Furthermore, when an intermediate layer, like glue is used, non-uniformities in the intermediate layer will add up to the substrate topography. This will deteriorate the die scale flatness and affects the tilt of the alignment markers.

Because wafers are usually optically flat, little is known about the response of the ASML PAS5000/50 alignment system on a tilted alignment marker. Therefore, the measurement offset as a function of marker tilt is determined experimentally. The experiment is based on the standard overlay test procedure (see fig. 1). Layer 1 is exposed and etched in the silicon, next all the marker positions in the fields of layer 1 are measured and the XY-coordinates are stored in an array layer1. On the back side of the wafer, approximately in the wafer center, a small piece (1 x 1 mm^2) of thin plastic foil is attached to create an intended wafer topography.

The wafer is reloaded in the waferstepper and the wafer flatness is measured. A procedure to measure the wafer flatness, is available on the ASML PAS5000/50 waferstepper for engineering and maintenance purposes. The principle of the test procedure is as follows: over an array of XY-stage positions the wafer height is measured using the waferstepper focus system. The resulting data set represents a height map of the wafer with a resolution better than 100 nm in the Z-direction. Such a wafer flatness measurement in the waferstepper is a good reference since the XY-wafer stage that carries the wafer is optically flat and the conditions for wafer height measurement are similar to that of the overlay measurement.

The measured wafer flatness in the center of the wafer is given in fig. 6. A peak to valley value of about 6 μm is measured, a value that also occurs in substrate transfer (fig. 3). From this measurement, the tilt of the alignment markers in the image field is calculated in X- and Y-direction.

After the wafer flatness measurement, the positions of the alignment markers in layer 1 are measured again and stored in an array layer1'. The focus of the lens remains constant during the overlay measurements. A wafer map with the differences of both measurements, layer1' - layer1 is given in fig. 7. It clearly shows the influence of wafer topography on the measured marker positions. It is assumed that the wafer is not distorted in the XY-plane thus the differences in layer1 and layer1' are solely caused by the wafer topography.

Based on the lens design, a relation can be derived between the measurement offset in X and Y direction ($\Delta_{X,Y}$) and the substrate related parameters, marker tilt ($\theta_{X,Y}$) and wafer topography (ΔZ). In the focal plane, any beam that departs

from the alignment marker will be focused in the image plane. Hence an alignment tilt does not contribute to the measurement offset if $\Delta Z = 0$ (fig. 8a).

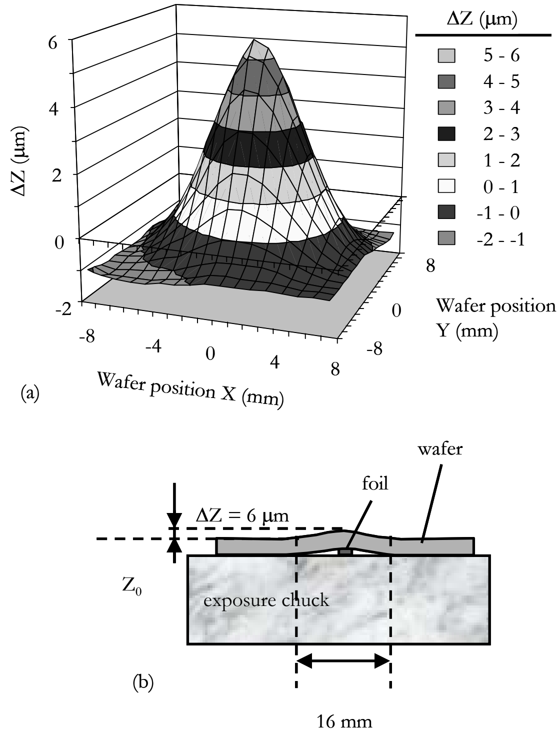


Fig. 6. Measured wafer height (ΔZ) versus wafer position (a). in (b) a schematic cross section is given of an intentionally distorted wafer, clamped on an optically flat exposure chuck in the waferstepper.

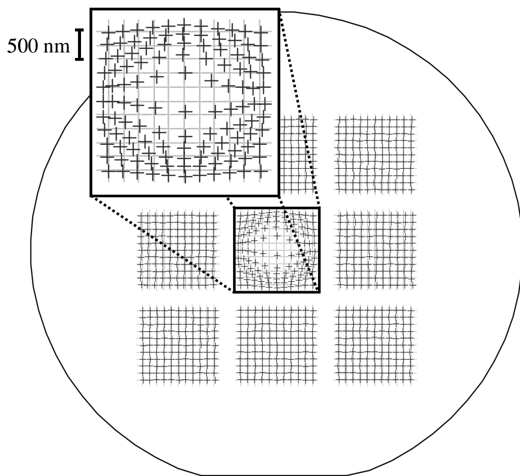
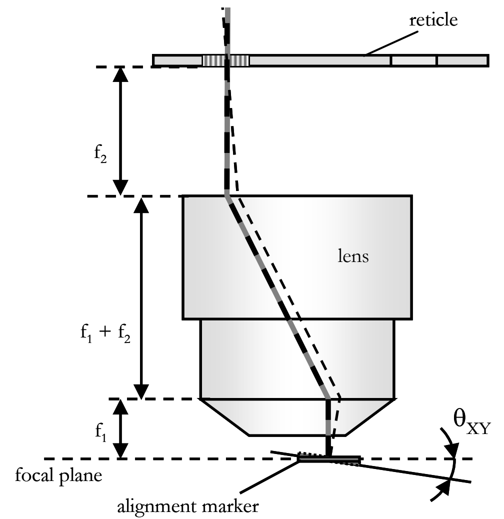


Fig. 7. Wafermap of the overlay of layer 1' to layer 12, measured on a 100 mm wafer with an intentional topography of 6 mm in the wafer centre. The die size is 15 x 15 mm[2], the scale of the deviations is indicated in the graph.

However, this is not the case for a de-focused alignment marker (fig. 8b). Because all the variations (ΔZ, $\Delta_{X,Y}$) are typically a factor 10^4 smaller compared with the physical dimensions of the alignment system (μm vs. cm) a linear relation is assumed:

$$\Delta_{X,Y} = a \cdot (\Delta Z + Z_0) \cdot \theta_{X,Y} \qquad (1)$$

Where: a is a proportionality factor that depends on the lens design,



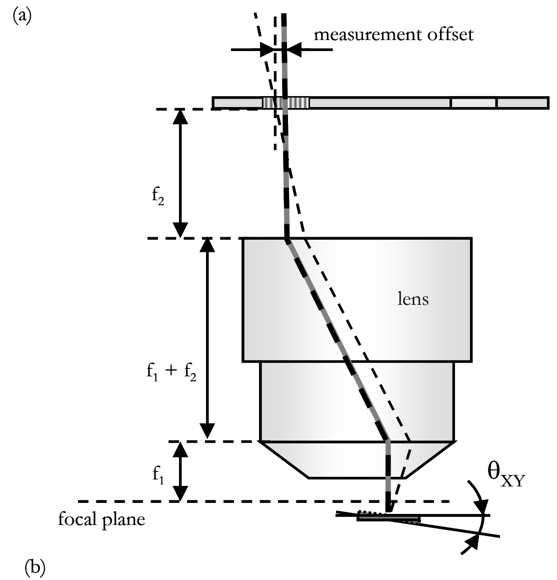


Fig. 8. Schematic overview of the alignment beam paths through the lens. In (a), the beam paths are shown of a planar and a tilted alignment marker, both in focus. In (b), the beam paths are drawn for a planar and tilted marker, both out of focus.

Z0 is the difference in focus of the alignment system (red light) and the imaging system (blue light).

Furthermore, a tilt on the incident alignment beam also causes a shift in the measured marker position (see fig. 9):

$$\Delta_{X,Y} = \beta_{X,Y} \cdot \Delta Z \qquad (2)$$

Where: $\beta_{X,Y}$ is the tilt of the incident beam in the X or Y direction.

Because the effect of alignment marker tilt and tilt of the incident laser beam are independent, the total offset is a linear superposition:

$$\Delta_{X,Y} = a \cdot (\Delta Z + Z_0) \cdot \theta_{X,Y} + \beta_{X,Y} \cdot \Delta Z + \delta_{X,Y} \qquad (3)$$

Where: $\delta_{X,Y}$ is a parameter to model the error in the reference grid of layer1 relative to layer1' caused by an alignment error on the primary markers.

This model (equation 3) is fitted to the measured difference layer1' - layer1 and the wafer topography parameters ΔZ and $\Delta_{X,Y}$, the results are given in table I.

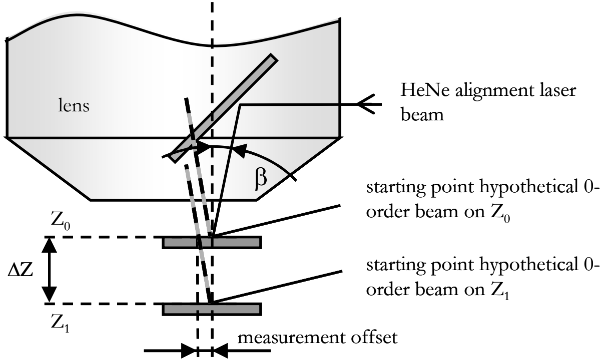


Fig. 9. Effect of tilt in the incident alignment beam on the aligned position on different focus levels.

Table I. Parameters of equation 3, fitted to $\Delta_{X,Y}$, ΔZ and the derived $\theta_{X,Y}$.

	X	Y
a (rad^{-1})	-10.71	-14.17
Z_0 (μm)	19.04	17.96
β (rad)	-0.00693	0.00629
δ (μm)	-0.00462	-0.0368
Sum of squares (μm^2)	0.0535	0.0843

VI. DISCUSSION

The substrate transfer process can introduce severe wafer topography and an alignment focus offset. Both can affect the alignment accuracy as explained in the previous sections. Using the model described in equation 3, the effect of the substrate topography in terms of marker tilt ($\theta_{X,Y}$) and alignment focus offset (ΔZ) on the alignment accuracy can be calculated. The fitted model (equation 3 and table I) can also be used to derive substrate and /or process specifications in terms of ΔZ and $\theta_{X,Y}$ if a given alignment accuracy is required. The relation between alignment offset, ΔZ and $\theta_{X,Y}$ is shown in fig. 10. Furthermore, the derived values for Z_0 and β are very useful to adjust the alignment to further reduce the influence of Z and θ variations.

Large ΔZ values may not only occur after substrate transfer. Also in the processing of MEMS devices often thick film like sacrificial layers or thick photoresist may result in a large ΔZ during processing. It is expected that the alignment accuracy on these layers will also be improved with a Z_0 and β optimized alignment system.

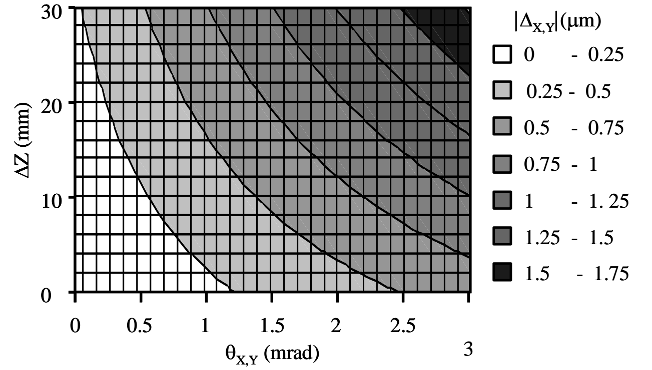


Fig. 10. Alignment offset ($\Delta_{X,Y}$) , for different values focus offsets (ΔZ) and alignment marker tilt ($\theta_{X,Y}$).) $\Delta_{X,Y}$ is calculated using equation 3, and the data from table I.

VII. CONCLUSIONS

Substrate transfer technology can alter the wafer topography. Consequently tilt and focal offset on the primary alignment markers after substrate transfer is different compared with the tilt and focal offset before substrate transfer. This will affect the before- to after substrate transfer overlay. Although a phase grating alignment system is virtually insensitive for focus offsets, the combined effect of focus offset and alignment marker tilt can affect the alignment accuracy. Therefore, to assess the alignment offset of the alignment system of an ASML PAS5000/50 waferstepper on high topography wafers, an experimental method is developed. These experimental results are described with a model of the alignment system. The model can be used to further optimize the alignment system for alignment, not only on substrate transferred wafers, but also on substrates where the topography and / or thick optical films causes a large focus offset between the image plane and the alignment markers.

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