

High Slew Rate Configurable Class AB Fully Differential Operational Transconductance Amplifier for Switched Capacitor Circuit Applications

Renato Rimolo-Donadio, Alexander Mora-Sanchez, and Dietmar Schroeder.

Abstract—In this paper, a configurable dynamically-biased class AB operational transconductance amplifier (OTA) for switched-capacitor (SC) circuit applications, based on the utilization of the flipped voltage follower (FVF), is presented. The proposed OTA offers high slew rate, low power consumption, and its speed can be configured to work in a unitary-gain bandwidth (UGBW) range from about 2MHz up to 50MHz. The amplifier has been designed to operate at 3.3V using a 0.35μm CMOS technology. Post-layout simulation results show that the OTA is suitable for the design of low-power and high-slew rate SC circuit applications, offering better performance in those aspects with respect to classical OTA architectures.

Index Terms—dynamic-biasing, configurable amplifier, fully differential, high slew rate, operational transconductance amplifier.

I. INTRODUCTION

OTA non-ideal parameters must be taken into consideration when designing SC-circuit stages since they detrimentally impact their performance [1]. For a fast and complete charge transfer the OTA must provide high open-loop gain, high slew rate (SR), and large bandwidth. The high slew rate and bandwidth ensure a small settling time, whereas the high gain improves the settling accuracy [2]. A high slew rate also helps to avoid distortions introduced when part of the settling of the amplifier is nonlinear.

On the other hand, low-power small-area design techniques are mandatory for the design of SC-circuits in modern portable applications. Dynamic biasing schemes [3] are capable of conciliating the gain, bandwidth and slew rate requirements with the low-power small-area characteristics.

This work presents a configurable CMOS OTA with dynamic biasing, featuring high slew rate and low-power

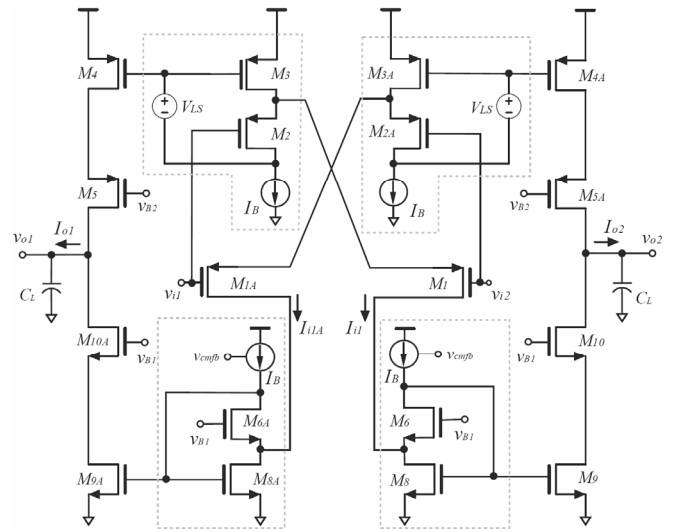


Fig. 1. Simplified schematic of the proposed fully differential OTA. Dashed blocks indicate the location of the FVFs.

consumption. In particular, it has been designed for the SC-based single amplifier sigma-delta ($\Sigma\Delta$) modulators reported in [4]. The configurability of the proposed amplifier allows the further optimization of the power consumption according to the bandwidth requirements of the target application.

This paper is organized as follows. Section II discusses the OTA architecture and its main features. The amplifier physical design in a CMOS 0.35μm process is addressed in Section III. Section IV presents main results at post-layout simulation level, being evaluated against a classical two-stage class A/AB OTA available in our custom design library. Finally, the conclusions are summarized in Section V.

II. OTA ARCHITECTURE

The proposed OTA, whose simplified schematic is seen in Fig. 1, is based on the class AB architecture presented by Peluso *et al.* in [5], but it incorporates some important modifications. First, the proposed solution is designed to work at 3.3V and, therefore, it requires the incorporation of voltage level shifters V_{LS} to bias properly the input transistors.

R. Rimolo-Donadio is graduate student at the Nanoelectronics Institute, Hamburg University of Technology, D-21073 Hamburg, Germany, on leave from the Costa Rica Institute of Technology (Phone: 0049-40-428783727; fax: 0049-40-428782877; e-mail: renato.rimolo@tu-harburg.de).

A. Mora-Sanchez and D. Schroeder are with the Nanoelectronics Institute, Hamburg University of Technology, D-21073 Hamburg, Germany (e-mail: rodrigo.mora@tu-harburg.de, d-schroeder@tu-harburg.de).

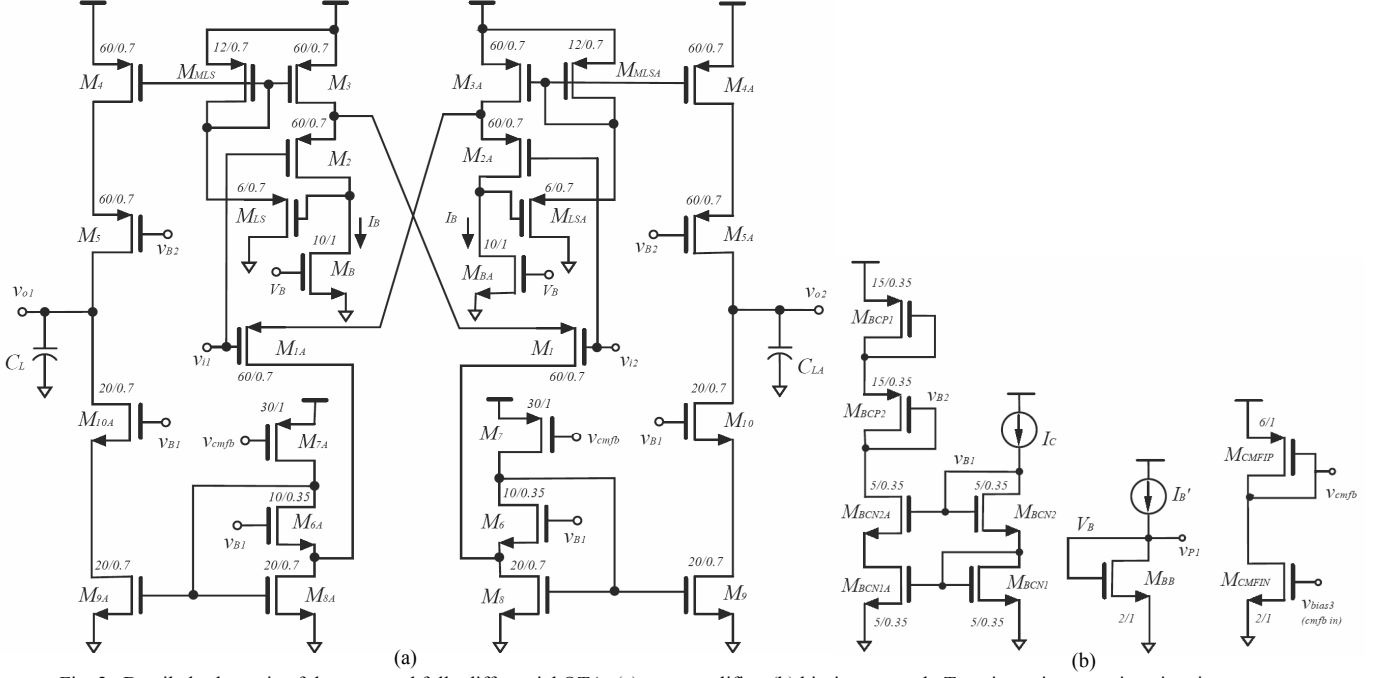


Fig. 2. Detailed schematic of the proposed fully differential OTA: (a) core amplifier; (b) biasing network. Transistor sizes are given in micrometers.

Besides, the amplifier includes output cascode transistors in order to achieve enough gain in a single-stage, and it uses a single SC common mode feedback network (CMFB) [6] applied to the NMOS low-voltage current mirror references.

A. Core Amplifier

The amplifier relies on a symmetrical input differential pair which exploits the high current source capability of the flipped voltage followers (FVF) [7], highlighted in Fig. 1. The FVFs connected at the input (transistors M_{2-2A} , M_{3-3A}) act as level shifters and provide the adaptive biasing: low quiescent current at zero differential input, and high current source capability proportional to the differential input signal excursion [8]. Regarding SC-circuits, this means that the OTA biasing currents will be regulated to provide a high current at the beginning of the charge transfer phase (when a large differential input voltage might be present), increasing the speed of the amplifier, and then, the current starts to decrease gradually as the charge is transferred (and the differential input voltage diminishes), increasing the gain.

The static currents through the input transistors are defined by the biasing current I_B :

$$I_{i1A} = I_{i1} \approx I_B, \quad v_{id} = v_{i1} - v_{i2} \approx 0. \quad (1)$$

For large v_{id} , one of these currents starts to increase and the other to decrease, providing the class AB operation according to:

$$I_{i1} \approx \frac{\beta_1}{2} \left(\sqrt{\frac{2I_B}{\beta_1}} + v_{id} \right)^2, \quad I_{i1A} < I_B, \quad v_{id} > 0, \quad (2)$$

$$I_{i1A} \approx \frac{\beta_{1A}}{2} \left(\sqrt{\frac{2I_B}{\beta_{1A}}} - v_{id} \right)^2, \quad I_{i1} < I_B, \quad v_{id} < 0. \quad (3)$$

The low-voltage current mirrors (transistors M_{6-6A} , M_{8-8A}) are used to replicate the current through the input transistors. At the same time, they provide the common mode (CM) input to control the CM level. The output single ended currents are given by the mirrored current from transistors M_{3-3A} and M_{8-8A} . Each current is sourced by one half of the circuit and sunk by the other half. Assuming that the circuit is symmetric and the transistors are working in saturation, these currents can be written as:

$$I_{o1} \approx -I_{o2} \approx 2B\sqrt{2I_B\beta_1}v_{id} \approx 2Bg_{m1}v_{id}, \quad v_{id} \approx 0, \quad (4)$$

$$I_{o1} \approx -I_{o2} \approx B \left(\frac{\beta_1}{2} \left(\sqrt{\frac{2I_B}{\beta_1}} + v_{id} \right)^2 \right), \quad v_{id} > 0, \quad (5)$$

$$-I_{o1} \approx I_{o2} \approx B \left(\frac{\beta_1}{2} \left(\sqrt{\frac{2I_B}{\beta_1}} - v_{id} \right)^2 \right), \quad v_{id} < 0. \quad (6)$$

where B is the output current mirror factor, defined as 1 in this case. Then, the output currents change linearly for small input voltage values and start increasing quadratically for large input signal excursions. Under static conditions the small signal open-loop gain and the unitary gain bandwidth are given approximately by:

$$A_{oldc} \approx 2g_{m1} \frac{g_{m5}}{g_{o4}g_{o5}}, \quad (7)$$

$$UGBW \approx \frac{2Bg_{m1}}{C_L}. \quad (8)$$

The voltage V_{LS} allows to have a bias source-gate voltage for the input transistors (M_{1-1A} , M_{2-2A}) very close to their threshold voltage. This condition is necessary to achieve a low

quiescent current (with a value near to I_B) when working at supply voltages in the order of 3V. The actual implementation of this “high-voltage” version of the FVF [9] is included in the detailed OTA schematic in Fig. 2 (transistors M_{LS-LSA} , $M_{MLS-MLSA}$). There, V_{LS} is equal to the source-gate voltage of the transistors M_{LS-LSA} . Note that at low values of I_B the transistors might become biased slightly in weak inversion, which results beneficial to achieve higher g_m/I ratios.

B. Biasing Network

The OTA basing network in Fig. 2(b) consist of a cascode current mirror to generate the reference voltages v_{B1} and v_{B2} , and a single current mirror to provide the reference current I_B and the CMFB voltage reference v_{p1} . The additional inversion introduced in the CM path (transistors M_{CMFIP} and M_{CMFIN}) is required in order to have a CM negative feedback-loop.

C. Configurability

Since the single amplifier $\Sigma\Delta$ -modulators are designed to be used in diverse biomedical applications [4] with different bandwidth requirements, the configurability is a key feature of the OTA. By varying both the bias current I_B' in a range from $0,2\mu A$ up to $10\mu A$ and the bias current I_C from $2\mu A$ up to $12\mu A$, the speed of the OTA can be adjusted to provide a UGBW from about 2MHz up to 50MHz, respectively. The current I_B is associated with a range from $1\mu A$ to $50\mu A$ since the current mirror ratio I_B/I_B' was defined to be equal to 5.

III. PHYSICAL DESIGN

The proposed OTA physical design was implemented in a $0.35\mu m$ 3.3V CMOS standard process. The overall layout including the biasing network is shown in Fig. 3.

The layout was made considering the mitigation of process gradients and mismatch by using a quite symmetric floorplan and trying to reduce parasitic capacitances by placing the transistors in close proximity. Besides, the input transistors were laid out using a cross-coupled common centroid structure. The overall on-chip area is approximately $83.5\mu m \times 105.8\mu m$.

The amplifier does not require additional compensation elements since it is a single-stage self-compensated amplifier on which the load capacitance is used for this purpose.

IV. SIMULATION RESULTS AND DISCUSSION

The OTA has been evaluated with the analog simulator Spectre at post-layout level. Main performance parameters are included in Table I using a 4pF load. The results show that the OTA provides a large slew rate, high gain in the order of 80dB, and good stability margins across the bandwidth of interest. Besides, it can operate at very low power levels below 50uW.

The performance of the proposed amplifier was evaluated against a classical two-stage class A/AB amplifier, similar to the one presented in [10]. Comparative results are presented

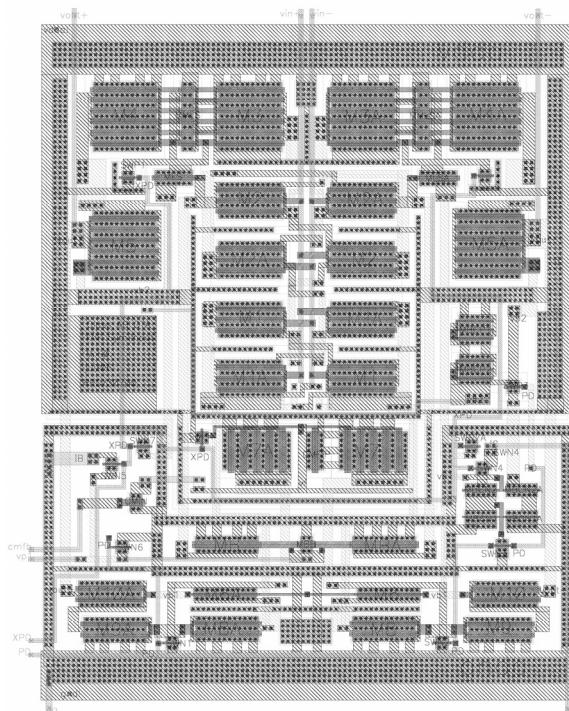


Fig. 3. Proposed OTA layout.

TABLE I
PROPOSED OTA MAIN PERFORMANCE PARAMETERS ($C_L=4pF$)

Parameter	$I_B'=0.2\mu A$	$I_B'=0.72\mu A$	$I_B'=10\mu A$
	$I_C=2\mu A$	$I_C=3\mu A$	$I_C=12\mu A$
DC Open Loop Gain SE (dB)	84.62	86.02	78.82
Unity Gain Frequency (MHz)	2.20	6.95	49.17
Phase Margin (°)	81.66	81.10	78.77
Dominant Pole (kHz)	0.127	0.336	5.30
SR Positive (MV/s)	39.51	83.90	169.74
SR Negative (MV/s)	38.28	83.39	168.68
1% Settling Time + (ns)	196.45	70.14	14.27
1% Settling Time - (ns)	210.35	73.40	14.40
Power Consumption (μW)*	45.58	146.05	1945.30
1/f Noise @1Hz ($\mu V/\sqrt{Hz}$)	3.28	2.78	3.05
Thermal Noise (nV/\sqrt{Hz})	56.80	46.22	41.39
Noise Corner Freq. (kHz)	1.11	1.21	1.81
Distortion @ 1 MHz (%)	2.75	0.45	0.49m

*including biasing network.

both in Table II and in Fig.4, which show how the main performance parameters behave as a function of the UGBW. Occupying just about one-fourth of the on-chip area with respect to the reference A/AB amplifier, at a UGBW near to 7MHz, the proposed OTA provides a slew rate 8 times larger, consumes 35% less static power consumption and settles 2.8 times faster (See Table II). This tendency is also kept at higher bandwidths. At a UGBW of about 43MHz the slew rate is still almost 20% higher, and the power consumption is 42% lower for the proposed OTA.

TABLE II
COMPARATIVE RESULTS ($C_L=4\text{PF}$)

Parameter	Proposed	Reference	Proposed	Reference
	UGBW	UGBW	UGBW	UGBW
	6.9MHz	6.6MHz	43.2MHz	42.7MHz
DC-Gain SE (dB)	86.02	90.47	80.17	78.58
Phase Margin (°)	81.10	65.40	79.02	69.27
SR+ (MV/s)	83.90	10.4	164.39	138.62
SR- (MV/s)	83.39	10.4	163.32	138.18
Settling Time+ (ns)	70.14	199.63	16.37	26.89
Settling Time- (ns)	73.40	199.76	16.45	26.91
Power (μW)*	146.05	224.41	1566.00	2730.30

*including biasing network.
Settling time calculated at 1%.

V. CONCLUSION

The realization of a configurable single-stage class AB OTA for SC applications has been addressed. It was shown that this approach is suitable for the design of low-power high-slew rate SC-stages operating at low to medium frequencies. This approach is an attractive solution in applications such as $\Sigma\Delta$ -converters for portable biomedical applications.

REFERENCES

- [1] F. Medeiro, A. Perez-Verdu, and A. Rodriguez-Vazquez, "Top-down design of high-performance sigma-delta modulators", The Netherlands: Kluwer Academic Publishers, 1999.
- [2] R. G. Carvajal, J. Galán, J. Ramirez-Angulo, and A. Torralba, "New low-power low-voltage differential class-AB OTA for SC circuits", IEEE International Symposium on Circuits and Systems, 0-7803-7761-3, 2003.
- [3] B. J. Hosticka, "Dynamic CMOS amplifiers", IEEE Journal of Solid-State Circuits, Vol. SC-15, No. 5, October 1980.
- [4] A. Mora-Sanchez, D. Schroeder, and W. H. Krautschneider, "Sigma-delta modulators of 2nd- and 3rd-order with a single operational transconductance amplifier for low-power analogue-to-digital conversion", Proc. of 16th ProRisc Workshop on Circuits, Systems and Signal Processing, Veldhoven, Netherlands, 2005.
- [5] V. Peluso, M. Steyaert, and W. Sansen, "Design of low-voltage low-power CMOS delta-sigma A/D converters", Kluwer Academic Publishers, 1999.
- [6] O. Choksi, and L. R. Carley, "Analysis of switched-capacitor common-mode feedback circuit", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 50, No.12, December 2003.
- [7] J. Ramírez-Angulo, R.G. Carvajal, A. Torralba, J. Galant, A. P. Vega-Leal, and J. Tombs, "The flipped voltage follower: a useful cell for low-voltage low-power circuit design". IEEE International Symposium on Circuits and Systems, vol. 3, 0-7803-7448-7, 2002.
- [8] A. J. López-Martín, S. Baswa, J. Ramirez-Angulo, and R. González-Carvajal, "Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency", IEEE Journal of Solid State Circuits, Vol. 40, No. 5, May 2005.
- [9] H. Chung-Chih, H. Changku, and M. Ismail, "CMOS low-voltage rail-to-rail V-I converter", Proc. 38th MWSCAS, vol.2, pp. 1337-1340, 1995.
- [10] S. Rabii, and B. A. Wooley, "A 1.8-V digital-audio sigma-delta modulator in 0.8- μm CMOS, IEEE Journal of Solid-State Circuits, Vol. 32, No. 6, June 1997.

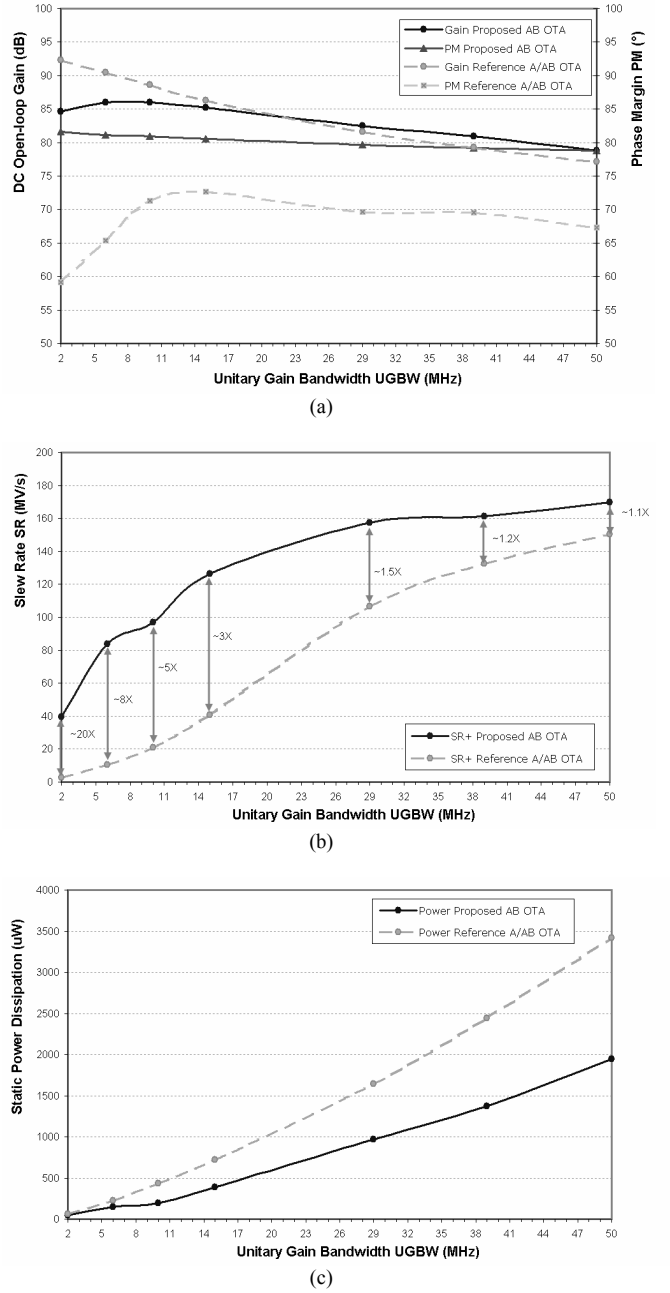


Fig. 4. Main performance parameters as a function of the unitary gain bandwidth (UGBW): (a) open-loop gain and phase margin, (b) slew rate, and (c) static power dissipation, for the proposed class AB OTA and the reference A/AB OTA.