

# Power Optimization for Pipelined ADCs

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*Abstract*—

The developments over the last years in portable and wireless communications have increased the demand for low power circuits and systems. Analog-to-digital converters (ADCs), as essential parts of these systems, should comply with this low power consumption trend. The pipelined ADC in particular is one of the most popular ADC architectures, because it exhibits very good speed and power consumption capabilities and can be easily implemented in digital CMOS technologies. Therefore a systematic study of power optimization for pipelined ADCs became necessary.

## I. INTRODUCTION

Nowadays, we are witnessing an increasing demand for portable and wireless communication applications. One of the main constraints in the design of circuits and systems for such applications is the low power consumption. Pipelined ADCs have become very popular choice for these systems, because they offer very good performance in terms of speed and power and can be combined with digital signal processing on a single substrate.

Usually, the designers of pipelined ADCs adopt *closed-loop* structures (incorporating a high gain opamp) for the implementation of the residue amplifiers. This solution uses the feedback mechanism and trades high opamp gain for high linearity.

On the other hand, nowadays, pipelined ADCs incorporating *open-loop* residue amplification are increasingly gaining designer's attention [1], [2]. Open-loop amplifiers are simpler than their closed-loop counterparts and by avoiding high-gain and wide-bandwidth requirements they are capable of consuming less power and/or operating at higher speeds.

Moreover, the need to reduce the design effort, cost and time dictates the usage of more flexible/modular designing methods and circuit/system architectures. The application of this design methodology to ADCs leads to flexible/modular pipelined ADCs that employ *identical stages*, [3].

Therefore, it is clear that a systematic study of

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power optimization for pipelined ADCs is necessary. Several studies can be found in literature [4], [5], [6], [7] and many models have been proposed. In this line of work we present power optimization methodologies for all three types of pipelined ADCs mentioned above, namely, ADCs with *closed-loop amplifiers*, *open-loop amplifiers* and *identical stages*.

Section II presents a study on the power optimization of pipelined ADC incorporating closed-loop amplifiers, while the next section (III) presents theory and results concerning power optimization of pipelined ADC incorporating open-loop amplifiers. Furthermore, section IV addresses the power consumption issue in modular pipelined ADC (identical stages) and presents a bias current scaling scheme.

## II. CLOSED-LOOP RESIDUE AMPLIFIERS, [5]

Concerning the  $kT/C$  related power consumption in a pipelined ADC, we can carry out a simple analysis according to find optimum distribution of power and capacitor size such as to minimize the overall power. The capacitor scaling is a result of the relaxed accuracy requirements (with respect to the thermal noise) due to the amplification of the previous stages. Therefore, we can scale down the sampling capacitors along the pipelined chain without compromising the accuracy of the converter. We can define the *scaling factor* [5] equal to

$$s = \frac{C_{S_i}}{C_{S_{i+1}}} = 2^{nx} \quad (1)$$

where  $C_{S_i}$  is the sampling capacitor of the  $i^{th}$  stage,  $n$  is the effective number of bits per stage and  $x$  is the *taper factor*,  $x \in [0,2]$ , a parameter that defines how "aggressive" or not is the applied scaling.

It has been proven, [5], using the model depicted in figure 1 and assuming constant resolution per-stage that the total power consumption of ADC is given by the formula:

Total Pipelined Power

$$\sim \left[ 2^{n(1-x)} + 1 - \frac{1}{2^n} \right] \left( \frac{1}{1 - \frac{1}{2^{nx}}} \right) \left[ \frac{1}{1 - 2^{n(x-2)}} \right] \quad (2)$$

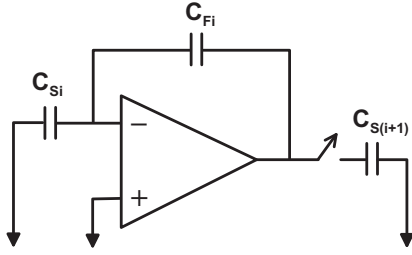


Fig. 1. Model for capacitor scaling in closed-loop ADCs.

Figure 2 depicts the normalized total power of the pipelined ADC versus the taper factor with  $n$  as parameter.

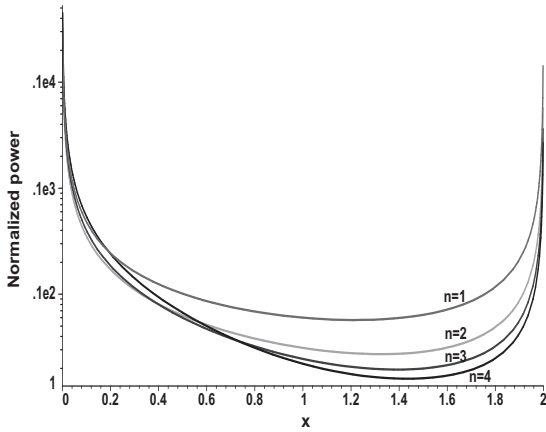


Fig. 2. Optimum capacitor scaling.

The total consumed power reduces when higher resolution per-stages ( $n$ ) are considered. Furthermore, for larger  $n$  more aggressive scaling (higher  $x$ ) leads to power savings.

### III. OPEN-LOOP RESIDUE AMPLIFIERS, [8]

#### A. Theory

##### A.1 Thermal noise calculations

Fig. 3 depicts the typical structure of a pipelined ADC (a) and the internal view of its stages (b).

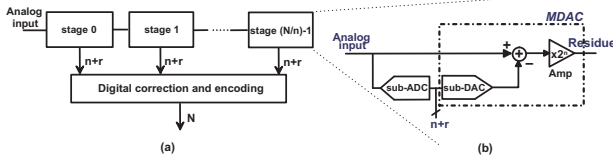


Fig. 3. A typical pipelined ADC

The stage is composed of an  $(n+r)$  bits flash sub-ADC (essentially comparators), an  $(n+r)$  bits sub-DAC, a subtraction block and an amplifier with gain of  $2^n$ . The effective resolution of each block is  $n$  bits

and  $r$  redundant bits are reserved for digital correction, [8].

According to ease the calculations and make the extraction of useful information feasible, the effective resolution ( $n$ ) and redundancy ( $r$ ) are assumed to be constant along the pipelined chain of the ADC. Although power savings do exist by allowing varying resolution from stage to stage, for the clarity of analysis we limit ourselves to constant resolution per stage, which is still valid and realistic (e.g. in case that fast time-to-market is an issue).

The input referred thermal noise of a pipelined ADC is given by Eq. 3:

$$k_B T \left[ \frac{1}{C_{S_0}} + \frac{1}{2^{2n} C_{S_1}} + \frac{1}{2^{4n} C_{S_2}} + \frac{1}{2^{8n} C_{S_3}} + \dots \right] \quad (3)$$

where  $k_B$  is Boltzmann's constant,  $T$  the temperature in K and  $C_{S_i}$  the total sampling capacitance of the  $i^{th}$  stage.

It is clear that the input referred thermal noise and the noise distribution is dependent on two factors (*i*) the size of the sampling capacitors ( $C_{S_i}$ ) and (*ii*) the effective resolution per stage ( $n$ ). Therefore, finding the optimum scaling means finding the optimum values for those two parameters.

We can identify two extremes:

- *No scaling*, in which all the stages have the same size and contribute equally to the power consumption. In that case the thermal noise is dominated by the front-end of the pipelined chain.
- *Aggressive scaling*, in which all the stages contribute equally to the input referred thermal noise. In that case, the power is dominated by the front-end of the pipelined chain.

Assuming that the capacitance of the  $0^{th}$  stage is  $C_{S_0} = C_{unit} 2^n$ , where  $C_{unit}$  is a unit capacitance, the sampling capacitance of the  $i^{th}$  stage can then be expressed as in Eq. (4):

$$C_{S_i} = \frac{2^n C_{unit}}{2^{inx}} \quad (4)$$

Given that the input-referred noise should be equal to or smaller than  $\frac{1}{2}$  LSB leads to Eq. (5)

$$k_B T \left[ \frac{1}{C_{S_0}} + \frac{1}{2^{2n} C_{S_1}} + \frac{1}{2^{4n} C_{S_2}} + \dots \right] \leq \left( \frac{2FS}{2^N \sqrt{2}} \right)^2 \quad (5)$$

where  $N$  is the total ADC resolution and  $\pm FS$  the voltage range. Combining equations (4) and (5),  $C_{unit}$  can be expressed as a function of  $N$ ,  $n$ ,  $x$  and different technological constants.

## A.2 Comparators' input capacitance calculation

We can prove that for a pipelined ADC incorporating  $r$  redundant bits in the sub-ADCs, the maximum allowable deviation of the comparison level is:

$$\delta_{max} = \frac{FS}{2^n} \left(1 - \frac{1}{2^r}\right) \quad (6)$$

We limit the stochastic deviation  $\delta_{max}$  by  $4\sigma$  and we use that  $\sigma = \frac{AV_{th}}{\sqrt{W_C L_C}}$ , [9], (neglecting  $A_\beta$ ), where  $W_C$  and  $L_C$  are the dimensions of the comparators' input transistors.

Given that the input capacitance of a single comparator is  $C_{C_{unit}} = RW_C L_C$  ( $R$  is a constant of proportionality, which depends on the comparator's topology and technological constants), we can prove:

$$C_{C_{unit}} = R \left( \frac{4AV_{th} 2^{(n+r)}}{FS (2^r - 1)} \right)^2 \quad (7)$$

Therefore, since the number of comparators per sub-ADC is  $2^{(n+r)} - 1$ , the total input capacitance of a sub-ADC is:

$$C_C = R \left( 2^{(n+r)} - 1 \right) \left( \frac{4AV_{th} 2^{(n+r)}}{FS (2^r - 1)} \right)^2 \quad (8)$$

The comparators are not scaled-down along the pipelined chain, because their accuracy requirements do not depend on their position in the chain due to the use of redundant bits. For the rest of this study we consider one bit of redundancy ( $r=1b$ ), since this is a very common implementation practice.

## A.3 Final calculations

Fig. 4 shows the model that we use to carry out the calculations.

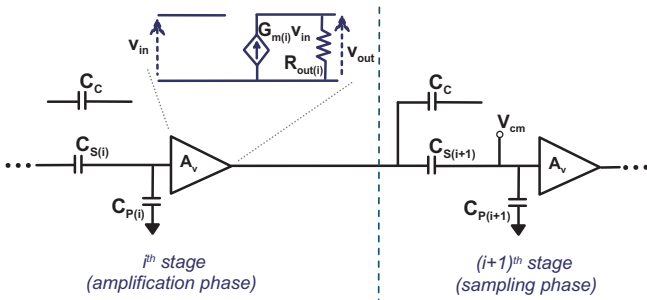


Fig. 4. The model used for calculations

$C_{S_i}$  is the sampling capacitance of the  $i^{th}$  stage,  $C_C$  the input capacitance of the sub-ADC and  $C_{p_i}$  the parasitic capacitance at the input of the open-loop amplifier of the  $i^{th}$  stage. The amplifier has been

modeled in a simple way according to ease the calculations. Due to charge sharing (between  $C_{S_i}$  and  $C_{p_i}$ ) the signal at the input of the amplifier is attenuated demanding a higher gain to compensate this loss. Therefore, the amplification is given by:

$$A_v = \left(1 + \frac{C_{p_i}}{C_{S_i}}\right) 2^n \quad (9)$$

The total load capacitance of the  $i^{th}$  stage is:

$$C_{L_i} = C_{S_{i+1}} + C_C \quad (10)$$

We assume that the amplifier scales-down with the same rate as the sampling capacitor and hence,  $C_{p_i}/C_{S_i} = constant$ .  $C_{p_i}$  does not load the input of the previous stage and is not included in Eq. 10, because during the sampling phase of the  $(i+1)^{th}$  stage (amplification phase for the  $i^{th}$ ) the input of the amplifier is connected to the common mode voltage ( $V_{cm}$ ).

It can be proven that the settling time of each stage (for linear settling) is given by  $\tau_{sett} = \tau_i (N - in) \ln 2$ , in which  $\tau_i = R_{out_i} C_{L_i}$  is the time constant of the amplifier. Therefore, according to the model of Fig. 4:

$$\tau_{sett} = R_{out_i} C_{L_i} (N - in) \ln 2 \quad (11)$$

By substituting Eq. 4 and Eq. 8 in Eq. 10 and having already expressed  $C_{unit}$  in the desired units  $N, n, x$  (section III-A.1), we express  $C_{L_i}$  of every stage as a function of  $N, n, x, r$  and different technological and topological constants.

Assuming that the open-loop amplifier is a differential pair with resistor load [1], we have  $G_{m_i} = \sqrt{\mu_n C_{ox} \frac{W_i}{L_i} I_{b_i}}$ , where  $W_i$  and  $L_i$  are the dimensions of the input transistors and  $I_{b_i}$  the biasing current of the differential pair. Additionally, Fig. 4 indicates  $A_V = G_{m_i} R_{out_i}$ .

Using the above formulas, we can express  $I_{b_i}$  as a function of  $N, n, x, r$  and different technological and topological constants.

The total power consumption of ADC ( $P_{cons.}$ ) is dominated by the power consumed by the amplifiers. Therefore, a coarse but valid estimation is:  $P_{cons.} \sim \sum_i I_{b_i}$ . In the following section we present arithmetical results based on this estimation. A close-form analytical expression of  $P_{cons.}$  is in principle possible but not helpful due to its complexity.

## B. Results

This subsection presents the optimum choices for  $n$  and  $x$  employing different ADC resolutions ( $N$ ). In

particular, we performed calculations for four different resolutions ( $N \in \{10b, 12b, 14b, 16b\}$ ), because we identify this range of resolutions as the most relevant for a pipelined ADC.

According to make some arithmetic results feasible and draw useful conclusions, we use typical values for the technological constants taken from a CMOS18 technology.

Fig. 5 depicts the total (normalized) power of a 10b pipelined ADC as a function of the taper factor ( $x$ ) and the number of bits per stage ( $n$ ) as a parameter. The optimum choice is  $n=1b$  with  $x$  approximately 1.5. As we increase  $n$ , the total power of the ADC increases resulting in non-optimum implementations.

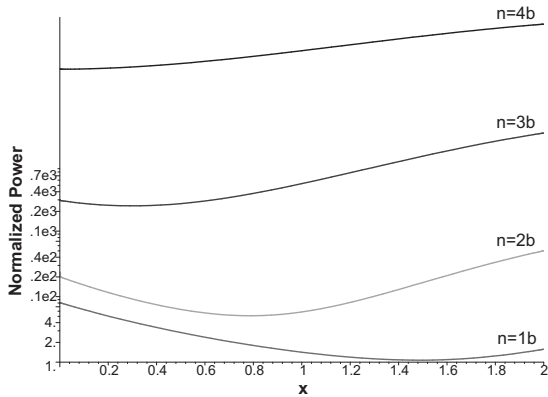


Fig. 5. Pipelined ADC with  $N=10b$

If we increase  $N$  to 12b and perform the calculations, Fig. 6 shows the optimum  $n$  and  $x$ . Now we can

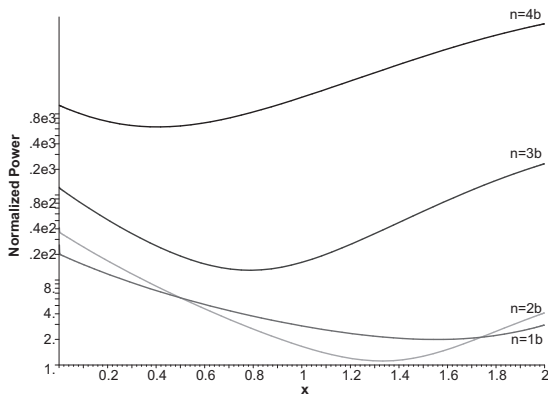


Fig. 6. Pipelined ADC with  $N=12b$

see that the optimum choice is  $n=2b$  and  $x$  approximately 1.3. The choice  $n=1$  gives sub-optimum implementation, as well as the choices  $n=3b$  and  $n=4b$ . Another observation is that the minimum of every curve is shifted to a higher  $x$  value, meaning that by using more bits per stage we have to scale more aggressively.

Increasing the total number of bits further

( $N=14b$ ), Fig. 7 shows the optimum  $n$  and  $x$  choices. The choice  $n=2b$  remains the optimum, but it is fol-

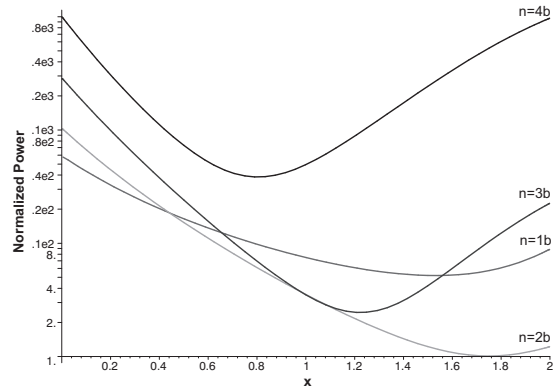


Fig. 7. Pipelined ADC with  $N=14b$

lowed by  $n=3b$  and not by  $n=1b$  as in the  $N=12b$  case. Moreover, the minimum of every curve is even shifted further to higher  $x$  values resulting in an optimum taper factor of, approximately, 1.75.

Finally, for  $N=16b$ , Fig. 8 shows the optimum  $n$  and  $x$  choices. In this case the optimum choice is

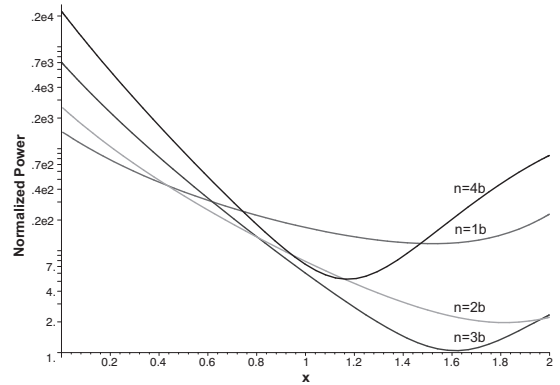


Fig. 8. Pipelined ADC with  $N=16b$

$n=3b$ , followed by  $n=2b$ ,  $n=4b$  and  $n=1b$  (in increasing total power order). Again the minimum of every curve is shifted to higher values of  $x$ , implying that for high resolution ADCs more aggressive scaling is preferable.

The results above reveal that for higher ADC resolutions, if we scale-down the sampling capacitors, it is beneficial to use higher number of bits per-stage. The interpretation is that the increase in the total number of comparators and the load connected to them ( $C_C$  part of Eq. 10) does not overrule the power savings due to the reduced number of amplifiers, even if they should have higher amplification ( $A_v \sim 2^n$ ).

#### IV. ADCs WITH IDENTICAL STAGES, [10]

##### A. Theory and Results

In the modular pipelined ADCs, [3], and in general in those with identical stages (e.g. for fast time-to-market) we cannot apply capacitor scaling. Therefore, we pay a high power penalty due to the wanted modularity.

Under the assumption that the amplifier is not slew-rate limited, but it settles with a pure linear way, following an exponential relation ( $1 - e^{-\frac{t}{\tau_o}}$ ), we can prove that the minimum amplifier bias current ( $I_{bias}$ ) is determined by the largest  $\frac{dV}{dt}$ , meaning, the value needed for the initial transition, [10]. Therefore,

$$I_{bias} = C_L V_{sig} \frac{1}{\tau_o} \quad (12)$$

where,  $C_L$  is the load capacitance,  $\tau_o$  is the settling time constant of the amplifier and  $V_{sig}$  the signal amplitude. Moreover, it can be proved that the settling time requirement of each stage ( $\tau_{sett}$ ) is dependent on the  $\tau_o$  and the position of the stage in the pipelined chain and is given by:

$$\tau_{sett}(= \frac{1}{2f_s}) = \tau_{o_i}(N - in) \ln 2 \quad (13)$$

where  $N$  is the resolution of the converter on bits,  $n$  the effective number of bits per stage and  $i$  is a number that determines the position of the stage in the pipelined chain,  $i \in [0, \frac{N}{n} - 1]$ . Combining the two previous formulas we have:

$$I_{bias_i} = 2C_L V_{sig} \ln 2 (N - in) f_s \quad (14)$$

The above formula shows the dependency of  $i$  and  $f_s$  on the  $I_{bias}$ .

Therefore, based on formula 14, we propose the *self-adjusting current technique*, [10], as a power efficient way to bias the amplifiers of the stages without compromising the performance nor the modularity of our converter. The adjustment of the ( $I_{bias}$ ) can be twofold:

1. The  $I_{bias}$  is made proportional to the sampling frequency,  $f_s$ .
2. The  $I_{bias}$  of every stage is adjusted individually according to its position in the pipelined chain.

For a given  $N$  and  $f_s$  we can calculate, based on that formula, the power savings due to the scaling of the ( $I_{bias}$ ) along the pipelined chain. Taken into account that the power consumption is proportional to the summation of the bias currents of each stage,

we determine the power saving in comparison to the non-scaling case.

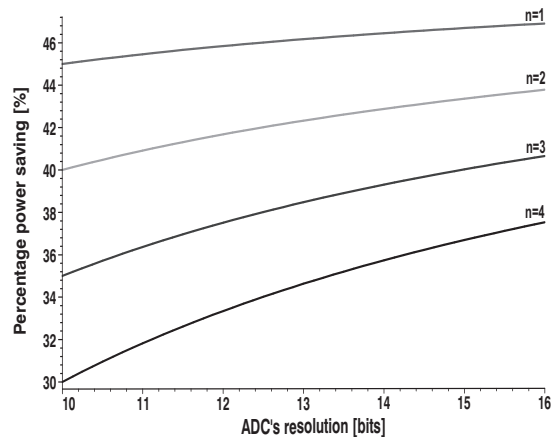


Fig. 9. Percentage power saving due to bias current scaling.

Figure 9 shows that we have the maximum power saving for large  $N$  and  $n=1$ , because this case allows extensive use of scaling. The power savings can be approximately 46%.

Finally, for a given resolution ( $N=14$ ) and  $n$  as parameter, figure 10 shows how the bias current scales along the pipelined chain (normalized values).

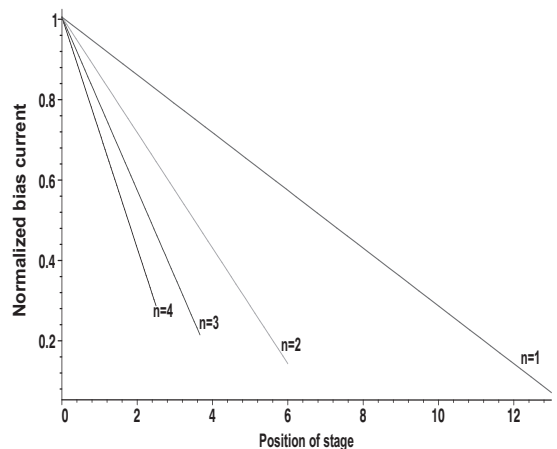


Fig. 10. Bias current value along the pipelined chain.

##### B. Circuits

According to apply the above described technique to a pipelined ADC we have to answer two questions:

1. How can we generate a bias current proportional to the  $f_s$  and the position of the stage in the pipelined chain?
2. Is the OTA still operational varying the  $I_{bias}$  through quite a large range of values?



Consequently, knowing the variation on  $f_{c_o}$  and  $A_o$  we can take it into account during the design phase of the system.

## V. CONCLUSIONS

In this paper we present different power optimization methods for different pipelined ADC realizations, using as main parameter the total ADC resolution. We present the optimum number of bits per-stage and capacitor scaling for closed-loop pipelined ADCs and we report a model and calculations that lead to optimum power consumption for open-loop pipelined ADCs. Finally, we present the parametric (bias current) scaling as an alternative solution to the hardware (capacitor) scaling, when the last one is not applicable (i.e. pipelined ADCs with identical stages).

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