Sigma Delta ADC with Accurate Dynamic Reference for Temperature Sensing and Voltage Monitoring

N. Saputra, M. A. P. Pertijs, K. A. A. Makinwa, and J.H. Huijsing

Abstract— **A second-order sigma-delta analog-to-digital converter (ADC) with 12-bit absolute accuracy has been designed using a 0.7µm CMOS technology. The ADC is part of an accurately trimmed temperature sensor. The temperature sensor employs a dynamic reference voltage, which is well defined over a large operating temperature range (-40°C to 125°C). Its curvature error is corrected at the system level by using a look-up table driven feedback loop. The result is a low cost accurate temperature sensor with additional voltage sensing capability. The input dynamic range is from 0 to V_{DD} for V_{DD} ranging from 2.5-5.5V. The chip area is 6.4mm^2, and has a current consumption of 85µA.**

Index Terms— **ADC, Dynamic Reference, Temperature sensor, Sigma Delta, and Switched capacitor circuit.**

I. Introduction

An Analog-to-Digital Converter (ADC) is probably one of the most important components of data acquisition systems. ADCs convert voltages that represent real world signals into bits that can be manipulated by microprocessors or software. The analog-to-digital conversion process involves sampling the applied analog input signal and quantizing it to a digital representation by comparing it to a reference voltage.

For audio or instrumentation applications, which require high resolution with low sampling rates, ADCs in the low speed and high accuracy class are suitable. Sigma-delta ADCs are members of this class of ADC. The sigma-delta architecture is very attractive because it has several advantages [1-3][11-12]:

- Simple and compact architecture, thus requires a small number of component
- Low power consumption, especially at low sampling rates
- No component matching required and relaxed component accuracy
- High resolution possible
- Direct trade off between resolution and sampling rate
- Serial clock-synchronous output

A switched capacitor high accuracy smart temperature sensor (SCHAT), with a 3σ inaccuracy of ±0.1°C over the military temperature range has been built [4]-[6]. The sensor uses a sigma-delta ADC to determine the ratio between a proportional to absolute temperature (PTAT) voltage and a built in voltage reference. Here, this well proven architecture is modified to build an accurate general-purpose ADC. Many ADC designs assume the existence of an accurate external reference voltage and since their accuracy depends on the quality of the reference voltage it is specified as a relative accuracy. Designing a built-in reference voltage with high accuracy is quite challenging, especially when it must maintain accuracy across a large temperature range. In this context, SCHAT has promising features such as [4]-[6]:

- Accurate temperature sensing capability
- A 16-bit sigma-delta ADC
- An accurate dynamic voltage reference

For this reason, it was decided to implement a voltage sensing ADC as an extended version of this high accuracy temperature sensor.

II. SCHAT

Temperature sensors are widely used in many applications such as measurement, instrumentation and control systems. Therefore, it is attractive to have temperature sensors with digital output. Such *smart* temperature sensors combine a sensor and its electronic interface on a single chip. It is also preferable that the temperature sensor is manufactured in a low-cost standard CMOS process. The realization in 0.7μm CMOS meets the target of ±0.1°C over the full military temperature range of −55°C to 125°C [4]-[6].

SCHAT was designed to achieve an overall inaccuracy of ±0.1°C or equivalent to 200µV. The design method involved reducing all temperature errors resulting from circuit non-idealities to the 0.01°C level. The design techniques used to reduce these errors are as follows:

- Errors due to offset were reduced by a combination of correlated double-sampling and system-level chopping in the ΣΔ converter, and chopping in the bias circuit.
- A special bias circuit was designed to make the sensor insensitive to variations in the current gain of the substrate bipolar transistor used, and to variations in the supply voltage.

- Mismatch-related errors were eliminated by means of dynamic element matching.
- Temperature dependent curvature was corrected by using a temperature-dependent reference and a slightly non-linear decimation filter.
- Spread of the base-emitter voltage of the bipolar transistors (the only significant error source remaining) was trimmed out by calibration at a single temperature, using a high-resolution trimming circuit based on a ΣΔ current DAC.

In order to produce a temperature reading, a temperature dependent signal has to be compared to a reference signal. While virtually every device has temperature-dependent characteristics, bipolar transistors are particularly suitable for generating this combination of signals [7-8]. They can be used as a generator for both a voltage that is accurately proportional to absolute temperature (PTAT), and a temperature-independent bandgap reference voltage. In CMOS process, substrate bipolar junction transistors (BJT) can be used for this purpose [7]. The digital output is in the form of a bit stream *(bs)* which has a density *(μ)* that proportional to temperature.

$$\mu = \frac{\alpha \cdot \Delta V_{BE}}{V_{BE} + \alpha \cdot \Delta V_{BE}} = \frac{V_{PTAT}}{V_{REF}} \qquad (1)$$

Fig. 1 shows the architecture used in SCHAT. The circuit does not require a physical reference voltage (V_{REF}). Instead, the reference is created dynamically by the averaging mechanism of the sigma-delta converter. By combining V_{BE} and $\alpha\Delta V_{BE}$ dynamically in the sigma-delta converter, an accurate voltage reference is created. The sigma-delta converter will sample $\alpha\Delta V_{BE}$, when bs = 0, and sample $-V_{BE}$, when bs = 1. The total charge from the input signal is averaged to zero by the sigma-delta converter. As a result of this averaging mechanism, the output bit stream density *(μ)* is the ratio of $\alpha\Delta V_{BE}$ and $V_{REF} = \alpha\Delta V_{BE} + V_{BE}$, as stated in (1).

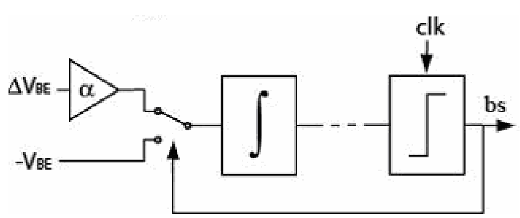

Fig. 1. Block diagram of SCHAT

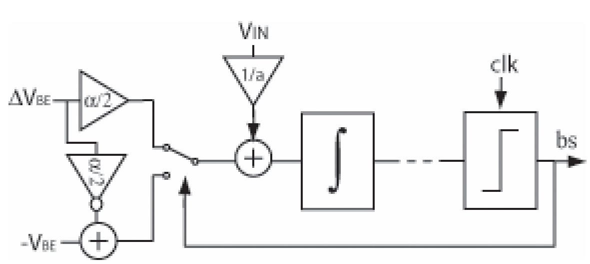

Fig. 2. Proposed architecture block diagram for the ADC

III. ADC ARCHITECTURE

The desired bit stream density of the voltage sensing ADC will be a ratio of a scaled version of V_{IN} and V_{REF}. However, a single loop second-order sigma-delta converter is only conditionally stable. Long limit cycles will occur for small non-zero V_{IN} and for large V_{IN} i.e. values close to V_{REF} When this occurs, the averaging mechanism does not work properly, because the decimation filter can not filter the resulting low frequency components (tones) [1].

The proposed solution is by introducing a known offset, such that the bit density will always be in the middle of its range for all possible values of V_{IN}. On top of that, V_{IN} must also be scaled down, so that its maximum value is smaller than V_{REF}. For a second-order converter, it is advantageous to limit the range of the input signal to about 0.5 to 0.6 V_{REF} [11]. The trade off is a loss of resolution, since the converter does not use its full range. To be able to measure a maximum supply rail voltage of 5.5V, V_{IN} must be at least scaled down by a factor of a = 10, for $V_{REF} \sim 1.2$V

Considering the dynamic range of V_{IN} with respect to the V_{REF}, the desired output bit stream density equation is:

$$\mu = \frac{V_{OFFSET} + V_{IN} / a}{V_{REF}} \qquad (2)$$

The ideal offset voltage will be a constant voltage, which is a fraction of the reference voltage. However, the implementation of this requires a complex architecture, which is quite different compared to the existing architecture of the temperature sensor. For simplicity, the architecture described in Table I was adopted. Here, a temperature dependent offset (a scaled version of $\alpha/2(\Delta V_{BE})$) is used instead of a constant voltage offset. Fig. 2 shows the block diagram of the proposed architecture.

TABLE I Proposed architecture

When *bs* = 0 ΣΔ sampled $\alpha/2.\Delta V_{BE}$ and $+ V_{IN}/10$
When *bs* = 1 ΣΔ sampled $\alpha/2.\Delta V_{BE}$, V_{BE} and $-V_{IN}/10$
So, the **charge balance** equation is: $\mu\left(\frac{\alpha \cdot \Delta V_{BE}}{2} + V_{BE} - \frac{V_{IN}}{10}\right) - (1-\mu)\left(\frac{\alpha \cdot \Delta V_{BE}}{2} + \frac{V_{IN}}{10}\right) = 0$ And the **bit stream density** is: $\mu = \frac{\frac{\alpha.\Delta V_{BE}}{2} + V_{IN}/10}{(V_{BE} + \alpha \cdot \Delta V_{BE})}$

A band-gap voltage reference will exhibit a temperature dependent curvature.[7]. As a result the reference voltage still has some temperature dependence in the desired operating temperature range (220°K – 400°K). The error caused by curvature has to be corrected in if the ADC is to be capable of accurate voltage measurements over the whole operating temperature range. In order to do this, the temperature must be known. So to make an accurate voltage measurement, multiple measurement steps are needed. These steps are shown in Fig. 3.

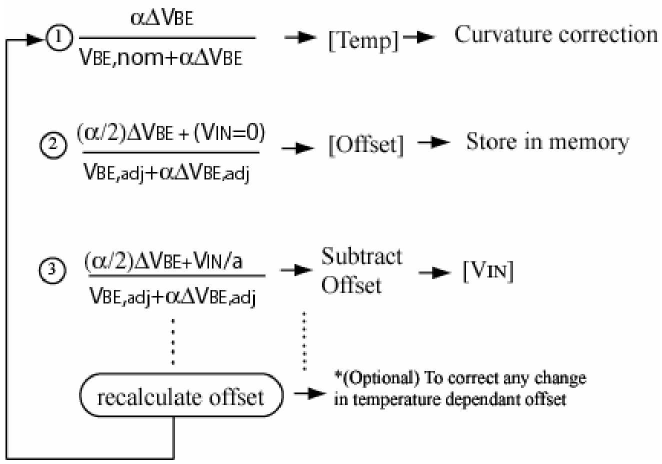

Fig. 3. Measurement procedure

Initially, the temperature must be measured accurately. This can be done by using SCHAT as a temperature sensor. From the known temperature result, the curvature correction can be performed. Curvature correction will generates $V_{REF,adj}$, a new compensated reference voltage.

The next measurement step is to measure the temperature dependent offset. Offset measurement is done by applying $V_{IN} = 0V$ to the ADC, and measuring the resulting temperature dependent offset. This measurement also effectively acts as a system-level auto-zero, which reduces the overall offset error in the system. The offset measurement result is stored in memory, which later will be subtracted from the output bit stream density obtained when V_{IN} is applied to the ADC. Because any quantization error in the measured offset will be added directly to the measurement result, the conversion time used for the offset measurement must be larger than the normal conversion time used for $V_{IN.}$ Hence, the offset quantization error must be reduced well below half an LSB. Based on simulations, it can be said that a factor of two increases in conversion time will be sufficient to achieve this.

After one offset measurement, the ADC can be used for measuring several subsequent input voltages. The number of subsequent measurements that can be accurately made depends on the stability of the ambient temperature.

Finally, another (optional) measurement of the offset voltage can be made. This last step is not necessary if the measurement is done in a temperature stable environment. However if there is a linear temperature change during the measurement cycle, the last step is necessary to correct for the offset changes. The difference between the initial and the last offset measurement correspond to temperature changes during the measurement cycle. By using linear interpolation, the offset correction is then applied to all the previous voltage measurement result

IV. CURVATURE CORRECTION

The curvature correction can be done by changing the gain of the sigma-delta modulator or by adjusting the reference voltage as a function of temperature. The corrected transfer function is then given by (3), with *CF* as a correction factor.

$$\mu = \frac{V_{IN}}{V_{REF}(T)}.CF(T) \tag{3}$$

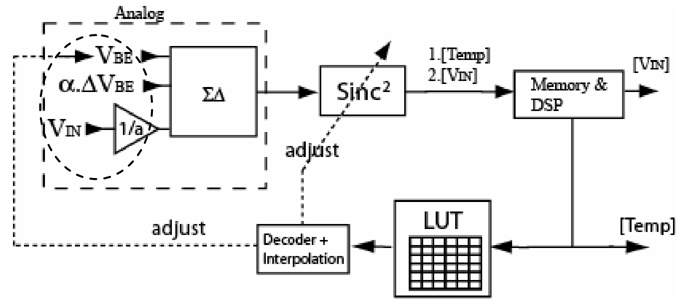

Fig. 4. Curvature correction architecture

Fig. 4 shows the block diagram of the ADC with curvature correction. A look up table stores the *CF* data obtained from either simulation or measurement. Each correction factor in the table corresponds to a specific temperature. The continuous curvature is then approximated by a piece-wise linear function. This approach can be used to approximate any kind of function. The accuracy obtained will obviously depend on the complexity of the curve and the size of the temperature interval between the point in the table.

Knowing the ambient temperature, the correction factor can be applied as a feedback into the ADC. There are several possibilities to perform curvature correction on the ADC, namely:

- adjusting the bias current of the V_{BE} generator
- adjusting the α (scaling of ΔV_{BE})
- adjusting the gain factor of V_{IN} in the prescaler stage
- adjusting the gain at the decimation filter (FIR) stage

Based on simulation, the decimation filter adjustment obtains the best result, since it has the smallest error and is simple to implement. The resolution of the decimation filter gain adjustment is high: a 1-bit step of the CF is equivalent to an 85µV step in voltage. The curvature error is corrected by creating a gain correction factor from the output bit stream of the ADC. This gain correction factor is then added or subtracted from the output of the digital decimation filter. Based on simulations, the effective gain needed for the curvature correction is shown in Fig. 5. The effective gain is expressed as a number of bits. In the implementation, this will corresponds to the width of the variable sinc filter.

Fig. 6 shows the block diagram of the temperature correction architecture. The *CF* at different temperature is stored in look up table. A sinc filter with a variable width provides a small gain modification to the original sinc^2 (triangular weighted filter). The look up table decides the width of sinc filter, so it will adjust the gain as a function of temperature. Adding a small change in the filter coefficient to the sinc2 filter only slightly changes its frequency response. Hence, this method is valid and can be easily implemented.

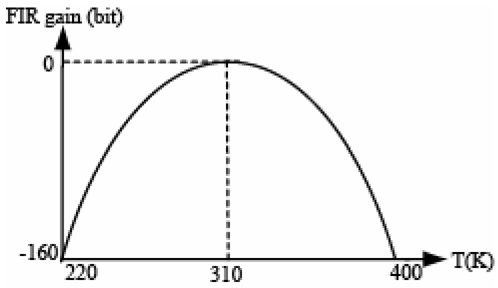

Fig. 5. Effective gain for curvature correction

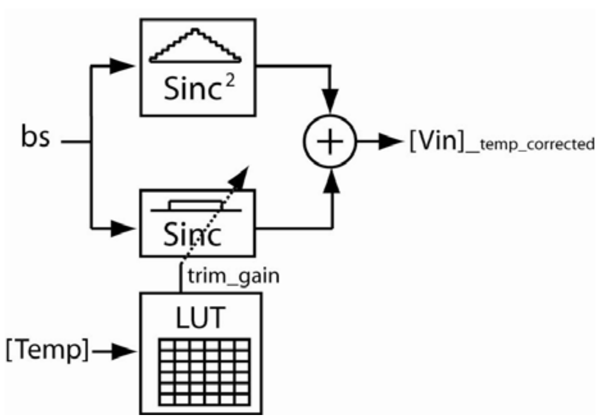

Fig. 6. Curvature correction by adjusting the decimation filter gain

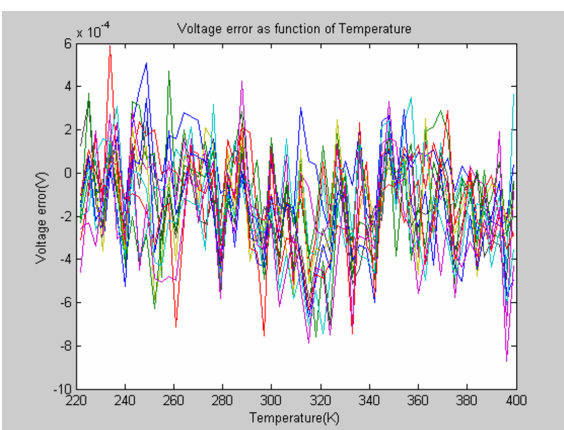

Fig. 7. Voltage error as function of temperature in decimation filter adjustment method

Fig. 7 shows the simulated voltage error at different input voltages as a function of temperature. The simulation is done with 512 samples using a sinc^2 decimation filter. This result shows that for the maximum input voltage of 5.5V, the curvature error can be corrected well enough to obtain 12-bit absolute accuracy. The whole operating temperature range is 220^{o}K to 400^{o}K.

V. CIRCUIT REALIZATION

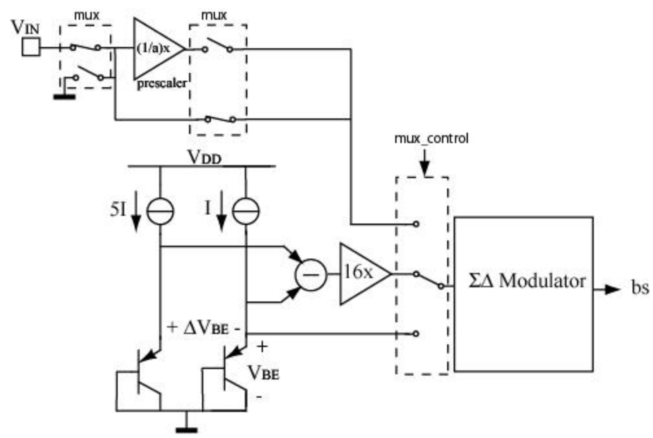

Fig. 8. Analog circuit's architecture

Fig. 8 shows the circuit architecture for the analog circuits. The prescaler block, which has a gain of 1/*a* times, is used to scale down the V_{IN}. In the implementation, the scaling factor *a* is equal to 10. This prescaler circuit must be able to detect rail-to-rail input signals. The bipolar transistor pair generates a V_{BE} and ΔV_{BE} signal. ΔV_{BE} is generated from the current bias ratio of 5, after which it is then amplified by a factor of 16. The V_{BE} signal is generated from a trimmed bias current. The multiplexer chooses the signal that will be fed into the sigma-delta converter, depending on the operating mode and the previous value of the bit stream. There are two other multiplexers for passing the prescaler stage and for grounding the input voltage during the offset measurement step.

The function of a prescaler circuit is to scale down the input signal such that it fits into the reference voltage range. The prescaler circuit must be able to accurately divide the input signal by a certain integer number, since any error in the prescaler will contribute to the total gain error. Furthermore, it is beneficial for such a circuit to be accurate by design. This means minimizing offset and/or mismatch..

The prescaler architecture is based on a switched capacitor gain circuit [9-10]. The accuracy of this circuit is enhanced by the dynamic element matching (DEM) technique. By employing the switched capacitor technique, the circuit can handle rail-to-rail input voltages without problems. A fully differential topology was used to further reduce common mode error sources, such as charge injection error and common mode noise.

Fig. 10 shows the prescaler circuit realization in differential mode and with dynamic element matching. A non-overlapping clock scheme was used, to reduce errors due to the non-idealities of the switches. DEM is employed by rotating the capacitance that samples the input signal with the other capacitances that scale down the voltage.

The prescaler must have an offset voltage much smaller than the required 12-bit quantization error. Since the amplifier has limited gain, there will still be some residual offset even after autozeroing. The residual offset is inversely proportional to the amplifier DC gain. To obtain 12-bit accuracy, a DC

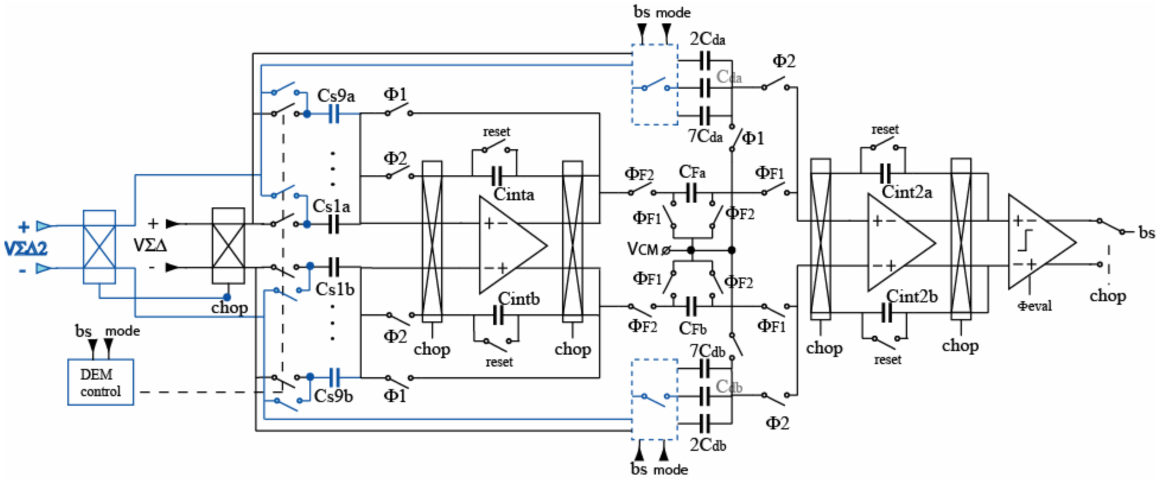

Fig. 9. A second-order incremental sigma-delta converter

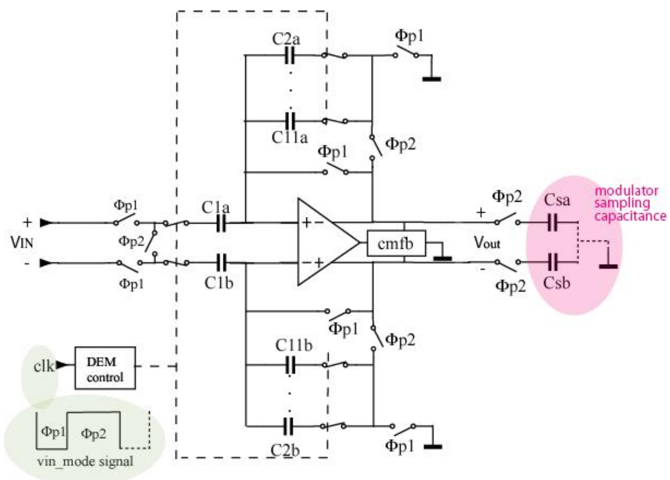

Fig. 10.Circuit realization of prescaler

gain of 90dB is necessary. Therefore the amplifier was realized by using folded cascode architecture with gain boosting [4].

A second-order sigma-delta converter, of the incremental type [12], converts the voltage input into a bit stream. Fig. 9 shows the schematic of the modified second-order sigma-delta converter. It is modified to accommodate two input signals. The digital decoder controls the number of sampling capacitors according to the operating mode of the sigma-delta. DEM is employed to reduce the mismatch between the sampling capacitors.

VI. CONCLUSION

A second-order sigma-delta ADC has been designed to obtain 12-bit absolute accuracy. It is based on an existing high-accuracy temperature sensor. The architecture of the temperature sensor was modified to allow the digitization of external voltage and to achieve the desired performance. An additional curvature correction technique was added to compensate curvature error in the ADC's reference voltage. The new design retains the temperature sensing accuracy of the original temperature sensor.

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