

Design of a Radiation Tolerant LIDAR Receiver with mm Accuracy in 0.13 μm CMOS.

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Abstract—The radiation hard design of a low noise, 500 MHz, 0.13 μm CMOS front-end for a Light Detection And Ranging (LIDAR) receiver with mm accuracy is presented. The design features enhanced tolerance to radiation induced threshold voltage shifts by employing a current steering compensation mechanism. In order to generate an accurate timing point, independent of the amplitude of the input signal, a new Current-Mode-Gain-Control (CMGC) structure was developed using a replica-based current divider. The design was simulated using a worst-case design methodology, which is developed to facilitate the design and evaluation of analog circuits that are robust to parameter shifts induced by ionizing radiation, temperature drift or intrinsic process variations.

Index Terms—CMOS, radiation hardening, analog, design methodology, current mode gain control, current steering, total ionizing dose (TID), simulation.

I. INTRODUCTION

THE aim of this work is the design of a radiation tolerant transimpedance amplifier circuit for a mm accuracy LIDAR receiver. LIDAR is the optical equivalent of the well known RADAR (Radio Detection And Ranging) system and uses optical rays instead of microwaves to determine the position of an object. The envisaged LIDAR system will be used in the MYRRHA reactor, which is being designed in the Advanced Nuclear Systems Institute of SCK-CEN.

The main focus of the LIDAR system is to measure the height of a Pb-Bi eutectic fluid in constant motion. The position needs to be determined with an accuracy of a few mm and should be updated on a ms basis. These requirements put a serious strain on the receiver specifications. The targeted accuracy corresponds with a jitter specification of only a few picoseconds. The dynamic range (DR) of the input signal can approximate 100 dB and needs to be reduced by the use of automatic gain control (AGC) structures in the receiver channel.

Besides these challenging specifications of the LIDAR receiver the necessary precautions need to be taken to improve the radiation tolerance of the circuit. The effect of ionizing radiation on CMOS integrated circuits has been described in literature [1], [2] and [3].

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To facilitate the design of the radiation tolerant front-end, the radiation effects described are modeled in a radiation model which takes into account the maximal variations of the shifts in the MOS transistor threshold voltage for the technology used. This model allows us to simulate the system for a large range of variations and foresees an evaluation of the robustness of the design to parameter shifts induced by ionizing radiation, temperature drift or intrinsic process variations.

In this work we only consider ionising gamma radiations. The radiation effects are handled at both circuit level and layout level. Since we will use radiation hardened transistors at the component level, i.e. with an enclosed lay-out and p+-guard rings, we merely consider variations of the threshold voltage shifts in our radiation model, since most radiation-induced leakage currents will be suppressed. The expected dose levels for our applications are about 1MGy in a temperature range of 25°C to 100°C.

The radiation induced shifts in the MOS transistor threshold voltage, which could degrade the performance of the circuit are tackled with a current steering compensation mechanism.

The design further introduces a low noise solution to enable CMGC, independent of the MOS transistor threshold voltage. This is conventionally implemented using a Gilbert cell, which relies on the stability of the threshold voltage [8]. Our proposed solution utilizes a replica of the low noise TIA with a variable transconductance.

This paper is therefore structured as follows. In the next chapter, after a brief summary of the most important radiation-induced effects observed in MOS structures, the design methodology for radiation hardness assurance is presented. Subsequently, the design of the LIDAR receiver front-end and the simulation results are discussed and the robustness of the receiver with respect to radiation or temperature induced changes in the threshold voltage is demonstrated.

II. DESIGN METHODOLOGY

The most sensitive part of a MOS device when exposed to ionizing radiation are the isolating oxide materials, such as the gate and the deep trench oxides. After exposure to ionizing radiation holes are trapped at the $Si - SiO_2$ interface and chemical bond rupture at the $Si - SiO_2$ interface creates new interface states. The effect of the interface states and holes trapped in the gate oxide is a radiation induced threshold voltage shift. For a PMOS transistor these two effects make the negative threshold voltage decrease under radiation. For a

NMOS the positive gate oxide charges cause an initial decrease of the threshold voltage, which is followed by a subsequent increase, caused by the charged interface states.

The field oxide of the isolation structures (STI or LOCOS) exhibits the same degradation mechanism as the gate oxide. This enables a parasitic conductive path from source to drain, which gives origin to an increase in the 'off' state current of a n-channel transistor.

The inherent radiation tolerance of the thin gate oxide of modern deep submicron CMOS technologies has made cheap, commercial-off-the-shelf (COTS) technologies appealing from a point of view of radiation hardness. Nevertheless some radiation induced shifts of the threshold voltage still remain [4]. This could degrade the performance of analog circuitry and should be avoided or compensated. Radiation hardening by layout has proven to eliminate most of the leakage current [1]. This, however, requires the use of Enclosed Layout Transistors (ELT) which tend to have a large gate and source/drain capacitances, an increased $1/f$ noise and are more cumbersome to model [1].

To simplify the design of analog circuits, that prove to be more robust to shifts in their electrical parameters, a design methodology is proposed using a worst-case design strategy. The proposed design flow is shown in figure 1.

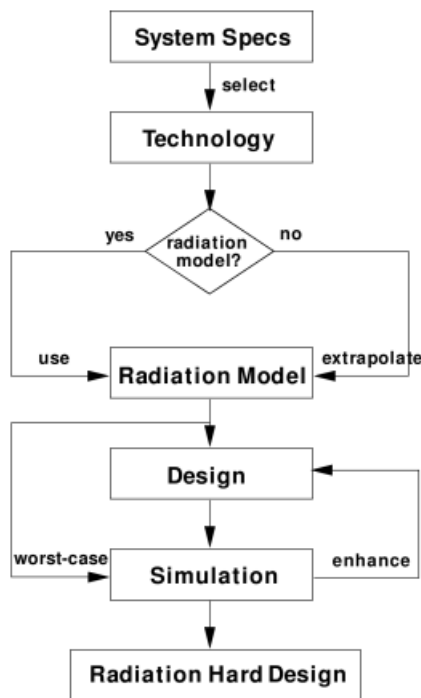


Fig. 1. Design flow for analog circuits that are robust to parameter shifts.

First an analysis of the system requirements is performed. The critical specifications of the design are identified, together with the operational and environmental conditions of the circuit. The environmental conditions of the circuit include the radiation levels, and an estimate of the temperature range.

In the next step the process technology is chosen, with a given set of intrinsic process variations. This can vary from cheap commercial technologies to more expensive and

robust technologies [5]. The scaling of technologies has shown a steep decrease of the degeneration of MOS transistors for technologies with a thin oxide [1]. This enables cheap commercial technologies in the field of radiation hard design.

Once the process technology is chosen, a radiation model can be extracted for the given environment and process technology. The design must be simulated and designed to meet the specifications under any circumstances. Therefore the model has to comply every worst-case scenario possible in the environment. The worst-case scenario means that there needs to be taken an overestimate of the real conditions to define the corners of the model. When no measurements of the process technology are available under the application specific circumstances, the model must be extrapolated from a reference radiation model. An overestimation can be assumed when a model from a technology with a thicker layer of oxide is used as a reference for extrapolation. The extrapolation is done using the $V_T \propto t_{ox}^2$ relationship. This is an overestimate for submicron technologies [7].

The design has to be flexible enough to tolerate a drift of the MOS transistor parameters. More flexibility is introduced by using an optimal operating point for the devices. The design can also be made more robust to process variations in the MOS transistor parameters. Current steering of the load transistors in a classic differential pair leads to a compensation of the threshold variations. The current steering mechanism which compensates the threshold variations is illustrated in figure 2.

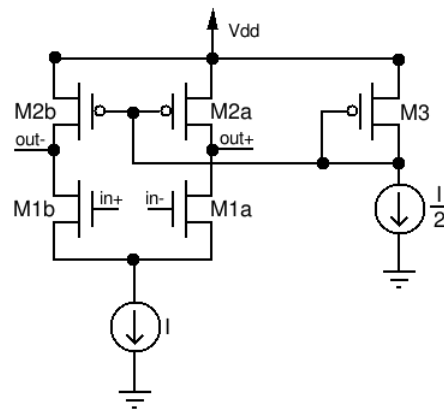


Fig. 2. Schematic representation of a current steering compensation mechanism.

When the gate of the load PMOS transistors $M_{2a,b}$ is grounded, an increase in the threshold voltage will lead to an increase in $V_{DS,M2}$. This will result in a higher output resistance. The proposed design will compensate the increase in $V_{DS,M2}$ and thus the output resistance by correcting the gate-source voltage of the load PMOS transistors, $V_{GS,M2}$. The diode-connected PMOS transistor, M_3 , will adapt his gate-source voltage $V_{GS,M3}$ to make sure that the current $I/2$ flows through the transistor, as long as he remains saturated. The corresponding variation of $V_{GS,M2}$ results in a smaller increase of $V_{DS,M2}$.

This design can be altered when the common-mode output voltage is used instead of the diode-connected transistor, M_3 . The common-mode output voltage will decrease as $V_{DS,M2}$

increases. Connecting the common-mode output voltage to the gate of the PMOS load transistors will reduce the increase in $V_{DS,M2}$. This mechanism however also needs an alternative adaptation of the biasing current to maintain the input transconductance $g_{m,M1}$. To do so, the use of bleeder transistors is needed, at the expense of an increased noise and a reduced bandwidth.

Finally, the design is simulated with a Monte-Carlo sweep that varies the parameters of the radiation model. The limits of these variations are imposed by the worst-case boundaries of this model. If the performance of the design does not meet the specifications, the design must be revised. The worst-case approach also foresees a margin that allows the designer to take peak deviations into account. The performance of the design can now be evaluated for any deviation of the parameters. In this work the shift in threshold voltage is taken equal to the largest threshold voltage shift ($\Delta V_{TN,max}$ and $\Delta V_{TP,max}$) of the weakest device for every NMOS and PMOS transistor. This does not compromise the worst-case scenario.

III. FRONT-END DESIGN

The LIDAR system is implemented using a pulsed time-of-flight (PTOF) strategy to measure the distance. The block diagram of a LIDAR system is shown in figure 3. A short laser pulse is generated and transmitted to an optically reflective target. An electrical reference signal is taken directly from the transmitter to a time interval measurement circuitry (time-to-digital converter, TDC) as a start pulse. The reflected optical pulse is detected by an external photodetector, which converts it into a current pulse.

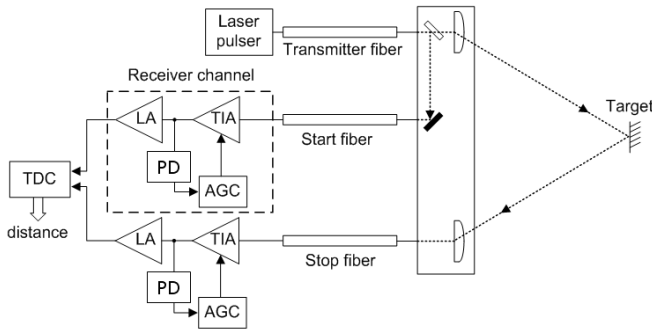


Fig. 3. Block diagram of a LIDAR system.

This current pulse is further amplified by the receiver channel and a timing discriminator generates a stop signal for the TDC. The timing point, at which the logic pulse is generated, must be independent of the amplitude of the input signal. When the zero crossing point of a differentiated, bipolar is used as a timing mark for the timing discriminator, the timing point becomes insensitive to amplitude variations. The designed receiver front-end is indicated with a dashed line in figure 3.

The schematic of this receiver channel is depicted in figure 4. The main factors that generate an error in the timing mark are amplitude variations of the input signal and noise. Amplitude variations can be minimized by the use of AGC to process the signal in a linear way. AGC is implemented

in the receiver with a CMGC cell and a Voltage Mode Gain Control R-2R voltage divider. The amplitude of the output signal is measured by the peak detector, which controls the AGC structures. The output of the peak detector produces a 4-bit digital word, corresponding to the amplitude level, measured at the output of the TIA. The bandwidth of the channel should be large enough not to distort the small pulse. For this design oversampling of the number of measurements with a factor N is chosen and the bandwidth can be reduced with a factor \sqrt{N} [9].

The fully differential transimpedance amplifier (TIA) is shown in figure 5 and is designed for low noise, high bandwidth and employs current steering for radiation purposes. To obtain low noise, the TIA has a high input transconductance (73 mS), capacitive matching with the large input capacitance of the diode (0.35 pF) and a fairly low voltage gain of the two stages A_V (≈ 25). The transimpedance resistance is limited to $4\text{ k}\Omega$ in order to satisfy the bandwidth requirement. The second stage can be made significantly smaller to ensure stability.

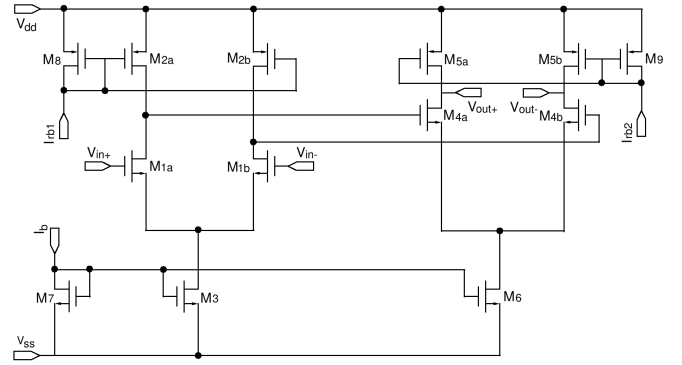


Fig. 5. Schematic diagram of the transimpedance amplifier

The CMGC cell must be transparent for small signals and must have a low noise contribution when enabled. A Gilbert cell cannot be used in this work because the attenuation of the cell depends on the threshold voltage. The proposed CMGC cell is shown in figure 6. This is a replica of the TIA with a variable transimpedance resistance, which employs variable current division to attenuate the input signal.

The replica only contributes to the noise when it is enabled, allowing small signals passing through with a large signal-to-noise ratio (SNR). When the replica is enabled the equivalent input noise contribution becomes:

$$\overline{d_{eq,in}^2} = \frac{4kT}{R_{fb,var}} df \quad (1)$$

With $R_{fb,var}$ the variable transimpedance resistance of the replica. The noise contribution is A_V lower than a normal current divider using passive components. The noise contribution of the replica is very low, and allows very small input signals to be processed with high accuracy. The input capacitance leads to a small decrease of the bandwidth when the replica is disabled. The bandwidth increases when the transimpedance resistance of the replica is enabled.

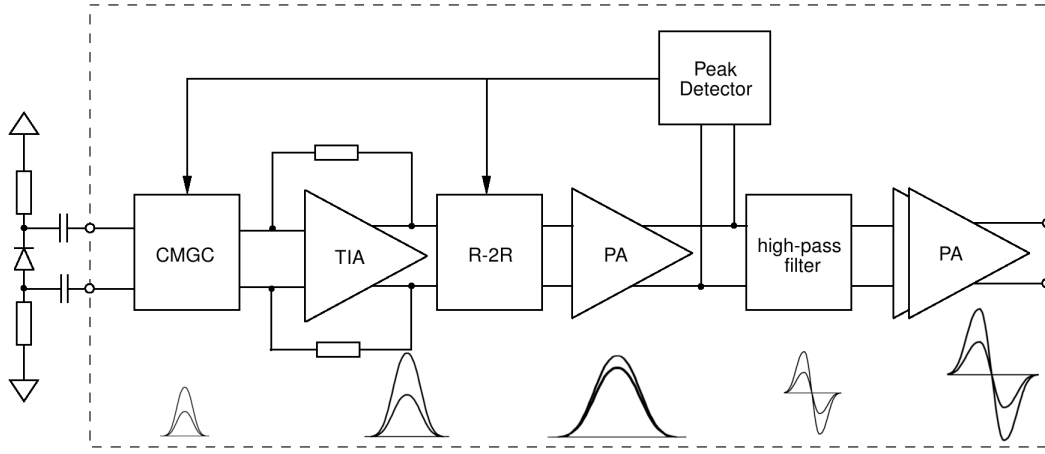


Fig. 4. Block diagram of the LIDAR receiver front-end.

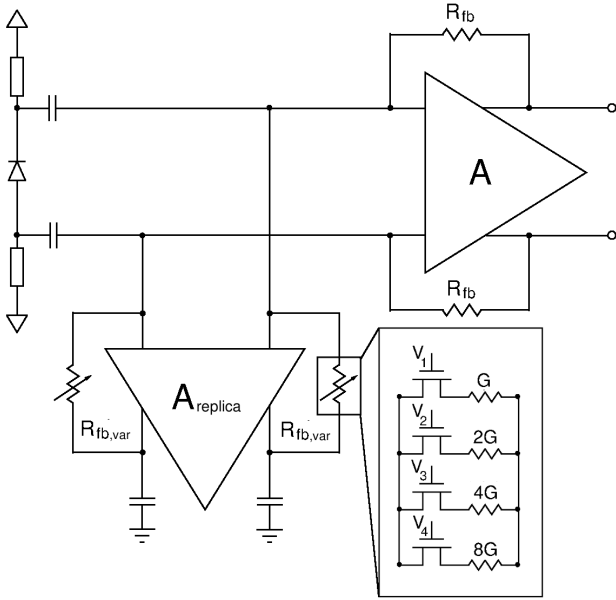


Fig. 6. Schematic diagram of replica TIA as a CMGC cell.

IV. SIMULATIONS

The design is simulated with the $0.13 \mu\text{m}$ CMOS technology of UMC. The total accumulated ionizing dose at the close environment of the MYRRHA reactor is expected to exceed 1 MGy. Temperature levels can rise to 100°C . The oxide-thickness for this technology is 2.7 nm and there is no radiation data available for this technology. The maximal threshold voltage shifts for the worst-case boundaries are extrapolated from the irradiated I/O transistors of a $0.13 \mu\text{m}$ CMOS technology with an oxide-thickness of 5 nm [4]. The results are shown in table I.

A. Steady State Behaviour

The bandwidth, phase margin and input noise of the design were simulated when the CMGC cell is disabled at a temperature of 100°C . The results are displayed in figures 7, 8 and

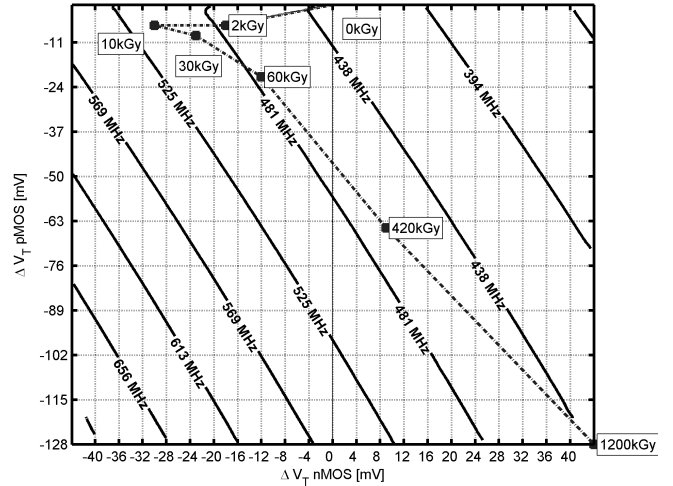


Fig. 7. Simulated bandwidth [MHz] of the receiver using the worst-case design methodology at 100°C . Also shown is the total ionizing dose corresponding a threshold voltage shift.

9.

The resulting threshold voltage shift is also indicated for different cumulative dose values. This results show that the performance of the design was not compromised by the threshold voltage shifts, with a large margin (up to 14dB) The minimal bandwidth of the receiver is 420 MHz. The phase margin always exceeds 69° . The receiver remains stable in the worst-case conditions. The maximal integrated input referred noise is about 180 nA . With a minimal SNR of 10, signals of $1.8 \mu\text{A}$ can still generate an accurate timing point.

Further observation show that the bandwidth is less sensitive to threshold voltage changes of the PMOS transistors. This means that the increase of the output resistance, due to threshold variations, is compensated by the current steering mechanism.

B. Transient Response

Figure 10 shows the transient response of the receiver for input signals with a large dynamic range and different gain

TABLE I

BOUNDARIES OF THE MAXIMAL THRESHOLD VOLTAGE SHIFTS FOR THE WORST-CASE RADIATION MODEL FOR THE 0.13 μm CMOS PROCESS TECHNOLOGY OF UMC. THE VALUES ARE EXTRAPOLATED *) FROM AN IRRADIATED 0.13 μm CMOS TECHNOLOGY (OXIDE-THICKNESS = 5 nm) [4]. ALSO SHOWN ARE THE MAXIMAL VARIATIONS OF AN IRRADIATED 0.13 μm CMOS TECHNOLOGY WITH AN OXIDE THICKNESS OF 2.2 nm [4] FOR COMPARISON.

	5 nm		2.7 nm*		2.2 nm	
	ΔV_{Tn}	ΔV_{Tp}	ΔV_{Tn}	ΔV_{Tp}	ΔV_{Tn}	ΔV_{Tp}
min.	-100 mV	-440 mV	-30 mV	-128 mV	-23 mV	-22 mV
max.	150 mV	0 mV	44 mV	0 mV	5 mV	0 mV

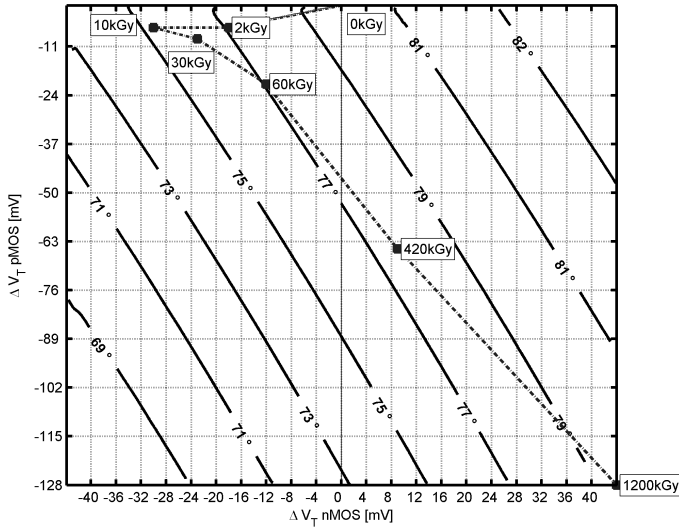


Fig. 8. Simulated phase margin [$^{\circ}$] of the receiver using the worst-case design methodology at 100°C. Also shown is the total ionizing dose corresponding a threshold voltage shift.

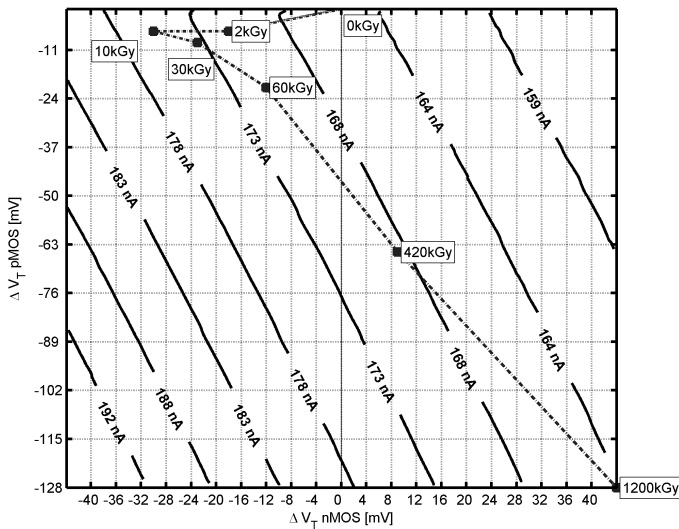


Fig. 9. Simulated input noise [nA] of the receiver using the worst-case design methodology at 100°C. Also shown is the total ionizing dose corresponding a threshold voltage shift.

settings for a temperature of 100°C and no irradiation. This set-up corresponds to the minimal bandwidth of the receiver. The maximal simulated error of the measurements due to a varying amplitude is 66 ps, which corresponds to ± 1 cm. This can be reduced to 24 ps (± 4 mm) when an offset voltage of

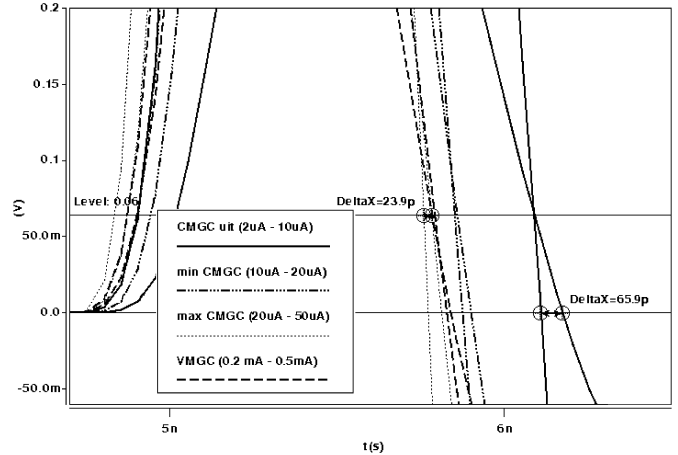


Fig. 10. Transient response of the receiver channel for different settings of the gain control.

about is 60 mV added to detect the zero crossing point.

Oversampling of the measurements increases the accuracy of the timing. This allows us to achieve mm accuracy at a kHz sample rate.

V. CONCLUSION

This work presents the radiation hard design of a low noise, 500 MHz, 0.13 μm CMOS front-end for a Light Detection And Ranging (LIDAR) receiver with mm accuracy. The design has shown a great tolerance to radiation induced threshold voltage shifts by employing a current steering compensation mechanism and a careful design topology. This is necessary due to the expected high radiation levels and temperatures in the environment of the MYRRHA reactor.

The dynamic range of the input signal was reduced by AGC. The main feature is a low noise CMGC cell, based on a replica of the low noise TIA. The common-mode output voltage of replica could for instance be used to compensate for variations in the threshold voltage.

The design was simulated using the worst-case design methodology and proved to be tolerant up to high ionizing dose levels (> 1 MGy). This design methodology used an extrapolated radiation model of the simulated processtechnology. To verify the results, the design should be irradiated with gamma rays and monitored during irradiation, with due attention for possible dose rate and other thermal or polarization related recovery phenomena. The design needs to be extended with a TDC and digital logic. The effects of SEE on digital devices should then also be modeled in the radiation model.

Our design methodology also applies to other material systems. It should also allow us to develop robust devices using strain-engineered technologies such as SiGe [10] and MuGFET [5] components, in order to further enhance the performance of the current commercial technologies.

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