

## Abstract

The European photonics market is well over 50 B€ per year. It equals the size of the micro-electronics production but shows a faster growth. Photonic Integrated Circuits, abbreviated PICs, are considered as the way to make photonic systems or subsystems cheap and ubiquitous. The share of Photonic ICs in the total Photonics market is still small, however, because the development costs of Photonic ICs are prohibitive for most applications. Recently, a novel disruptive approach in photonic integration is emerging which will reduce the R&D costs of PICs by more than an order of magnitude. This is done by developing generic integration technologies that can be applied to a broad range of applications, similar to the methodology that allowed CMOS-electronics to change the world. This approach will bring the application of PICs that integrate complex and advanced photonic functionality on a single chip within reach for a large number of small and larger companies and will initiate a breakthrough in the application of Photonic ICs.

It is the aim of the program to strengthen the position of the Dutch photonics community, both academic and industrial, by bringing about a major advance in the state-of-the-art in Photonic IC design and manufacturing by building on emerging international generic photonic foundry capabilities that combine high performance with low cost and by introducing Photonic ICs (PICs) in advanced applications. Europe is leading the generic foundry approach and our proposal will use this lead for building a novel technology sector with a large growth potential.

The program builds on the prominent position that the Dutch photonics community has obtained due to large investments in the past decades. It will use this knowledge to provide a substantial number of companies with low-cost access to leading edge photonic integration technology to increase the competitiveness of their product portfolio and expand their market share.

## **Contents**

1. *Introduction*
2. *Generic Manufacturing Technologies*
  - a. *Generic Integration Technology*
  - b. *Generic Packaging Technology*
  - c. *Software development*
3. *Applications and industrial relevance*
4. *National and international position*
5. *Goals and ambitions*
6. *Research topics and selection criteria*
7. *Knowledge transfer and utilization*
8. *Organisation of the program*

## 1. Introduction

### *The problem*

It is an interesting question why so few of the advanced Photonic ICs reported in the literature have made it to the market, despite the fact that in the last two decades several billion dollars have been invested in development of integration technologies in national and international projects in Europe, America and the Far East. The main reason is that in most cases they are too expensive to compete with other technologies like micro-optic or hybrid integration. The problem with the present approach in photonic integration technology development is that it is very closely tied to specific applications: in order to meet the specifications of the application, which are usually very challenging, the technology has to be fully optimized for that application and, as a result, we have almost as many technologies as applications. Due to this huge fragmentation the market for these specific technologies is usually too small to justify their further development into the industrial volume manufacturing process that would really lead to low chip costs. This is quite different from the situation in micro-electronics where a huge market is served by a relatively small set of integration technologies (mostly CMOS technologies), and most of the technologies are used for a wide variety of applications. In this way the development costs of the integration process are shared by a large number of applications and the volume of all applications together is sufficiently large to justify the development of a sophisticated industrial manufacturing process for large volume production, which combines high performance with low manufacturing costs.

### *The solution: generic integration technology*

the solution to the problem described above seems obvious: we should introduce to photonics the same methodology that allowed microelectronics to change the world. This can be done by shifting focus from application specific technologies that, due to their specific nature, can only serve specific markets, to **generic integration technologies** that can serve a wide variety of applications and have much better market perspectives.

In micro-electronics a broad range of functionalities is realised from a rather small set of basic building blocks, like transistors, diodes, resistors, capacitors and interconnection tracks. By connecting these building blocks in different numbers and topologies we can realize a large variety of circuits and systems, with complexities ranging from a few hundred up to over a billion transistors.

In photonics we can do something similar. On inspection of the functionality of a variety of optical circuits we see that most of them consist of a rather small set of components: lasers, optical amplifiers, modulators, detectors and passive components like couplers, filters and (de)multiplexers. By proper design these components can be reduced to an even smaller set of basic building blocks. In a generic integration technology that supports integration of the basic building blocks we can realize a variety of functionalities.

An advantage of generic integration technologies is that, because they can serve a large market, they justify the investments in developing the technology for a very high performance at the level of the basic building blocks, which will make circuits realised in this technology highly competitive. This performance will not apply for every application, of course. Just like in CMOS different classes of applications need different processes, e.g. for high-voltage, high speed, high power or low power, etc. In a similar way photonics will need a few different generic technologies, optimized for different kinds of applications, to cover a major part of all applications. But the number of basic building blocks remain small, and the number of generic technologies required is much smaller than the number of technologies which are presently in used.

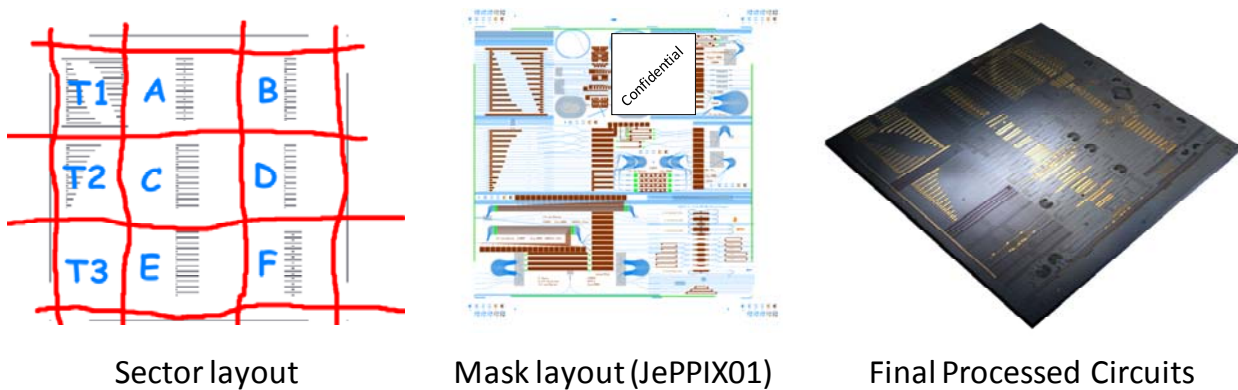
In the FP6 European Network of Excellence on Photonic Integrated Components and Circuits, ePIXnet, three major generic integration technologies were identified: InP-based integration technology, which supports the highest degree of functionality, including compact lasers and amplifiers, Silicon Photonics technology, which offers most of the functionality offered by InP except for the compact lasers and amplifiers, but at a potentially better performance and lower cost because of its compatibility with mature CMOS technology, and further a dielectric waveguide technology, which offers low-loss and high-quality passive optical functions and some thermo-optic active functions, through the full wavelength range from visible to infrared.

At present a number of national (MEMPHIS) and European projects (EuroPIC, ePIXfab, PhotonFAB, HELIOS) are running in which these three technologies are being developed for commercial foundry operation. The GTIP program aims to launch a number of projects that connect to these emerging technologies and that will provide the Netherlands with a strong position in this newly developing field, in which Europe has a clear lead over the US and the Far East.

### Cost reduction for research, development and manufacturing

the generic integration approach adopted by the epixnet platforms is expected to lead to a dramatic reduction of the costs of photonic ics and a significant reduction of the number of design cycles needed to come to a full functional device. This is mainly due to the fact that they offer access to a well characterized process, rather than to a cleanroom. A number of companies is presently offering cleanroom access to so-called fabless customers. They do process development for the customer's devices. This kind of foundry operation makes it possible to develop a product without having to build your own cleanroom, which leads to a significant cost reduction. The process development costs, which are in the range of several million euros, are still specific for the customer's product. Therefore, we call these companies 'custom foundries'. In a 'generic foundry' also the costs of the process development are shared by many users and low manufacturing costs can be realized already at small volumes. And because the generic process is used by a large number of customers it is worth the effort to create dedicated design kits with accurate models for the building blocks and powerful simulation engines, which makes it possible to obtain a working pic prototype in a very small number of design and manufacturing cycles. This will lead to a dramatic reduction of the cost of both pic r&d and manufacturing. We expect this breakthrough to happen in the next few years. And, due to cooperation that was initiated in epixnet, it will start in europe.

R&D costs can be further reduced by combining test versions from different users in a single wafer run, so that the costs of a run are shared by several users. illustrates how a number of different user designs can be combined on a single wafer. The figure at the left shows how a wafer is subdivided into 9 sectors, three for testing and six for user designs. The picture in the middle shows an actual mask design from a JePPIX Multi Project Wafer (MPW) and the picture at the right a photograph of the realised chip (before cleaving of the individual user chips and test chips. On a 3'wafer this pattern can be repeated more than 10 times. If the process batch contains 3 wafers each user will have more than 30 copies of his chip, which is usually more than sufficient for testing the design and eventually a redesign, if necessary. By sharing space in Multi-Project Wafer runs the costs of a single run can be effectively shared between a number of users. In this way the manufacturing costs for a single design iteration can be reduced below 200 € per mm<sup>2</sup> for a set of 20-30 chips, i.e. less than 10 € per mm<sup>2</sup> chip area.



**Figure 1** Example of a Multi-Project Wafer (MPW) realised in the JePPIX01 process. The wafer is subdivided in 9 sectors, three for test structures and 6 for user designs. The picture in the middle is an example of a mask layout, and at the right is a photograph of the realised chip.















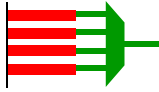

Chip manufacturing is not the only cost factor: with chip costs as low as mentioned above the costs of a module will be fully dominated by the R&D and packaging costs. R&D costs can also be strongly reduced in a generic foundry model because of the availability of a design kit with accurate models for the building blocks and a powerful simulation engine for optimizing the PIC performance prior to manufacturing. This will reduce the number of design and test cycles that are required to arrive at a chip that meets the specs. And finally, the packaging costs can be reduced by developing a generic packaging technology, in which a large number of chips can be packaged in a small number of generic packages, by standardization of positions of the electrical and optical output ports and by developing highly automated low-cost alignment and packaging technologies. In the following section the generic integration technology, packaging and software design tools will be described in more detail.

## 2. A generic foundry model

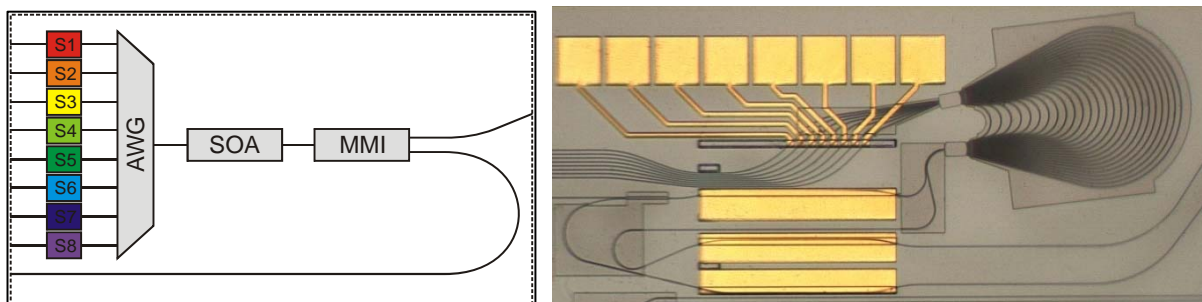
### Generic integration technology

#### Indium Phosphide

Figure 2 illustrates which functionalities can be realized in a generic Indium Phosphide technology that supports integration of four basic building blocks: passive waveguide devices (PWD), phase modulators (PHM) and Semiconductor Optical Amplifiers (SOA). With these building blocks a variety of modulators, switches and lasers can be realized. Most of the examples in 2 have been reported in the literature. 3, for example, shows a photograph of an integrated discretely tuneable laser with nanosecond switching speed, useful for packet switching applications, which has recently been developed in an experimental generic technology by the COBRA institute of the TU Eindhoven. The schematic on the left shows how the laser is composed of only two basic building blocks: passive waveguides in the MMI-coupler, the AWG demultiplexer and the interconnections, and Semiconductor Optical Amplifiers for amplification and switching.

Passive	Phase	Amplitude	Polarisation
 waveguide	 phase modulator	 optical amplifier	 polarisation converter
 curve	 amplitude modulator	 $\lambda$ converter, ultrafast switch	 pol. splitter / combiner
 MMI-coupler	 2x2 switch	 picosecond pulse laser	 pol. indep. 2x2 switch
 AWG-demux	 WDM OXC	 multiwavelength laser	 pol. indep. diff. delay line

**Figure 2** Example of the functionalities that can be realised in a generic integration technology that supports four basic building blocks: Passive Waveguide Devices, (Optical) Phase Modulators, Semiconductor Optical Amplifiers and Polarisation Converters.

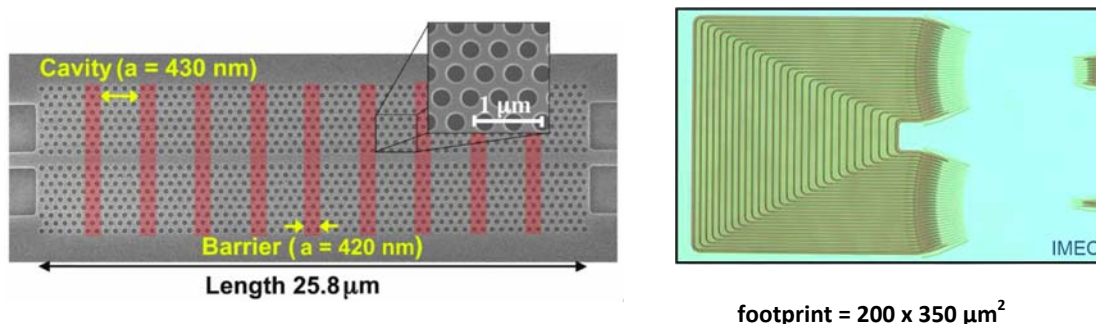


**Figure 3** Circuit scheme and microscope photograph of a fast discretely tuneable laser with 100 GHz channel spacing, which has recently been realised in the COBRA InP-based generic integration process. Chip dimensions are 1.5 x 3.5 mm<sup>2</sup>.

The InP-based generic technology platform JePPIX is supported by a consortium containing Europe's key players in the field of InP-technology: chip manufacturers (Oclaro, Heinrich Hertz Institute - Fraunhofer Gesellschaft and Philips MiPlaza), Photonic CAD companies (Photon Design, Phoenix Software and Filarete), equipment manufacturers (ASML, Aixtron and Oxford Plasma Technologies) and research institutes (COBRA and Alcatel-Thales III-V Lab). It is coordinated by COBRA - TU Eindhoven. Within the framework of the NMP-EuroPIC project and the Dutch MEMPHIS project it is working on the development of industrial generic foundry capability, including software design kits for fast and accurate chip design, and generic packaging and test facilities. Commercial photonic foundry operation is expected in or shortly after 2013. Restricted access to alpha and beta versions may start as early as 2011. Until that time the University of Eindhoven (COBRA) will provide small-scale access to its generic integration process, for research purposes (proof-of-concept, example in Figure 3).

### Silicon Photonics

The Silicon Photonics platform is presently supported by Europe's major CMOS research institutes IMEC and LETI and coordinated by the University of Gent. It offers low-cost shared access to processes for high quality silicon photonic ICs to an increasing number of customers, also from outside Europe. The technology that is currently offered comprises the realization of passive silicon waveguide components on a silicon-on-insulator waveguide platform with a silicon waveguide layer thickness of 220nm. These devices are fabricated using state-of-the-art 193nm deep UV lithography on an 8inch wafer scale. Two device examples are shown in Figure 4. The high omni-directional refractive index contrast allows to scale down the size of the integrated components dramatically. An 8 channel arrayed waveguide grating demultiplexer as shown in figure 4b can be realized on an area that is a small fraction of a mm<sup>2</sup>. While the generic technology currently mainly offers passive waveguide circuits, currently efforts are undertaken to also offer active optical functionality on the silicon waveguide platform, including high speed optical modulators and photodetectors.

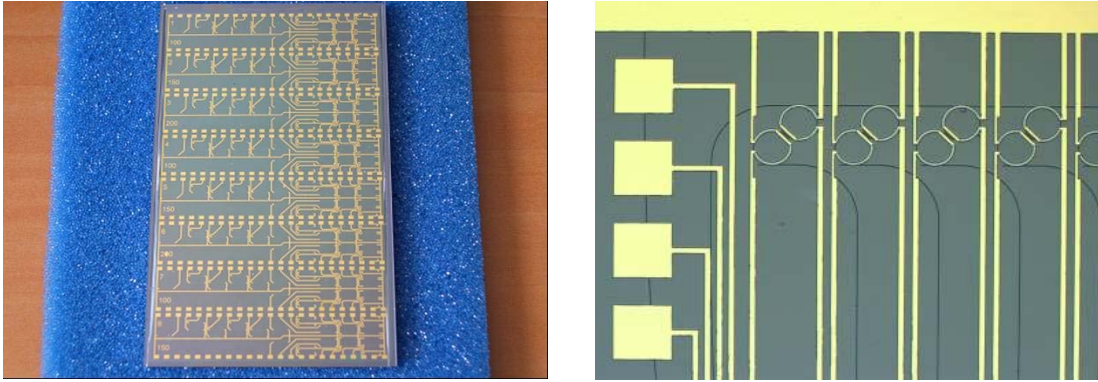


**Figure 4** Examples of circuits realised in the ePIXfab silicon-on-insulator technology platform: a complex Photonic Crystal waveguide filter with a periodically changing lattice constant (left) and an extremely compact 8-channel Arrayed\_Waveguide Grating demultiplexer with high performance.

### TriPleX

The third platform, which is supported by the Dutch company LioniX, provides access to its flexible TriPleX™ waveguide technology. TriPleX™ is a dielectric waveguide platform for Photonic ICs operating from the near UV, through visible, to far into the infrared. It supports low-loss waveguides with small polarization dependence for use in a variety of passive components, like couplers, ring-filters, Mach-Zehnders and AWG's, and it allows for integration of spot-size converters for low-loss coupling to optical fibre.

TriPleX™ is being supported by an increasing number of Europe's key players in integrated optics in a number of European research projects. In addition, several companies are commercializing different applications based on this technology. Within the framework of the Dutch Memphis project, LioniX and the Dutch software company Phoenix are currently introducing several standard components (some are depicted in figure 5) into a generic TriPleX™ library. A first call for a commercial MPW offer is envisioned in the second half of 2010.



**Figure 5** Two examples of Photonic ICs realised in the Triplex generic technology platform: a photonic True-Time Delay system for Microwave Phased Arrays Antenna's (left) and an integrated optical Add-Drop Multiplexer (right)

### Generic packaging technology

In a generic foundry approach the chip costs for smaller chips are expected to drop below 10 € already for smaller volumes if the foundry has sufficient load. With such low chip costs the total costs of a module will be dominated by the package, and the advantage of the low chip costs may be largely neutralized by the packaging costs, which is currently far too high. The reason for high packaging cost is that there is no agreed standard way of packaging of photonic chips, the variety in packaging solutions is too high. Developing a packaging technology which is both low-cost and generic is, therefore, crucial for the success of a generic foundry approach.

The key approach in generic packaging technology is to develop a small set of packages that can be used for a large number of different PICs, e.g. a package that can handle up to 40 optical IO-ports, a large number of electrical dc ports (e.g. 40) and a few rf ports (e.g. 2), and a few packages for smaller port counts. This is possible if we agree on standardization of package layouts, as well as the size and the position of both the optical and electrical ports.

The package layout requires either vertical (out-of-chip-plane) or horizontal (in-chip-plane) coupling of optical IO. In the Silicon photonics approach, for instance, grating structures are used to create out-of-chip-plane coupling. Laser or photo diodes or fibres need to be mounted in a specific angle with respect to the chip surface. This may require sub- $\mu\text{m}$  positioning and bonding precision. Advanced flip-chip technology can reach the level of a few micrometers precision, but sub- $\mu\text{m}$  precision is hard to achieve this way. In the InP material platform, coupling is usually done horizontal / in-chip-plane. Again, the spot-size requires sub- $\mu\text{m}$  alignment precision.

Optical alignment (chip-to-chip or chip-to-fibre or fibre array) is either done in a passive or an active way, or a combination of these approaches. In a passive scheme, the chips and components to be aligned are assembled together, the geometry of the mating parts determines the accuracy achieved, which is depending then on the manufacturing accuracy and the accuracy in the assembly and joining processes. In active alignment, the active optical function (e.g. the laser diode) is used to find the optimal relative position of the components by measuring the coupled light. Generally speaking, for a low cost packaging technology, passive alignment is preferred. However, the achievable precision is limited, sub- $\mu\text{m}$  levels are hard to obtain; in this perspective active alignment performs better. Of course, the combination of passive and active alignment (e.g. only some of the degrees of freedom aligned by a passive approach the others by and active approach) may provide a good balance in terms of cost and alignment performance.

As part of the research proposed in the GTIP program, a set of standardized layouts and assembly and alignment processes is aimed at. This may require the identification of classes of packages, which differ in mounting orientation, optical IO count and required alignment precision. Ideally, for each class, there must be one or a limited number of standard solutions.

For the optical ports the most important features of a standard for multi-port interfaces are the spot size of the optical ports and their pitch. Because a pitch of 250  $\mu\text{m}$  is impractical for larger port counts because of the large chip area that is lost in the coupling interface region, it is not possible to couple the chips directly to a fibre ribbon, and an interposer chip will be needed to adapt the pitch on the chip to the pitch of the fibre ribbon

(usually 250  $\mu\text{m}$  and more recently also 127  $\mu\text{m}$ ). As interposer chips we can use SHD-silica or TriPleX chips (*SHD: Super High Delta =index contrast*). These chips have the possibility for bridging a difference in spot size between the InP-PIC and the fibre. The interposer gives us, therefore, freedom in the choice of both the spot size and the pitch of the optical ports. Although it is technically possible to couple the InP waveguides directly to an interposer with a very small spot size, this is impractical because of the extremely tight tolerances required for aligning such small spots. By integrating Spot-Size converters we can enlarge the spot size of the ports, thereby increasing the alignment tolerance. Enlarging the spot size to match the fibre mode ( $\sim 10 \mu\text{m}$ ) is very difficult however. An intermediate value of 3-4  $\mu\text{m}$  seems, therefore, to be most practical. With such a spot size the pitch of the ports can be chosen as small as 25  $\mu\text{m}$ , so that 40 ports can be accommodated on a chip area with 1 mm length, which can be positioned at a convenient place, e.g. at the edge of the chip. The main problem for low-cost packaging is in passive alignment and mounting of a chip and an interposer with such a port array with an alignment precision better than 500 nm. Once we choose for an SHD silica-on-silicon or TriPleX interposer to connect an InP or Silicon chip to a fibre ribbon, we get almost for free the possibility to integrate optical functionality on the interposer, e.g. low-loss delay lines or high Q filters. Actually the combination of an InP or Silicon PIC and a dielectric interposer provides us with a hybrid platform where we can combine the strong points of both technologies (such as the low-loss features of the dielectric platform) and use the port-array as an optical bus for interconnecting the components located on the two chips.

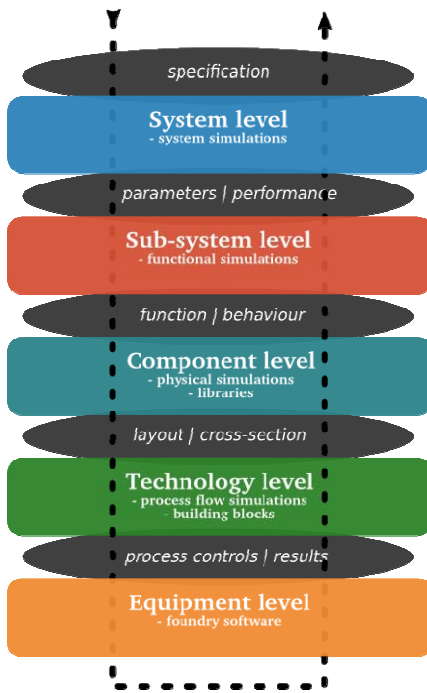
Another issue in generic packaging technology is to define approaches and standards for electrical interconnection and heat management. An InP-PIC generates heat, which must be removed in an elegant way, without affecting the alignment or the optical performance of the active optical chip. The layout of the package determines for a main part the possibilities for electrical interconnection. Electrical cross-talk is to be prevented.

In order to reach a similar level of packaging maturity as in the micro-electronics domain, effort is needed on package and packaging process reliability. Failure modes for photonic packages need to be defined and analysed. Also, procedures for failure mode analysis, on the basis of a package design and on the basis of a realized package, as well as the test procedures and equipment are to be developed. The targeted outcomes of research on generic packaging technologies within the GTIP program therefore are:

- A limited set of standard packages (layout, optical IO count, tolerance range);
- Assembly, alignment and bonding processes, as well as equipment for these processes;
- Tools for total package design, which includes design of electrical interconnections and solutions for heat management. Design guidelines are to be formulated, which can be integrated in package design software;
- Package reliability test procedures and equipment.

### **Software development**

The generic integrated technology approach means a fundamental change of working in photonic integration. For decades researchers have been developing processes in order to meet component and system requirements. Now they will have to develop photonic circuits in a 'frozen' technology release. In order to support the generic integration approach new working methods and tools need to be developed to decouple the designwork from the manufacturing technology and to bring the design of photonic integrated components at a higher abstraction level.



The design and simulation of photonic ICs can be divided into several abstraction levels as depicted in figure 6. To support the generic integration technology platforms, new software tools will especially need to address the building block or library approach and designing at ‘component level’ (functional design). Furthermore tools need to be able to cope with a wide variety of applications, resulting in co-simulation of both optical as well as other physical domains. In addition to this the development of application unspecific, and thus generic, manufacturing technologies will need support from dedicated software tools for datamanagement at the ‘technology and equipment level’ and the possibility to estimate the effects of the manufacturing tolerances on the functional performance of the photonic IC.

*Figure 6 Graphical representation of the design and simulation process. This structure is reflected in the software as abstraction layers, to decouple the system level design from the wafer processing parameters.*

### 3. Applications and industrial relevance

We expect that the large reduction of R&D time and chip manufacturing costs will lead to a large growth of the share of Photonic ICs, designed and developed in generic photonic foundry processes, in the photonic components market. So far the use of PICs has been mainly restricted to some niche areas in high-end telecom applications, where their specific functionality cannot be met by competing technologies. With the expected cost reductions through a generic foundry approach they will also become competitive in high volume markets like the telecom access network.

But when chip costs drop photonic chips will increasingly penetrate also other applications. A good example is the fibre sensor market, which amounted already 300 M\$ in 2007 with double digit annual growth figures. A significant part of the sensor costs is in the readout unit, which contains a light source, a detector and some signal processing circuitry. Here Photonic ICs can replace a significant part of the existing modules, and enable novel sensor principles. Examples are various types of strain sensors, heat sensors, biosensors and a variety of chemical sensors.

Recently research has started in applying PICs in Optical Coherence Tomography. Traditionally OCT is done in the 800 nm window, which is the preferred choice for retina diagnostics. For skin or blood vessel diagnostics 1500 nm is a better wavelength, however, because light penetrates three times deeper into the tissue due to reduced scattering losses at this wavelength. This provides good opportunities for InP PICs in OCT equipment.

Another interesting class of devices are pico or femtosecond pulse lasers. Here PICs containing mode locked lasers, optionally combined with pulse shapers, can provide small and cheap devices that can be used in widely differing applications, such as high-speed pulse generators and clock recovery circuits, ultrafast AD-converters using multiwavelength pulse trains for reducing the sampling rate with photonic serial-parallel conversion, and in multi-photon microscopy. These are just a few examples. Once Photonic ICs and their development get really cheap they will enter into many advanced products. This offers ample opportunities for small and larger companies to improve their competitiveness by applying PICs in their products.

### 4. National and international position

The GTIP program aims to make effective use of the achievements within the IOP Photonic Devices and the Smartmix MEMPHIS project, and the FP7 EU projects EuroPIC, ePIXfab, PhotonFAB and HELIOS. It builds on

the approach developed in the FP6 Network of Excellence ePIXnet ([www.epixnet.org](http://www.epixnet.org)), which has initiated development and implementation of a foundry model based on generic integration and packaging technologies. This approach has gained broad interest also in the US and the Far East, but Europe presently has a clear lead and Dutch partners are playing a prominent role in the development of this new model.

The program aligns with the NWO themes 'Use of nanoscience and technologies' and 'Kennisbasis voor ICT-toepassingen', and it is relevant for the themes 'Sustainable world' and 'New instruments for health care'. Further we expect the program to form a bridge between the Smartmix (MEMPHIS) and the IOP Photonic Devices programs and the Point-One program, where it can contribute with the introduction of photonic functionality that can overcome speed and capacity bottlenecks that are increasingly hampering progress in nanoelectronic integration.

## 5. Goals and ambitions

It is our aim to initiate a breakthrough in the application of Photonic ICs (PICs) that provide improved or novel functionality in advanced products or services to a wide range of applications, and to bring about a major advance of the state-of-the-art in Photonic IC design. This will be realized by building on emerging generic photonic foundry capabilities that combine high performance with low cost by introducing the same methodology into the field of photonics that allowed microelectronics to change our world. These foundry processes support integration of a set of basic photonic building blocks (comparable to transistors, resistors and capacitors in electronics), on the basis of which a large number of different circuits can be realised by connecting them in different circuit topologies. We expect that this approach will reduce the R&D costs of PICs dramatically by introducing the Multi-Project Wafer concept for photonic ICs. And we expect a significant reduction of the R&D time through the use of dedicated design tools, and at the same time an increased functionality level of the PICs. Finally we aim at a comparable reduction of the cost of packaging by applying the generic technology concepts also there.

## 6. Research topics and selection criteria

The GTIP program calls for research proposals addressing development of

- New building blocks or novel features in existing or emerging generic integration technologies based on InP-technology, Silicon-on-Insulator technology, and silicon oxide/nitride dielectric waveguide technology covering applications from the visible to the IR wavelength window. A criterion for an integration technology to be generic is that it supports integration of a set of basic building blocks (like couplers, filters, demultiplexers, modulators and detectors, lasers and optical amplifiers), in a standardized technology, such that a number of different designs with different functionalities can be combined in a single Multi-Project Wafer Run. Further it should support a design language, including design rules, that can be implemented in a software design kit.
- Generic packaging technology that allows for automated low-cost packaging of optical chips with standardized positions of optical and electrical input and output ports. Exploration and definition of a total package concept, from the perspective of protection and long-term stability, minimizing cross talk, and thermal-mechanical stability. Development of standards that allow for automated packaging of chips with a large variety of functionalities with a small number of different packages is part of the call. The generic packaging technologies should be applicable to a class of chips without the need of adapting the technology to the specific functionality of the chip.
- Software tools and component libraries that allow for accurate simulation of PIC-performance in the generic integration technologies and a strong reduction of the time required for designing a PIC in such a technology. Modelling of the effects of manufacturing variations on building block and PIC performance.
- Procedures and equipment for accurate and rapid testing of generic PICs or generic technology process steps. Development of methods for on-wafer testing and design-for-testability. Packaging failure mode analysis, characterisation procedures and equipment.
- Development of chips in generic technologies and their application in novel or improved products or services. Test chips should be realised or realizable (to be clearly motivated in the project plan) in Multi-Project Wafer runs.

Proposals should meet the following criteria:

- By the end of the program projects developing PICs should demonstrate their application in a prototype product or service. Projects developing technology or software should address a concrete PIC application as a vehicle.
- Proposals should connect to existing or emerging generic technology infrastructures that address the full chain from idea to application (chip modelling and design, manufacturing, packaging, characterization and testing). Isolated proposals that do not fit into such an infrastructure are not eligible.
- It is required that multiple steps in the chain are addressed in the project.

The STW GTIP call and the IOP Photonic Devices Call on Generic Integration Technologies are closely related and partially overlapping, but address complementary aspects of the generic technology development:

- STW focuses on the development of the generic technology infrastructure, and has a longer term perspective.
- IOP focuses on the applications of generic technology and has a shorter term perspective.

It is not allowed to submit the same proposal into both programs.

Proposals will be evaluated on their compliance with the GTIP focus.

## **7. Knowledge transfer and utilization**

### **Knowledge transfer**

Within each individual project a User Committee is formed that will meet at least twice a year. The scientific and technological information generated by the academic parties is transferred to the industries involved in that project in accordance with STW IP-policy rules.

The results will be protected as much as possible by patents and made public by scientific papers. Patents will be jointly owned by STW and the University. And will be made available for licensing according to the STW IP-practice.

Know-how that can be patented is expected on design-tools, processing of chips, packaging, applications etc. In the 'foundry model' the rights on processing aspects will be of primary interest of the foundries. Patented processes will by no means impede standardisation, as standardisation concerns mainly the deliverables and not the way it is manufactured. The standardisation enables (small) companies a fab-less development & marketing of systems and devices at low costs and short throughput time. Like is happening currently in micro electronics with CMOS technology. Patenting of applications (circuits) of standard components is likewise possible, in a similar way to the practise in micro electronics.

### **Kick-off and closing symposium**

The program as a whole will have a widely advertised symposium as kick-off event, which will be planned after the projects that will be granted have been selected. During that symposium, the scope of the program and the infrastructure and expertise of all partners will be presented. All of the academic and industrial teams working on this subject in The Netherlands will be invited. This will foster the (inter)national collaboration and cross fertilisation. At the end of the program a closing symposium will be organized.

The program is organized and executed in close collaboration with the IOP-Photonic Devices and other related programs, like Smart Optic Systems. Where possible joint symposia and meetings will be held in order to strengthen the network and collaboration between groups. Connection to the highly successful Photonics Event is evident.

For these activities a separate budget is made available by STW (see below).

## 8. Organisation of the program

### **Coherence**

The program focus and description is based on a workshop held in Dec 2009, with 25 participants from academic and industrial background. The background of the participants covered the whole chain of research and design to manufacturing and application.

For the guarding of the goals and coherence a Program Committee is installed by the STW-board. This committee will screen the pre-proposals and will advise the applicants on the fit of the proposal with the program. After the ranking of the full proposals by referees and a jury, the list of ranked proposals will be reviewed by the Program Committee on relevance to the program goals and on coherence. The program committee will advise the STW board on the cohesion of the ranked proposals. Based on the jury report and the Program Committee advice, the STW board will decide which of the proposals will be granted.

### **Budget**

For this call a budget of M€ 4,0 is available which must be matched by the contributions of potential technology users (companies / institutes) to a total of at least M€ 5.4. The maximum of budget that can be requested from STW is € 750.000 per project. A contribution of potential 'users' of at least 25% of the total project budget is compulsory and adds up to the requested amount.

The users do not have to co-finance up-front in the program but may contribute in-kind (materials, equipment, facilities etc.) and/or financially in the project wherein they will participate.

To realize the ambitions and cohesion of the program a budget of k€ 70 for conferences, workshops and events will be reserved at the program level. This funding will be made available by the STW board upon advice of the program committee.

### **Who can apply**

Scientists employed by Dutch universities or institutes recognized by NWO are eligible to submit a (pre) proposal (see OTP-guidelines of STW for eligibility criteria). Since GTIP is a multidisciplinary program, projects where multiple steps in the chain from chip modelling and design to characterization and testing are addressed, are required.

### **Proposals and selection**

The selection of proposals will be done in two steps: a call for pre-proposals and an invitation to the applicants of pre-proposals to submit full proposals. The pre-proposals will be evaluated by the program committee. The STW board will decide on the funding of the full proposals.

The main criteria for assessment whether a specific project application fits within the program are:

- The project should build on generic integration technologies developed in national and European projects.
- The photonic ICs should be realizable on multi-project wafers
- The project should address multiple steps in the chain from chip modelling and design to characterization and testing.

### **Funding**

Project grants will cover:

- personnel costs (including PhD and postdoc researchers, technical assistants and programmers)
- material costs (including national travel costs)
- international travel costs
- costs for equipment

The institution(s) of the applicant(s) ensure(s) the required infrastructure, the supervision and the fitting into the research program of the research institute. STW may verify this with the dean or the executive board of the institute.

The expertise required for the research must be available at the requesting institute(s), so that external consultants will not be necessary. When foreign universities and institutes that cannot apply for STW-funding (e.g. TNO) are involved in the program, these parties take care of their own funding.

### **How to submit?**

In order to minimize the time needed for writing and evaluating the proposals, it is compulsory to submit a preliminary proposal. All pre-proposals must be written in accordance with the formal guidelines that can be found in the call for pre-proposals. Only pre-proposals written in English and in accordance with the guidelines will be accepted for evaluation. **Pre-proposals should be sent to STW via Iris (on-line electronic submission system of STW). Pre-proposals should be submitted to STW before Tuesday March 23, 2010 at 12.00 a.m.** Pre-proposals submitted after this deadline will not be accepted.

### **Pre-proposals**

Pre-proposals should contain a short description (3 A4) of the proposed research, utilization paragraph and estimated budget. The proposal should make clear which potential users will contribute to the project. Support letters are optional for the pre-proposals but can be included (letters of intent are accepted).

The pre-proposals will be ranked by the program board on the basis of how well they fit within the scope of the program. The members of the program board will first assess the pre-proposals individually before discussing them plenary in the board. The program board will advise the applicants 1) to submit a full proposal or 2) to adjust the proposal so that it would fit better into the program or 3) not to enter the subsequent selection procedure.

### **Full Proposals**

Full proposals must consist of a detailed description of the expected results, planning of the research and a utilization paragraph. The utilization paragraph should include the important industrial challenges that will be solved, the time frame to implementation and the expected bottle-necks during the implementation. Companies and institutes, which will potentially contribute, should be involved bottom-up during the preparation of the proposal.

A full proposal will be evaluated only if it is preceded by a pre-proposal.

The scientific quality and the utilization perspective of the full proposals will be evaluated individually by peer review. An independent jury of about eight (inter)national experts of universities and industry (applicants will be excluded) will rank the full proposals. Each jury member will give 3 marks for each proposal: one for scientific quality, one for utilization potential and one for the strategic fit within the program. The marks will be averaged with equal weight to one final score for the proposal which determines the ranking. In addition to the ranking by the jury the program committee will formulate an advice on the cohesion between the project proposals and their relevance for the program. The decision of the STW board will be based on the ranking by the jury and the advice of the program committee.

The guidelines for full proposals are based on the 'Open Technology Program (OTP)' with as main difference that the potential technology users (companies/institutes) should contribute for at least 25% of the total project costs. The proposals should therefore be accompanied by a 'letter of participation' in which the contribution has been made explicit and in which details are given on what, when and how these contributions will be made available. For more details see: 'richtlijnen voor het Open Technologieprogramma' ([www.stw.nl](http://www.stw.nl)).

## **Assessment and selection criteria**

Upon receiving a pre-proposal STW will decide on its admission (eligibility criteria). The program committee will assess the strategic fit within the research program and its topics. Each individual program committee member will give a mark for the strategic fit for each proposal. Then, in a plenary session the program committee will discuss all pre-proposals and formulate an advice to the applicants. This advice can be: 1) to submit a full proposal or 2) to adjust the proposal so that it would better fit into the program or 3) not to enter the subsequent selection procedure.

The program committee will evaluate the fit of the pre-proposals within the framework of the program and will use the following considerations:

- How well do the goals of the project fit within the ambitions of the program. Do the expected results meet the industrial needs in the long term (2014-2018)?
- To what extent does the proposal fit within the research topics of the program?
- Does the program strengthen the Photonic Integration expertise in The Netherlands in general and of the participants in the project in particular?
- To which extent is the project proposal multidisciplinary? What are the positive effects from the interdisciplinary cooperation? How is interaction in between researchers and between university and industry organized?
- Do the proposals overlap each other and if so, what are the consequences for the funding?

Full proposals will be evaluated by peer review on scientific quality and utilization potential.

### Scientific quality

- Originality and innovative character of the proposal
- Contribution to the aims of the Perspectief program
- Expected impact on the scientific community
- Research method
- Time schedule
- Budget
- Infrastructure

### Utilization

- Potential economic impact
- Past performance in utilization by the applicants
- Contribution to the development of applied knowledge and aims of the program
- Impact on utilization if the project is carried out successfully
- Different steps needed (time path) to utilize the results
- Chance on patents and/or know how agreements
- Participation of users

The jury will be asked to assess the proposals on these aspects and also on the strategic fit within the program.

### **Time schedule GTIP proposals**

Call for pre-proposals open	Wednesday February 10, 2010
Deadline pre-proposals	Tuesday March 23, 2010, 12.00 a.m.
Notification to applicants pre-proposal of the positive/negative advice to submit full proposal	Monday April 12, 2010
Deadline full proposals	Tuesday June 8, 2010, 12.00 a.m.
Start review by experts	Monday July 5, 2010
Protocol sent to applicants	Monday August 23, 2010
Deadline comments applicants	Monday September 6, 2010
Ranking by jury ready	Monday October 11, 2010
Advice Program Committee to STW board ready	Friday October 15, 2010
Decision by STW board on funding + notification to applicants	Friday October 22, 2010

### **Program Committee**

Prof.dr.ir. M.K. Smit (program leader), COBRA, TU Eindhoven  
Dr.ir. M. Tichem, Fac. Mechanical, Maritime & Materials Eng., Dept. PME, TU Delft  
Dr. B.H. Verbeek, chairman IOP Photonics, SenterNovem, The Hague  
Dr.ir. R.G. Heideman, LioniX BV, Enschede  
Dr.ir. W. Hoving, XiO Photonics BV, Enschede  
Dr.ing. M. van der Hoek, VanderHoekPhotonics, Vlaardingen  
Ir. T. Korthorst, Phoenix BV, Enschede  
Dr. M. Wale, Oclaro, Caswell, United Kingdom  
Dr.ir. G. Roelkens, IMEC, Leuven, Belgium  
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*This document has been compiled by STW on the basis of aforementioned workshop of dec'09, and the inputs of: Meint Smit (TU/e), Marcel Tichem (3ME), Rene Heideman (Lionix), Willem Hoving (Xio-photonix), Gunter Roelkens (IMEC/Uni-Gent), Twan Korthorst (Phoenix), Bart Verbeek (IOP-PD), Frank van den Berg (STW) and Hans d'Achard (STW) d.d. 2010, 19 January.*