

The Effect Of Non-Idealities In CMOS Chopper Amplifiers

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Abstract— This paper presents theory and simulations of non-idealities in the input chopper of a CMOS chopper amplifier, which causes residual offset. Because this can be in the order of 10 to 100 μV , a better understanding of these non-idealities is required for the design of CMOS amplifiers with sub-microvolt offset. The simulations were done with the SPECTRE simulation tool, using transistor models taken from a 0.7 μm CMOS process. The results show that mismatch in the input chopper itself is not negligible, and that its layout should be made with extreme care to reduce capacitive mismatch.

Keywords— Choppers, charge injection, CMOS, offset cancellation

I. INTRODUCTION

In CMOS circuit design, offset and $1/f$ noise are issues that circuit designers have to deal with. If an application requires an offset voltage lower than 1mV, trimming or dynamic offset cancellation techniques such as auto zeroing or chopping should be applied. These techniques are discussed in [1,2].

It is known that dynamic offset cancellation circuits still have a residual offset in the order of 1 to 100 μV . In the case of chopper amplifiers there should ideally not be any residual offset, since the switches themselves do not have offset. But due to the switches' charge injection some residual offset will remain.

In an ideal differential chopper amplifier, charge injection should have no influence, since the switches of the input chopper inject the same amount of charge on both inputs. However in non-ideal cases, component mismatch causes differences in the charge injected, which then gives rise to residual offset.

This paper is organized as follows. First the simulated circuit and simulation parameters are presented in section II. Next the simulation results are shown in

section III. And the paper ends with conclusions in section IV.

II. MODEL

A. Circuit

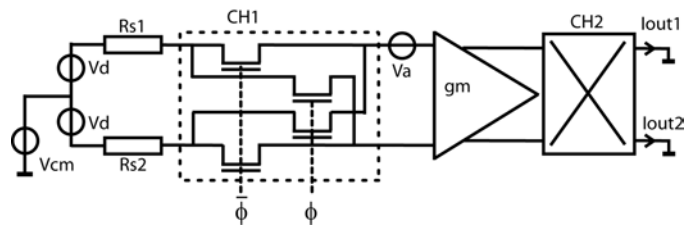


Figure 1: the simulation circuit of the input chopper.

In figure 1 the block diagram of a chopper amplifier is shown. The input chopper CH1 consists of four cross-coupled NMOS transistors ($W=1.2\mu\text{m}$ and $L=0.7\mu\text{m}$) and the output chopper CH2 consists of ideal switches. These switches are not shown in figure 1, because non-idealities in the output chopper are not considered in this paper. The gm stage is modeled as shown in figure 2.

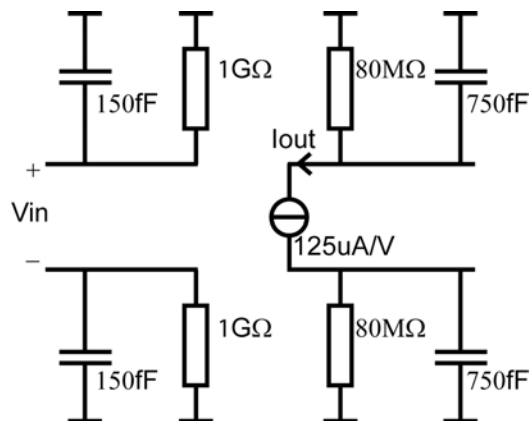


Figure 2: gm model

The mismatch capacitors C_{m1} and C_{m2} of the input chopper are shown in figure 3. These are not physical capacitances, but they model differences in the capacitance between the clock lines and the input and output of the chopper. They are placed in parallel with the parasitic capacitances of one of the chopper transistors.

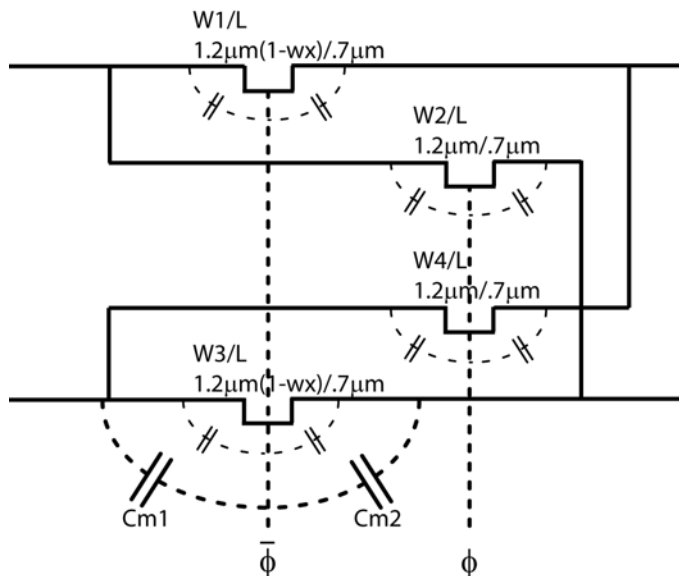


Figure 3: the non-ideal chopper

B. Parameters

Five parameters are varied during the simulations.

V_{cm} is the common mode voltage at the input of the amplifier (figure 1).

C_{m1} is the capacitive mismatch of CH1 towards the source (figure 3).

C_{m2} is the capacitive mismatch of CH1 towards the gm-stage (figure 3).

V_a the offset of the gm stage i.e. the offset that should be reduced by the chopper (figure 1).

And w_x is the mismatch between the chopper CH1 transistors. The mismatch w_x modulates the width of the two chopper transistors as follows: $W1=1.2(1-w_x)\mu m$ and $W3=1.2(1+w_x)\mu m$. We will only simulate the mismatch between $W1$ and $W3$, $W2=W4=1.2\mu m$.

The graphs in this paper are composed of multiple simulations in which one parameter is varied. If not stated otherwise, the other parameters are zero. And $R_{s1}=R_{s2}=10k\Omega$ in all simulations.

C. Simulation method

Each simulation consists of a 10 ms transient simulation, using a 10kHz clock to drive the choppers, with a rise and fall time of 1 ps, and amplitude of 5V.

The simulator tool derives the average of the output current difference ($I_{out1} - I_{out2}$) over the 10 ms time period. From this current average and the gm of the amplifier the referred input offset voltage is calculated.

III. SIMULATIONS

In the ideal case the circuit should exhibit no offset. The “ideal” case is simulated with all parameters equal to zero and $R_{s1} = R_{s2} = 10k\Omega$. For this simulation the referred offset voltage is 2.7592aV. So it can be concluded that in the ideal case, the average offset is essentially equal to zero.

For the frequency versus offset simulation presented in figure 4, the parameters are $w_x=0.1$ and $V_{cm}=1V$, and for the duty-cycle versus offset simulation shown in figure 5, the parameters are $w_x=0.1$, $V_{cm}=1V$ and $V_a=8mV$.

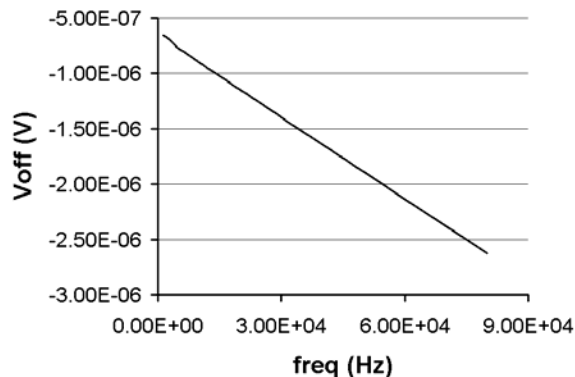


Figure 4: The input referred Voff versus the frequency

The known linear relationship between frequency and residual offset described in [3] and the linear relationship between duty cycle and residual offset are in agreement with the simulation results shown in figures 4 and 5.

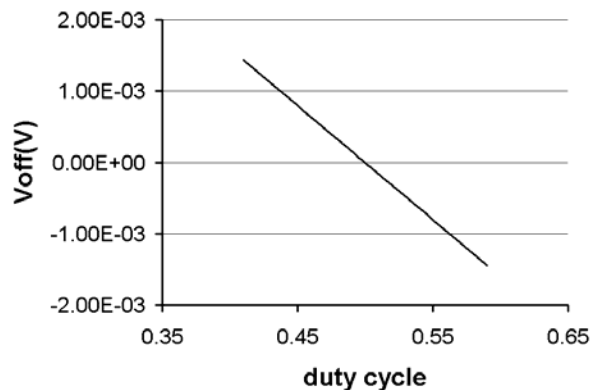


Figure 5: The input referred Voff versus the duty-cycle

Figure 6 and 7 show the results of the simulations with a varying common mode voltage. With all other parameters zero, V_{cm} does not have an influence. But from figure 6 it can be seen that the common mode voltage in combination with a transistor (switch) mismatch introduces a non-linear contribution to the referred offset.

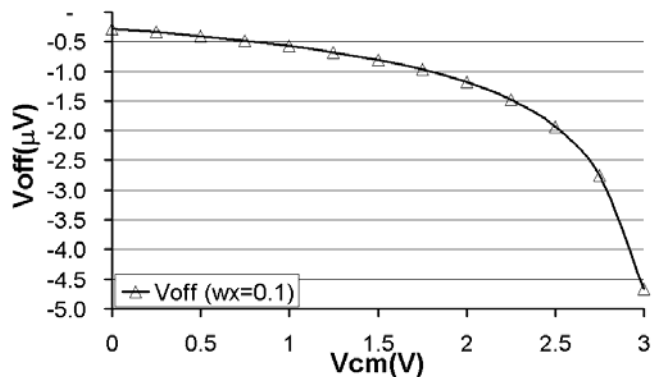


Figure 6: The input referred V_{off} versus the common-mode voltage V_{cm} with transistor mismatch.

This non-linear behavior is caused because the overdrive voltage of the NMOS transistors is decreased by increasing V_{cm} . Therefore the differences between channel charge injection and R_{on} between the unequal transistors are increased, causing more residual offset.

From figure 7 we can see that the mismatch capacitance from clock to the gm input, C_{m2} , has more influence than the mismatch capacitance from clock to input source, C_{m1} .

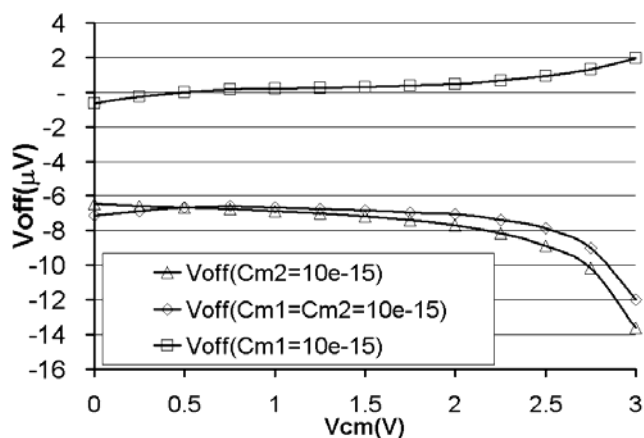


Figure 7: The input referred V_{off} versus the common-mode voltage V_{cm} with capacitance mismatch.

This can be explained by examining the circuit of figure 1. The mismatch capacitor C_{m2} (caused by asymmetric layout or process spread) from the input

chopper CH1 to the amplifier, gives rise to spikes at the amplifiers input. The output chopper CH2 will demodulate these spikes, thus creating a DC offset error.

Spikes caused by the mismatch capacitor C_{m1} from the input chopper CH1 to the input source will be chopped by the input chopper CH1 and by the output chopper CH2, and will therefore cause spikes, but ideally no DC error. So C_{m1} will contribute less to the referred input offset.

In figure 8, the input referred offset is shown as a function of the capacitive mismatch from the chopper to the input source C_{m1} . It can be seen that in this case the common mode voltage V_{cm} has more influence on the offset behavior than the transistor mismatch w_x .

It can also be seen that the influence of the mismatch capacitance is significant if it is of the same order as, or larger than, the parasitic capacitance of the chopper switch itself. This can be explained by assuming that a transistor opens and closes in different ways when a common mode voltage is applied over its source and drain. This means that the spike caused by the opening of a transistor does not cancel the spike caused by the closing transistor. And because the two input lines have a slight mismatch this causes a DC error.

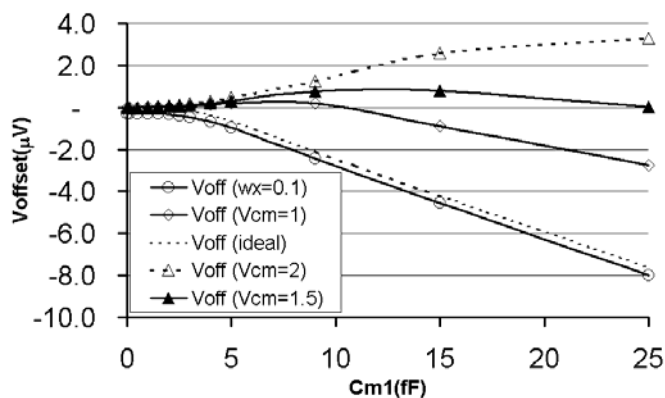


Figure 8: The input referred V_{off} versus the capacitive mismatch from clock line to input source C_{m1}

From figure 9, we can see that there is a linear relation between the capacitive mismatch from chopper to amplifier and the referred offset. The influence of the common mode voltage is smaller than in the case of the capacitive mismatch from chopper to input (as shown in figure 8).

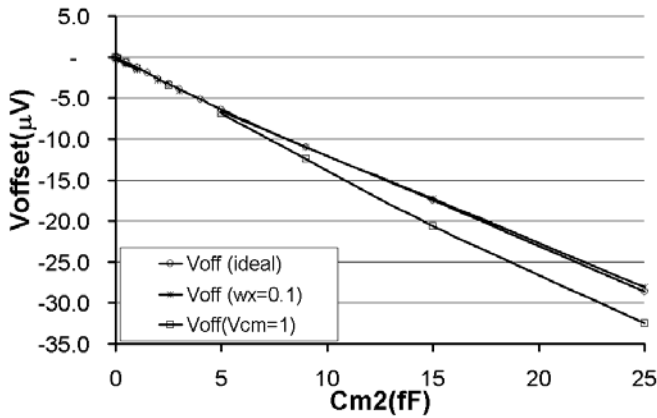


Figure 9: The input referred Voff versus the capacitive mismatch from chopper to amplifier input Cm2

In figure 10, we can see that Vcm modulates the offset caused by chopper transistor mismatch wx. When the mismatch of the chopper transistors increases the offset increases.

The increasing mismatch of two chopper transistors increases the mismatch of the ON-resistances, parasitic capacitances and channel charge injection. These three effects cause offset.

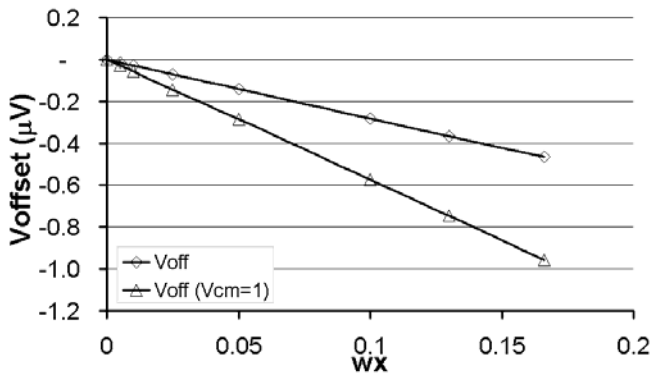


Figure 10: The input referred Voff versus the transistor mismatch wx

IV. CONCLUSIONS

The simulations done in this paper are hard to validate with measurements, because process spread inherently cannot be controlled. However some rules of thumb concept can be derived from these simulation results.

1. The parasitic mismatch capacitor from chopper to the amplifier is the largest contributor to the residual offset.

2. The parasitic mismatch capacitance from the

chopper to the input source is also of importance.

This means that a symmetrically layout of bond pads, chopper and amplifier is necessary to avoid these mismatch capacitances.

3. Mismatch between the chopper transistors can cause residual offset. So choppers should have a compact symmetrical layout in order to minimize the mismatch.

V. ACKNOWLEDGEMENTS

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