CMOS Receiver Frontends for mm-Wave Short Range Gigabit Communication

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Keywords— *mm-Wave, 60GHz, LNA, Downconversion, Broadband, Gigabit, Short Range Communication.*

Abstract—**Implicit in the design of a mm-wave receiver front-end is the requirement for broadband amplification and gain flatness in order to support advanced modulation schemes and assure design robustness. As seen from lower frequency wireless systems, the choice of technology often dictates the system architecture. While either silicon CMOS or silicon BiCMOS technology could be used for implementation, cost, availability, performance and time to market constraints typically dictate the technology choice. The common result is the use of CMOS technology due its low cost and high integrability with other system blocks. In this paper an alternative approach for the implementation of the preamplifier, by using a distributed topology, is proposed. While this topology is not common in wireless design due to its many drawbacks. Modifications are proposed that trade off unused bandwidth for better performance, while allowing more design flexibility and robustness. Next the downconversion is reviewed with respect to the constraint that deep sub-micron technology imposes. The methods used to overcome these difficulties do not reside only in circuit but also in system design. Architectures such as the heterodyne receiver , may be attractive for mm-Wave communication systems allowing us to minimize the circuit dimension and ease the demands on circuit performance.**

I. Introduction

Continued scale down of CMOS technology allows RFIC designers to exploit the unlicensed 7GHz of free spectrum around 60GHz. The proposed 802.15.3c standard for short-range, gigabit/s communication in the unlicensed bands at 60GHz may be used an adapter for any gigabit/s data source or sink requiring a short-range wireless link. The spectral allocations vary with region as shown in the following table.

TABLE I
Unlicensed Bands

Region	Unlicensed Band
USA	$57-64\ GHz$
Europe and Japan	$59-66\ GHz$

The small physical size of passive circuit elements at mm-wave frequencies enables more cost-effective integration of distributed elements such as antennas or baluns. A second benefit of mm-wave operation is immunity to interference due to attenuation (see Fig. 1) of the transmitted signal at 60GHz caused by absorption of the RF energy by oxygen (O_2). This natural immunity to interferers can relax the demand on the front-end circuit linearity, thereby conserving current and power consumption. Early demonstrations of 60GHz communication transceivers used silicon bipolar devices in an advanced BiCMOS technology [2,3]. However, CMOS examples of 60GHz receiver front-ends in both $0.13\mu m$ [4–6] and 90nm [7] technologies have also been reported. The potential for lower cost and higher integration (e.g., higher packing density for digital circuits at the latest CMOS technology node) for CMOS relative to BiCMOS make it the preferred technology for a consumer application. With deep sub-micron CMOS devices now offering transit frequencies well above 100GHz, there is a strong motivation to focus research in this area on CMOS implementations. However, the choice of technology also influences the eventual transceiver architecture, because many of the common receiver architectures cannot be implemented effectively in all technologies. This aspect is reviewed in Section IV of this paper. This

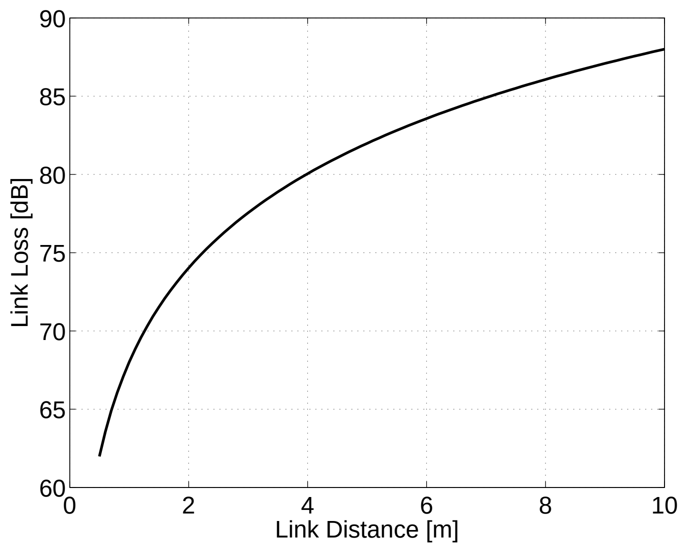

Fig. 1. 60GHz Link loss according to Friisṕrediction for an isotropic radiator and receiver [1]

paper is focused on the topology of the front-end (i.e. LNA and mixer) within the context of a broadband design.

II. Low Noise amplifiers

Gain flatness is necessity when employing advanced modulation schemes such as OFDM. The preamplifier's bandwidth, which, for covering the entire 60GHz band implies a quasi-broadband circuit.

$$\frac{f_{center}}{Bandwidth} = \frac{61GHz}{7GHz} < 10.$$

Bandwidth Enhancement of commonly used topologies is the common approach used. The required bandwidth can then be achieved in several ways

- Frequency Peaking
- Weak Interstage Coupling
- Feedback

The cascode circuit, which is commonly used as an LNA for lower frequency exhibits a high interstage parasitic capacitance which degrades its performance, both bandwidth and noise wise. Applying inductive peaking [8] (see Fig. 2) at the interstage connection, improves the performance of the circuit. Another factor is the Miller effect ,which depends upon the ratio between g_m to c_{gd}. At microwave frequencies this ratio is very small, however, at 60GHz $c_{gd} \approx 10fF$ and $g_m \approx 10m\mho$, which makes suppression of Miller effect relatively poor. Furthermore, shifting the interstage pole by a inductive peaking requires a low-Q inductor to realize a wide bandwidth, which degrades the noise performance. Also the circuit is very sensitive to device parameter variation, which may lead to a lower yield.

Distributed Amplifiers (DA) are excellent candidates to be used as preamplifiers for a 60GHz applications due to their inherent broad bandwidth. This class of amplifiers can operate from DC to the mm-wave frequency band with a relatively flat gain. Designers often avoid distributed topologies due to their many disadvantages, such as, relatively high current consumption, poor noise performance, design complexity and low overall efficiency. However, the 60GHz band specifications require operation over 7GHz of bandwidth and not the entire spectrum, and therefore a trade-off can be made between operating bandwidth and other aspects of the amplifier's performance.

A common source (CS) topology for a DA is shown in Fig 3. The amplifier consists of three CS stages which are distributed along a transmission line (TRL) at the input and at the output. The size of the amplifier can be significantly reduced for operation at the 60GHz band due to the small dimensions of the TRL (on chip $\lambda < 2.5mm$), as a consequence the parasitics of the passive components are also reduced. Furthermore, the accuracy of TRL models is much higher than on-chip inductor models, which leads to a successful design with less fab runs.

To tradeoff the bandwidth for gain we examine the gain expression for CS-DA given in [9]

$$G = \frac{g_m^2 Z_d Z_g}{4}\left[e^{\gamma_g l_g - N\gamma_d l_d}\sum_{n=1}^{N} e^{-n(\gamma_g l_g - \gamma_d l_d)}\right]^2, \quad (1)$$

where Zd and Zg are the drain and gate transmission line characteristic impedances, respectively, γ_d and γ_g are the respective drain and gate line propagation coefficients, l_d and l_g are the drain and gate line lengths, g_m is the transistor transconductance and N is the number of gain stages (i.e., 3 in Fig 3).

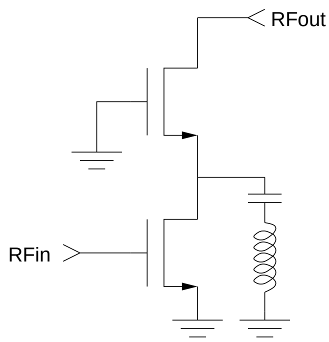

Fig. 2. Cascode stage with a shunt peaking inductor

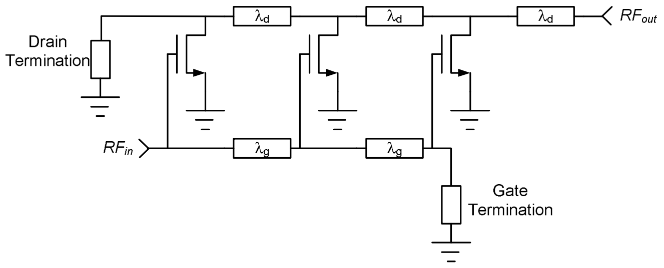

Fig. 3. Distributed Amplifier based on common-source stages

An example of this topology is presented in [10], where the current consumption is 132mA for a gain of 8dB. Examining equation (1), one can observe that the gain is reduced by a factor of 4 due to drain current which flows away from the output (i.e., towards the termination). Replacing the output line termination with a TRL (e.g., close to $\lambda/4$), can produce a higher impedance at the termination, and more current will flow toward the load. The expression for the gain becomes

$$G = g_m^2 Z_d Z_g \cdot \left[e^{\gamma_g l_g - N\gamma_d l_d} \sum_{n=1}^{N} \frac{Z_{T_n}}{Z_{T_n} + Z_d} e^{-n(\gamma_g l_g - \gamma_d l_d)} \right]^2 . \tag{2}$$

As seen from equation (2), the current flowing toward the load is now double the previous result, giving a 6dB increase in the in-band gain (see Fig. 4). The gain in the vicinity of 60GHz is 6dB higher, however, the amplifier bandwidth is now narrower by an order of magnitude.

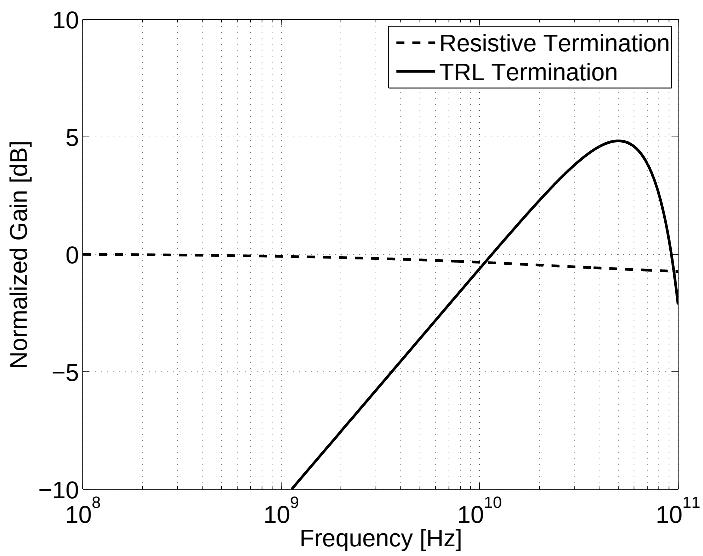

Fig. 4. The Normalized gain of a CS-DA compared with a modified DA with a TRL termination

The resistive gate termination, which contributes to the relatively poor noise performance (e.g., noise figure) can also be replaced by a TRL termination. Another option is to replace it by an active device (e.g., a common-source stage with feedback, or a common-gate stage), where the amplifier input impedance provides a broadband termination for the input (i.e.,gate) transmission line. This approach is also band-limited, which as mentioned before is not a problem for a 60GHz LNA.

III. A modified DA

Combining all the aforementioned modifications, and changing the topology to a CS stage driving a common gate (CG) distributed stage (see Fig. 5) a modified DA is obtained. The reason behind the topology change is the reduction of power consumption, the current consumption is now of standard cascode circuit, where CG stage current is distributed between its stages and allows the use of smaller area devices, which reduces the parasitic capacitance. Furthermore, the distributed CG stage exhibit a constant input impedance in the desired frequency band and thus a constant gain (see Fig. 6).The active termination of the input TRL prevents the degradation of the noise performance of the amplifier, and maintains it constant over the band.

The gain and bandwidth tradeoff of the amplifier can be controlled by the termination of the input TRL. Thus the design is less sensitive to parameter variation of the active devices. The design's passive components consist only of TRL which can be well modeled and assure good simulation and measurement matching.

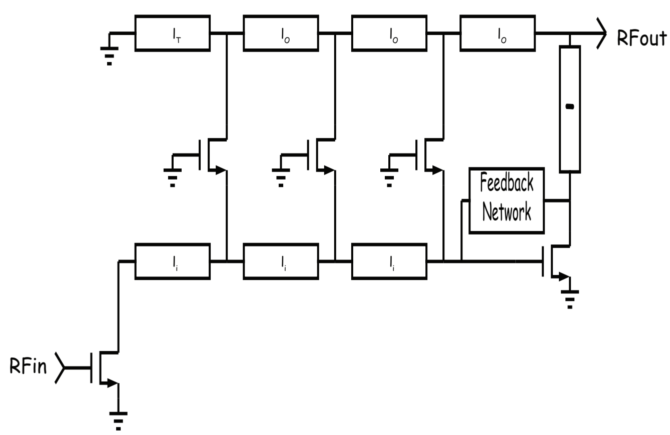

Fig. 5. A cascode amplifier with a distributed common gate stage allows to reduce the power consumption and maintain flat gain over the desired band.

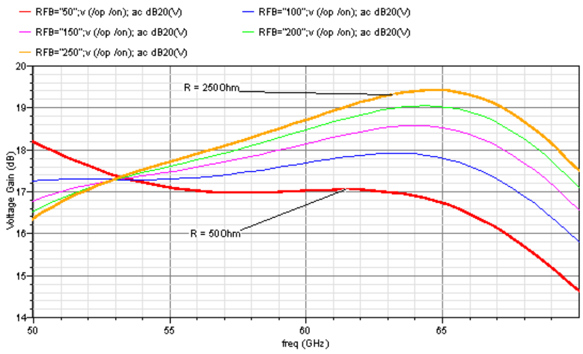

Fig. 6. The Normalized gain of a CS-DA compared with a modified DA with a TRL termination

IV. Downconversion

Implementation of circuits at mm-wave frequencies requires short-channel (CMOS). These devices pose a limitation on the supply voltage (e.g., 0.9-1.2V for 65-90nm CMOS). Another constraint imposed by a low-voltage supply is circuit linearity, which affects the ability of the receiver to operate properly when interfering signals are present. A logical choice for the mixer topology is the simple switching quad, as shown in Fig. 7. The mixer can be operate as a passive (i.e., resistive) mixer if no drain-source bias voltage is applied (i.e., VDS = 0V), or it may be biased if more conversion gain is required. This circuit is commonly used as an RF mixer in both CMOS and other technologies.

However, for deep submicron technologies operating at high frequency, there is a large difference in mixer noise performance between the 2 technologies. The 1/f noise produced by small- geometry CMOS devices is typically much higher than for a bipolar device, where the 1/f noise corner frequency may be as high as 1GHz for a gate width of a few microns at gate lengths of $0.13\mu m$ and below.

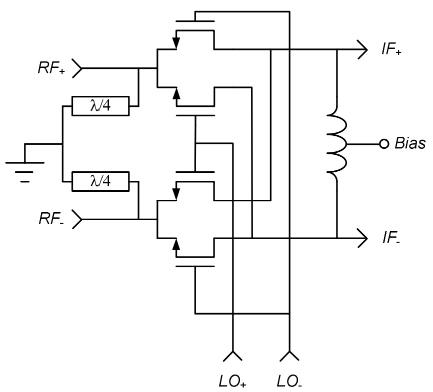

Fig. 7. A Switching Quad mixer

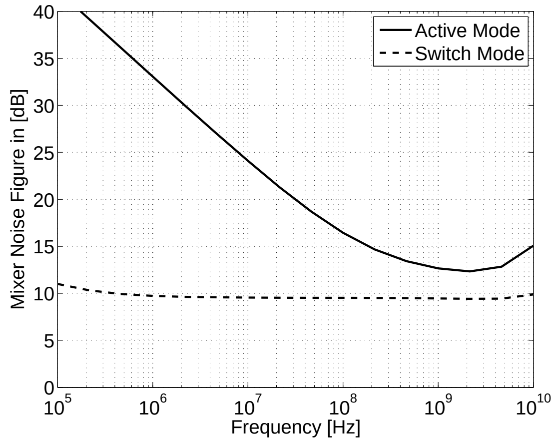

Fig. 8. Simulated mixer noise figure for active and passive mode CMOS mixers. Since CMOS technology is often preferable (cost and density-wise), the mixer trade-off between mixer noise performance and conversion gain at baseband must be addressed at the system design level, which will be discussed in the following section

Considering a single conversion receiver, the poor noise performance of the mixer can affect the receiver performance. In Fig. 8, the simulated noise figure (NF) of a switching mixer implemented in 90nm technology, with $7.5\mu m/90$nm devices, is plotted. It can be seen from the figure that the noise figure when the transistors are biased in the active mode is much larger than for the passive mixer up to about 1GHz, which precludes its use in a low IF receiver.

An alternative approach is to use a double downconversion architecture (sliding IF system). Heterodyne system are not commonly used in RFIC design due to the difficulties of the IF filter passive components, which are extremely large due to the low frequency and consume extra chip area or extra pads for using external components. However, for a $60GHz$ system, the IF is also located in the mm-wave band, for example choosing a $40GHz$ LO places the the IF at $20GHz$, the second source is obtained by division of the high LO and thus the quadrature phases are gained, freeing the designer from the use of a polyphase filter. If filtering is needed the the center frequency is at $20Ghz$, which allows the use of relatively small passive components saving costly real estate. In this scenario the first mixer can be biased to allow easier downconversion since the IF is well above the 1/f corner and the second mixer can be operated as passive, also a large swing is easier to obtain at $20GHz$. Such a system can be seen in Fig. 9, and was demonstrated in [7].

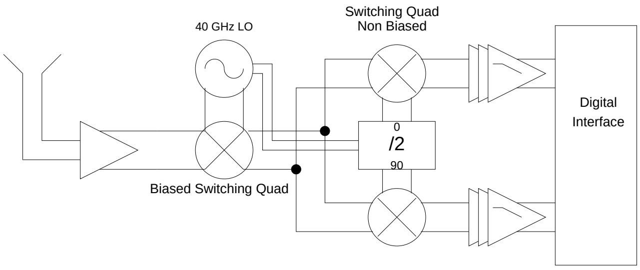

Fig. 9. Simulated mixer noise figure for active and passive mode CMOS mixers. Since CMOS technology is often preferable (cost and density-wise), the mixer trade-off between mixer noise performance and conversion gain at baseband must be addressed at the system design level, which will be discussed in the following section

V. Conclusions

Standard narrow-band amplifier topologies should be replaced by a broadband topology in order to make maximum use of the spectrum available at 60GHz and to support advanced modulation schemes such as OFDM. Acknowledging that passive components are not modeled well in VLSI silicon technologies at these (and other) frequencies (e.g., due to substrate losses), a fully-differential topology reduces the risk of implementation at the cost of increased power consumption. Also, simple passive structures, such as transmission lines, are physically small on-chip at mm-wave and show reduced parameter variation when driven differentially. Furthermore common receiver architectures must also evolve in order to overcome devices inherent difficulties.

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