

# Reduction of alloying temperature of metallization stacks containing Al/Ti/TiN from 400 to 300°C

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**Abstract** — In this work we have investigated, by means of electrical measurements on n+p junctions the Ti and TiN interface to implanted Si when the Si-metal alloying is performed either at 400°C or 300°C. It has been demonstrated that, in the case of Ti, the reduction of the alloying temperature to 300°C significantly benefits to the quality of the contact, while the 400°C alloying has detrimental effects on it. Differently, the TiN contacts have shown to be improved in the same extent by the above alloyings.

**Index Term** — Aluminium-silicon alloying, titanium, titanium nitride, ultra-shallow junction, junction leakage.

## I. INTRODUCTION

In conventional Si IC technology, one of the most commonly used metallization schemes involves the physical vapour deposition (PVD) of Al/Si(1%) layer followed by a thermal alloying step in forming gas. This alloying is usually performed at temperatures in the range of 400-500 °C and is mainly aimed at H-passivating the oxide-to-Si interface and dissolving any native oxide at Al-to-Si interface in order to minimize the contact resistance. The saturation of the Al with a small content of Si (usually 1-2%) is necessary to prevent Al spiking into the Si during the alloying [1]. Indeed at 400-500°C Si diffuses into pure Al forming deep holes at the surface (Fig. 1), which are filled in by the Al itself. These Al spikes cause the short-circuit of junctions that are of about the same depth as the holes into Si.

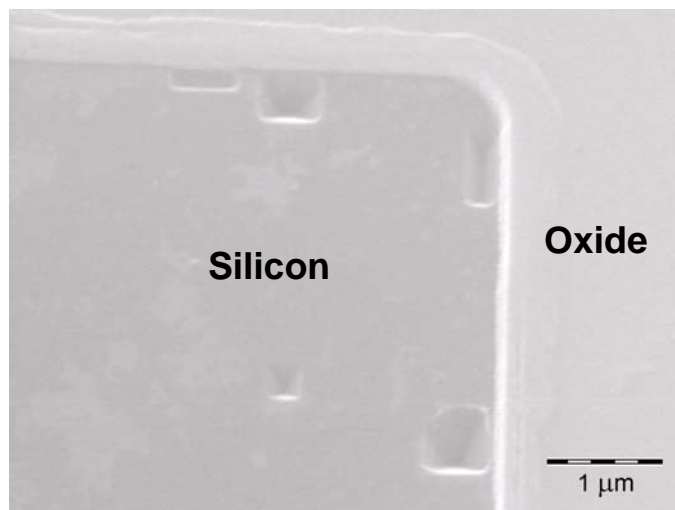


Fig. 1. SEM image of the Si surface metalized with pure Al and alloyed at 400°C for 30 min, after removing metal. Deep holes into Si are clearly visible, especially in the corners.

On the other hand, the presence of Si atoms into the Al layer results in the formation of Si-precipitates (Fig. 2) when the metal cools down after the alloying. These relatively large Si clusters increase the metal layer resistivity and enhance electromigration mechanisms. Especially in the case of submicron sized contacts, this issue is a serious problem. A possible and largely used solution is to interpose Ti/TiN barriers between Si and Al. In fact, they block the Si diffusion into the Al besides being electromigration-proof conductive layers.

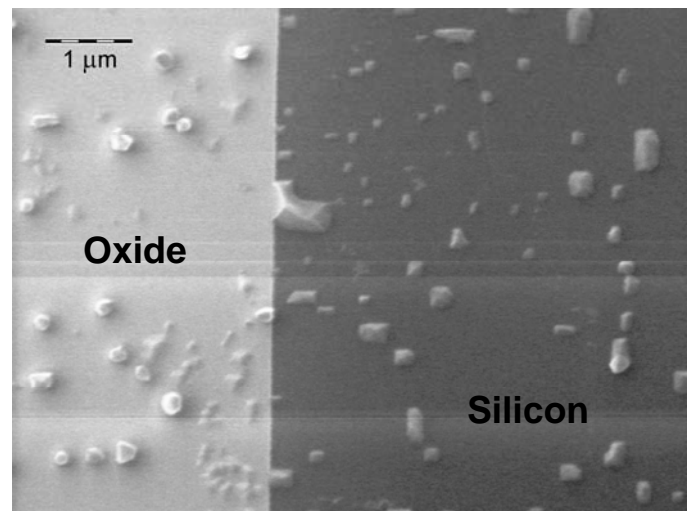


Fig. 2. SEM image of the Si surface, metalized with Al/Si(1%) and alloyed at 400°C for 30 min, after removing metal. Si-precipitates are present all over the surface.

Moreover, due to their propriety to form a low leakage Schottky junction on p-type silicon (Fig. 3), Ti and TiN have potential application in some advanced bipolar transistor designs, the so called NPM's [1], which have been predicted to give enhanced performance in terms of speed. These innovative transistors could be easily fabricated in back-wafer-contacted SOG bipolar technology [3][4][5], which is a substrate transfer process where the Si wafer is glued to glass. In such a process, schematically illustrated in Fig. 4, Ti or TiN would be used to form the back-side Schottky collector contacts (Fig. 4) and thus the Si-to-Ti or Si-to-TiN interface could not be alloyed at the normal alloying temperatures since the integrity of the glue limits the back-wafer processing temperature to below 300°C.

However, whether or not there are process restrictions on the alloying temperature, the use of Ti or TiN, instead of the

standard Al/Si(1%), as interface metal to Si poses the question of knowing the effect on the contact quality of a certain alloying.

In view of that, in this work we have investigated, by means of electrical measurements on  $n^+p$  junctions, the Ti and TiN interface to implanted Si when the alloying process is performed either at 400°C or 300°C.

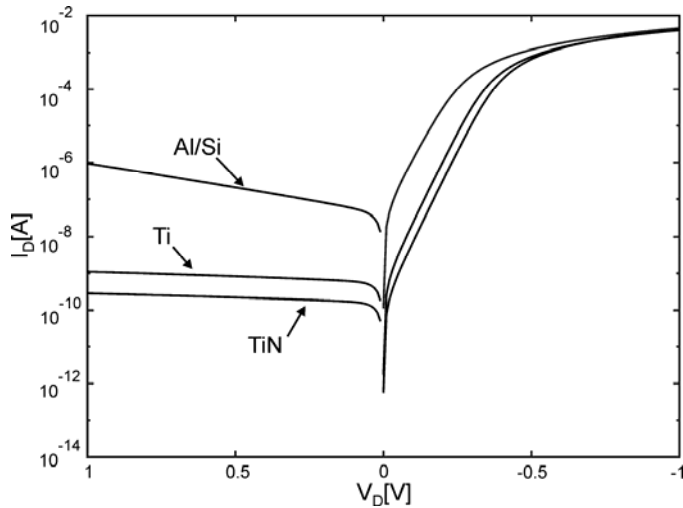


Fig. 3. I-V characteristics of p-Schottky diodes for different metals. The contact area is  $40 \times 1 \mu\text{m}^2$ .

## II. EXPERIMENTAL MATERIAL

The fabrication process of the samples used in our investigation is very straightforward. Starting from a p-type Si substrate, we deposit 400 nm of LPCVD TEOS and on top of it 100 nm of Al/Si(1%) is sputtered. Afterwards, the contact windows are plasma-etched and implanted with high-dose 5 keV  $7^\circ$  tilted As implants. Just before the implantation the native oxide at Si interface is removed by 15 sec BHF 1:7 dip etch. The implants are then activated by high-power excimer laser annealing as illustrated in Fig. 5a. The 100 nm Al/Si(1%) layer works as reflective mask for the laser and thus only the contact window is laser-annealed. The resulting  $n^+$  region is about 20-30 nm deep and self-aligned to the contact.

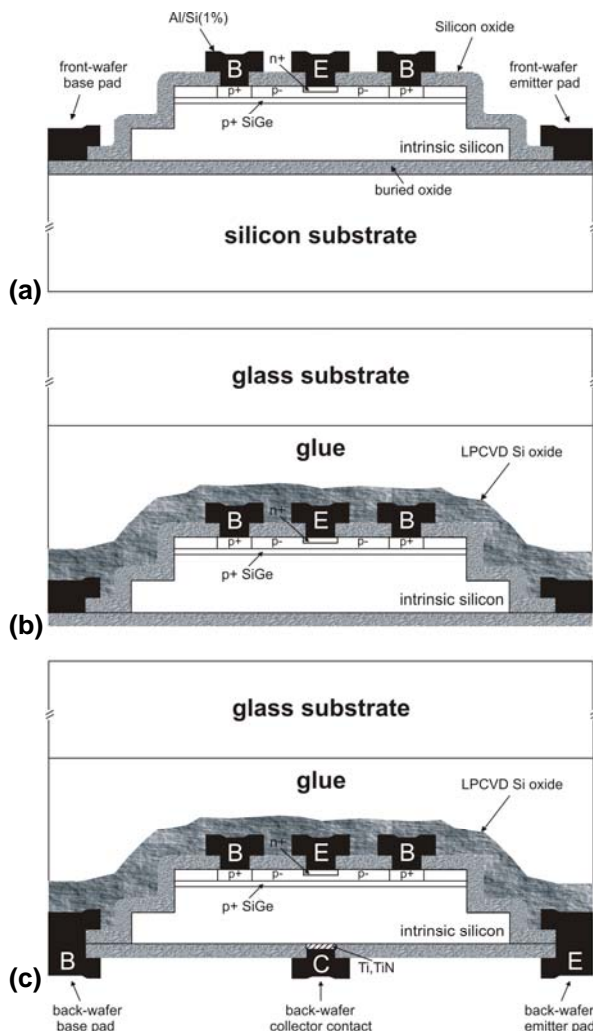


Fig. 4. SOG SiGe NPM bipolar process: (a) front-wafer process, (b) substrate transfer, (c) back-wafer process.

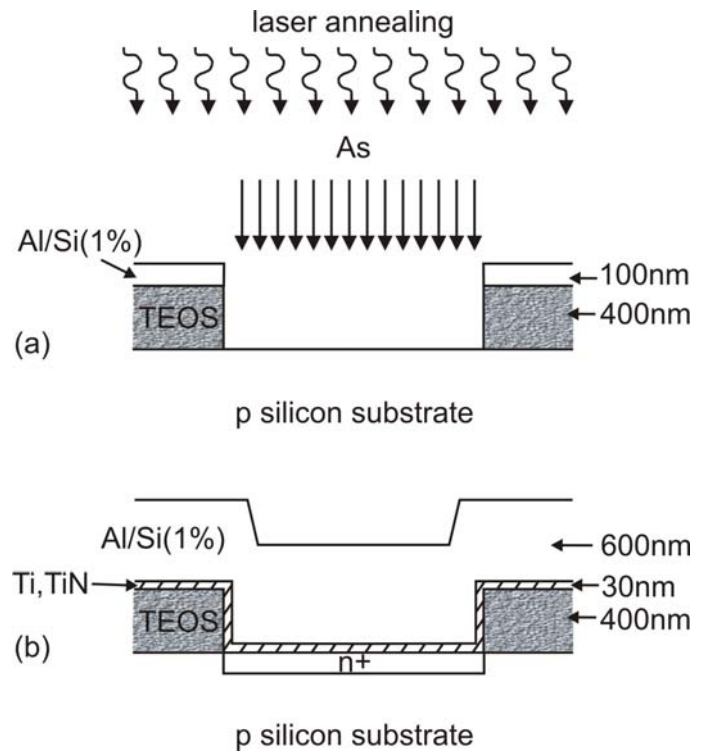


Fig. 5. (a) Implantation and laser annealing, and (b) metallization of the contact windows.

The wafers are then ready to be metallized. Just before the metallization, they are dipped in 0.55% HF for 4 min to remove any native oxide at the Si interface. During this dip etch, the 100 nm Al/Si(1%) layer is removed as well. The metallization is done by sputtering at 280°C 30nm of either Ti or TiN, capped by 600nm Al/Si(1%) layer (Fig. 5b). The latter is also used to metalize the back side of the wafer. The front wafer metal is then patterned and each wafer is halved. The two halves are alloyed in  $\text{N}_2\text{-H}_2(10\%)$  flowing gas, one at 300°C for 3 hours and the other for 30 minutes at 400°C.

### III. ELECTRICAL MEASUREMENTS

We have performed DC electrical measurements on the fabricated samples before and after the alloying step. Specifically, we have used the back-wafer contact as ground contact and measured the I-V characteristics of the front-wafer n<sup>+</sup>p junctions in forward and reverse mode. The results are shown in Figs. 6 and 7 for Ti and TiN, respectively. The analyzed samples have been implanted with the same As dose (10<sup>15</sup>cm<sup>-2</sup>) and laser annealed with the same energy (750mJ/cm<sup>2</sup>).

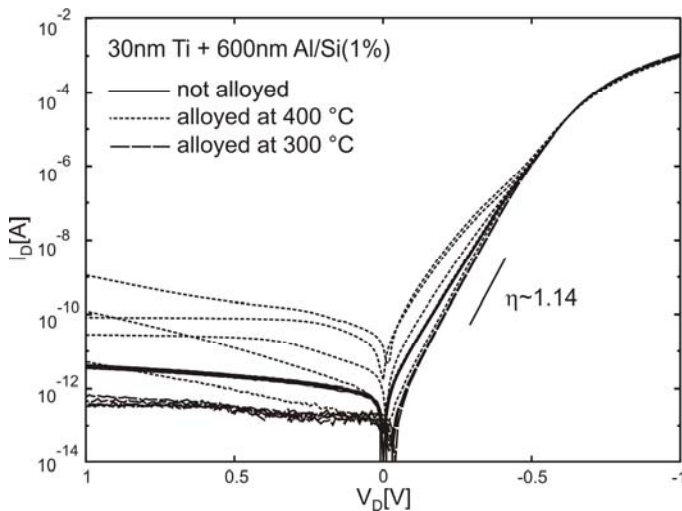


Fig. 6. I-V characteristics of implanted and laser annealed n<sup>+</sup>p junction contacted with 30nm Ti + 600nm Al/Si(1%). The contact area is 40x1 μm<sup>2</sup>.

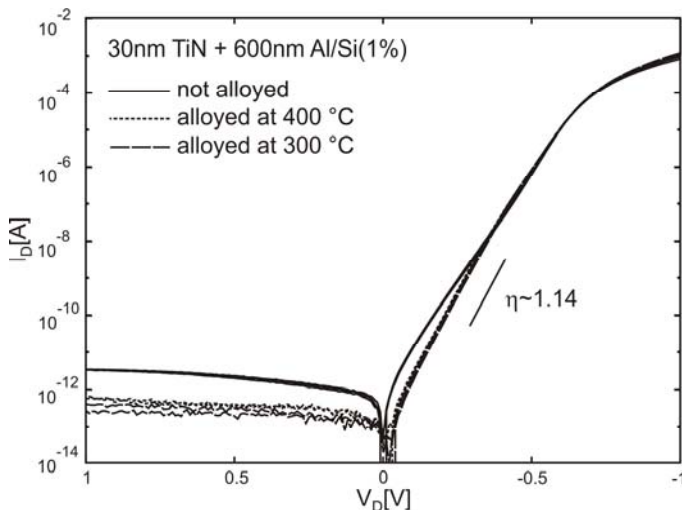


Fig. 7. I-V characteristics of implanted and laser annealed n<sup>+</sup>p diodes contacted with 30nm TiN + 600nm Al/Si(1%). The contact area is 40x1 μm<sup>2</sup>.

### IV. DISCUSSION

Due to the ultra-shalowness and the self-alignment to the contact of the n<sup>+</sup> regions, the measured n<sup>+</sup>p diodes are electrically very sensitive to defects or any kind of damage,

like for instance metal spikes, that might be present at Si-to-metal interface, especially in the corners of the contact. Indeed the more ruined the interface, the higher the leakage in I-V characteristics.

The solid lines in Figs. 6 and 7 indicate that, before the alloying step, the two types of contact have the same good interface to Si since the I-V curves are identical and with low leakage. The 300°C alloying improves significantly the quality of the contact to Si of both Ti and TiN layers (see the dashed lines in Figs. 6 and 7) since the reverse leakage drops of about one order of magnitude and the ideality factor in forward mode becomes reasonably good (η≈1.14) also in the low-voltage region.

Instead the effect of the 400°C alloying is very different on the two types of sample (see dotted lines in Figs. 6 and 7). The devices with TiN do not show any deterioration of the interface since the junction leakage remains as low as after the 300°C alloying. Differently, the I-V characteristics of the samples with Ti reveal an increased leakage. Moreover, in most of them this deterioration is so significant that the leakage is even higher than before the alloying. This clearly indicates that during the 400°C alloying a reaction between Ti and Si [6] has occurred at the interface which has created generation-recombination centres at the corners of the contact windows.

### V. CONCLUSIONS

We have investigated Ti and TiN contacts to implanted and laser annealed Si surface when alloyed either at 400°C or 300°C. Using the I-V characteristics of ultra shallow n<sup>+</sup>p junctions we have demonstrated that, in the case of Ti, the reduction of the alloying temperature to 300°C significantly improves the quality of the contact. We have also proved that the 400°C alloying is detrimental in the sense that it creates defects in the corners of implanted contacts. Instead, the TiN contacts have shown to benefit in the same extent from the alloying steps at 400°C and 300°C.

Further investigations are necessary to characterize the impact of the alloying temperature on the contact resistance and the layer thickness versus series resistance trade-off in order to efficiently use the Ti and TiN as contacting metals for advanced submicron devices.

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