Application of spacer hard-masks for sub-100 nm wide silicon fin-etching

Vladimir Jovanović, Silvana Milosvaljević, Lis K. Nanver, and Tomislav Suligoj

Abstract—**The use of spacers as a hard mask allows the wafer patterning in sub-100 nm range without the use of lithography tools with such high resolution. The patterned line width is determined by the thickness of the deposited spacer material and subsequent etching steps. The conformal deposition of the spacer material with precise thickness control is required for narrow spacer processing. Additionally, the sacrificial island and spacer etching steps need to be highly anisotropic. Silicon oxide and nitride layers deposited by LPCVD were examined for island/spacer combinations for silicon fin-etching. Excellent selectivity of buffered-HF solutions to silicon and silicon nitride makes silicon oxide the preferred island material. Consequently, silicon nitride was used for the spacers. The silicon nitride spacers with widths of 100 nm, 50 nm, and 30 nm were processed and used as a hard mask for silicon etching. Reactive-ion etching with HBr/Cl_2 chemistry achieved high silicon fins with sloped sidewalls. Wet silicon etching in 25% TMAH done on <110> wafers created vertical silicon fins with smooth sidewalls. Both processes resulted in silicon fins with high aspect-ratio.**

***Index Terms*—silicon fin, spacer, TMAH**

I. Introduction

THE advance of silicon devices is in strong relation with decrease in their size. Device speed depends on the distances over which the charge is transported, with designers trying to decrease these distances to achieve higher speeds. The lateral current flow of the CMOS devices means that their performance is determined by the layout dimensions, gate length in particular [1]. Additionally, new device concepts, such as FinFET, require patterning of dimensions smaller than 100 nm [3]. To investigate the advanced CMOS devices, it is necessary to be able to achieve these small dimensions. The lithography tools needed to pattern dimensions in the sub-100 nm range are often prohibitively expensive (e.g. wafer steppers) or slow (e.g. electron beam systems) for university laboratories [2]. However, spacers can be used as a hard-mask instead of lithography processing. This allows the patterning of structures with lateral dimensions determined by the thickness of deposited layer, rather than the resolution limits of the lithography tools.

Manuscript received June 29, 2006. This work was supported by European Network of Excellence SINANO under the Sixth EU Framework Programme.
Vladimir Jovanović is with ECTM-DIMES, Delft University of Technology P.O. BOX 5053, 2600 GB Delft, The Netherlands, on leave from the Faculty of Electrical Engineering and Computing, University of Zagreb, Unska 3, 10000 Zagreb, Croatia. (phone: +31 (0)15 27 82185; fax: +31 (0)15 26 22163; e-mail: v.jovanovic@dimes.tudelft.nl).

Silvana Milosvaljević and Lis K. Nanver are with ECTM-DIMES, Delft University of Technology, P.O. BOX 5053, 2600 GB Delft, The Netherlands.

Tomislav Suligoj is with the Faculty of Electrical Engineering and Computing, University of Zagreb, Unska 3, 10000 Zagreb, Croatia.

With the scaling of CMOS devices, FinFETs have been suggested as a possible candidate to replace the bulk silicon MOSFETs for future technology nodes [4]. The performance of FinFETs depends on the thin silicon walls (fins) where the intrinsic device is formed, with requirement for thin fins with good sidewall quality. The spacers have already been used in FinFETs as a hard-mask for silicon etching [5] with devices demonstrated.

The work in this paper presents processing for the formation of the spacer hard-mask and its use for the silicon fin-etching. The lithography system with the wafer stepper was utilized. The minimum feature size of the system is 0.5 μm, but the spacer hard-masks allowed the patterning of the fins with widths below 100 nm. Silicon fin-etching was done in two ways: (i) with dry plasma etching, and (ii) wet using TMAH solution.

Section II. presents spacer the hard-mask processing with the silicon fin-etching explained in Section III. The conclusions are given in Section IV.

II. Spacer Hard-mask Processing

The starting point in spacer processing is the deposition of the sacrificial layer, depicted in Fig. 1.(b). This layer is then etched by reactive-ion etching (RIE) through its whole thickness, using a photoresist mask (Fig.1.(c)). The remaining islands of the deposited layer serve as a structure around which the spacers are later created. The next step is the conformal deposition of the spacer material, with the thickness of this layer determining the width of the hard-mask (Fig.1.(d)). The spacer layer is etched by RIE, leaving the thin layer of spacer material around the island (Fig.1.(e)). The final step in spacer formation is the removal of the sacrificial islands (Fig.1.(f)).

The spacer processing and the underlying layer etching requirements determine the possible material and etching choices for the sacrificial islands and spacers. The chosen sacrificial layer and spacer materials have to be etched with high selectivity to one another and to the underlying material. With the final goal of etching silicon fins, silicon nitride and silicon oxide are chosen as the possible candidates for the top layers.

The sacrificial layer thickness determines the height of the spacers. The spacers need to be high enough in order to be

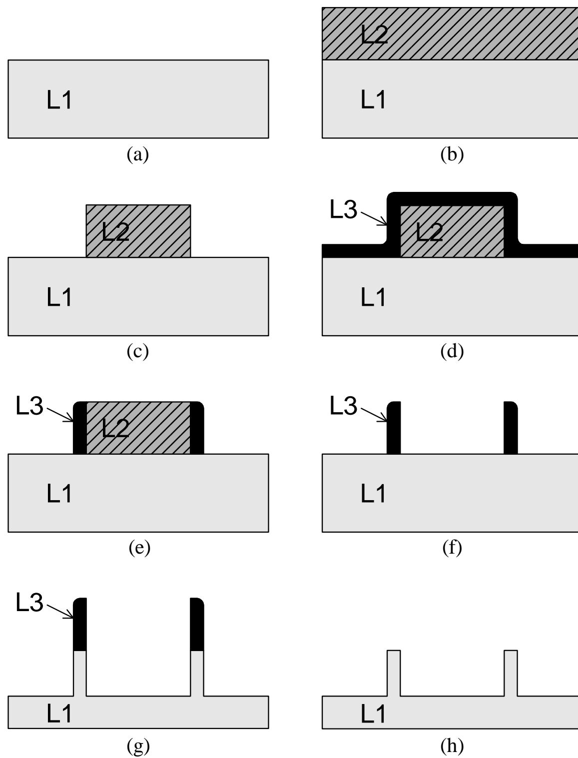

Fig. 1. Etching using the spacer hard-mask. The material L1 to be patterned (a) is covered with the sacrificial layer L2 (b). The sacrificial layer is anisotropicaly etched (c) and the spacer layer L3 is conformaly deposited (d). The spacers are created by the anisotropic etching of L3 (e) and the islands of sacrificial material L2 are then removed (f). The L1 layer is etched with spacers used as a hard-mask (g). Optionally, the spacers are also removed (h).

used as a mask for silicon etching. Therefore, the minimum sacrificial layer height is determined by the target depth of the silicon etching, and the selectivity of the silicon etching solution to the spacer material. With the goal of etching silicon fins higher than 500 nm, and with the expected high selectivity of silicon etching solutions to nitride and oxide layers, it was decided that the spacer height of 300 nm would be sufficient. To account for the possible spacer height loss during spacer layer etching (Fig.1.(e)), the sacrificial layer thickness was targeted at 500 nm. The sacrificial layer is etched using RIE to achieve good anisotropy. Ideally, the sidewalls should be vertical and the etching selectivity to silicon high.

The deposition of the spacer layer needs to be conformal to have good coverage of the island sidewalls. The spacers are etched by RIE for high anisotropy. In this way, the full thickness of the spacer material is left on the sidewall, allowing precise spacer width control. However, the deviation of the sidewall angle from the normal to the surface results in the angled spacer layer. Due to this, some spacer width is lost, even with highly anisotropic etch. Additionally, the angled spacers will shadow the bottom silicon during fin-etching, possibly increasing the fin width.

The final processing requirement is the high selectivity of the sacrificial-layer etching-solution to the spacer material and the underlying silicon. Since anisotropy is not important in this etching step, high selectivity is best achieved using the wet chemical etching.

As mentioned above, silicon nitride and silicon oxide were used to create the spacer hard-mask. Experiments were done with both combinations – nitride islands with oxide spacers and oxide islands with nitride spacers. Both materials can be conformaly deposited using the low-pressure chemical vapor deposition furnace (LPCVD), and anisotropicaly etched using the fluorine-based plasma etcher. The low-stress silicon nitride is deposited at 850°C, whereas the silicon oxide is deposited at 700°C using a TEOS source. Deposition time in the LPCVD can be precisely controlled, allowing excellent control of the deposited layer thickness. Experiments were done with the sacrificial island layer thickness of 500 nm and the spacer layer thicknesses of 100 nm, 50 nm, and 30 nm.

The results of the island removal by wet etching showed that the selectivity of the nitride etching solution was not high enough to preserve the thin oxide spacers. The ortho-phosphoric acid heated to 157°C, used to remove silicon nitride, has selectivity of roughly 6:1 to deposited oxide, resulting in significant spacer etching during island removal. On the other hand, buffered-HF solution (1:7 ratio) has excellent selectivity to both nitride and silicon. Therefore, the combination of the oxide islands with nitride spacers was chosen for the spacer hard-mask processing.

The reactive-ion etching of oxide (Fig.1.(c)) and nitride (Fig.1.(e)) were done in the fluorine-based plasma etcher Drytek Triode 384T. The nitride etching in this machine has low selectivity to oxide and silicon, and the precise process timing is required to avoid significant loss of underlying material. The selectivity of the oxide etching is approximately 10:1 to silicon, resulting in small silicon loss during island etching. This loss is of little importance, since that part of the silicon would be removed in the fin-etching step. Fig. 2. shows the scanning electron microscopy (SEM) image of the nitride spacers processed from the 30 nm thick nitride layer. The measured height of 436 nm shows the height loss from the 500 nm tall oxide islands, which can be attributed to the nitride overetching.

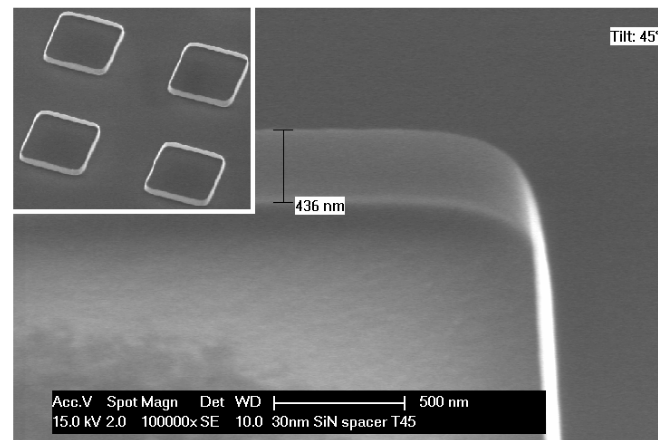

Fig. 2. SEM image of silicon nitride spacer obtained by deposition and subsequent anisotropic etch of 30 nm thick low-stress silicon nitride. Inset in the top-left corner shows a part of a field of spacers.

III. SILICON FIN-ETCHING

The nitride spacer hard-mask was used to etch thin silicon fins. Reactive-ion etching of silicon was performed in two different plasma etchers: (i) the fluorine-based plasma etcher Drytek Triode 384T, also used for oxide and nitride etching, and (ii) Trikon Omega 201 plasma etcher utilizing a combination of hydrogen-bromide (HBr) and chlorine gases (Cl_2). Additionally, wet silicon etching was done using tetramethylammonium-hydroxide (TMAH). The target depth for the silicon etching steps was 700 nm, which would make the fin aspect-ratio very high. Since the goal of the experiments was to show applicability of the spacer hard-mask for silicon fin-etching, the etching depth was not strictly controlled.

The fluorine-based RIE of silicon resulted in significant silicon undercutting, with silicon being completely etched through below the narrow spacer hard-mask. The etching in HBr/Cl_2 plasma system gave significantly better results, producing high silicon fins, as shown in Fig.3. The nitride spacers effectively masked silicon during etching and no undercutting below the hard-mask can be observed. The silicon-fin height of approximately 1.1 µm is higher than the targeted value, due to the inaccurate etching-rate data used for process timing. However, the additional fin height only proves the masking capability of the thin nitride spacers. The sidewalls of the silicon fins are at an angle to the wafer surface. Even with highly anisotropic plasma etching, the sidewall angle is not expected to be at 90° to the surface. Such profiles are typical for fin devices where fins are etched by RIE [5]-[7]. The achieved aspect ratio of approximately 6.3:1 is much higher than typical aspect ratios in FinFETs, making our process suitable for devices with very high current per single fin.

Crystallographic wet-etching of silicon with TMAH has also been used for FinFET processing [9], [10]. The etching in TMAH requires a nitride or oxide hard-mask, making it suitable for our nitride spacer hard-mask application. The silicon etch rate in TMAH is much higher for <110> and <100> crystal planes than <111> plane (Table I). The etching rate increases with higher TMAH concentrations and higher solution temperatures. More importantly, the etching-rate ratio of <111> crystal plane to other planes decreases, improving the etching anisotropy.

Silicon wafers with <110> orientation of the crystal cube at the wafer surface were used in experiments. The <111> plane is normal to the surface and parallel with the primary flat on these wafers. With the nitride hard-mask aligned in parallel to the primary flat, TMAH etching exposes these planes, leaving silicon fins with <111> sidewalls. The silicon etching with the nitride spacer hard-mask was performed in 25% TMAH solution heated to 85°C. The resulting fins are shown in Figs. 4. and 5. High selectivity of TMAH to different crystal orientations leaves nearly vertical silicon fins with smooth sidewalls. The fin width is determined by the nitride spacer width at the silicon interface without the influence of the spacer angle to the initial silicon surface. Different to the RIE fin-profiles, TMAH etching gives almost constant fin width along fin height. This allows more accurate device design compared to the case with varying fin-width.

The resulting <111> silicon fin sidewalls are not typical for CMOS devices. The preferred crystal orientation for the CMOS devices is <100> because of the highest electron

TABLE I
TMAH ETCHING RATES

TMAH, 20%, 79.8°C [12]			
Crystal orientation	100	110	111
Etching rate (µm/min)	0.603	1.114	0.017
Etching-rate ratio	0.54	1	0.015
TMAH, 25%, 70°C [11]			
Crystal orientation	100	110	111
Etching rate (µm/min)	0.272	0.532	0.009
Etching-rate ratio	0.51	1	0.017
TMAH, 25%, 85°C			
Crystal orientation	100	110	111
Etching rate (µm/min)	0.61	1.24	-
Etching-rate ratio	0.49	1	-

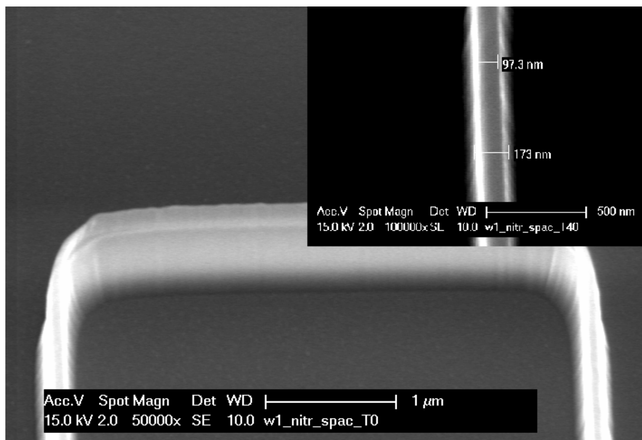

Fig. 3. SEM image of silicon fin etched in HBr/Cl_2 based plasma etcher with silicon nitride hard-mask. Thickness of deposited low-stress silicon nitride layer was 100 nm. Fin height is approximately 1.1 µm with 410 nm tall spacers. Inset in the top-right corner is a closer view of the structure from higher angle.

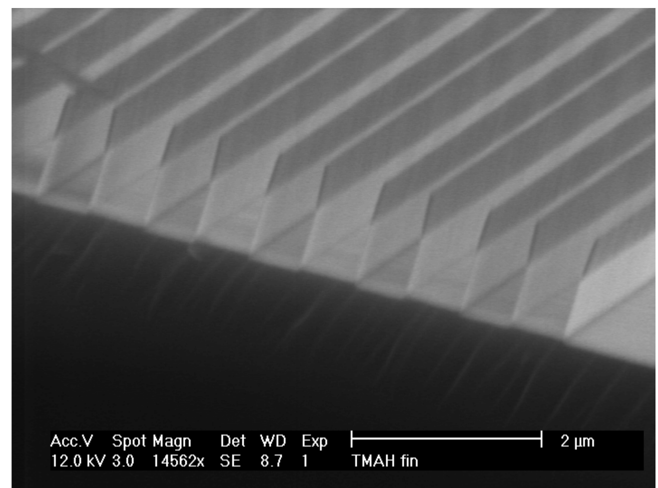

Fig. 4. SEM image of silicon fins etched in 25% TMAH solution at 85°C, with silicon nitride hard-mask. Thickness of deposited low-stress silicon nitride layer is 50 nm

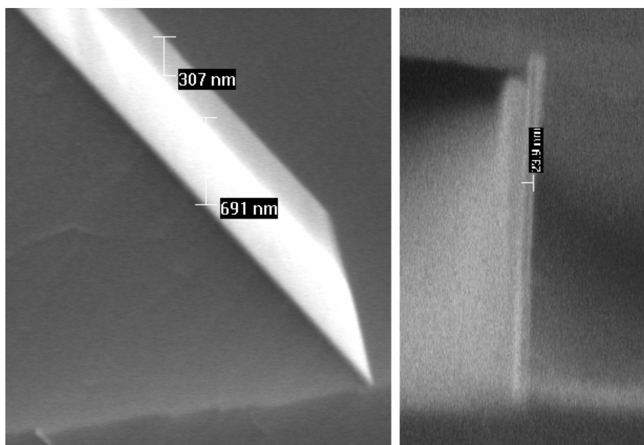

Fig. 5. SEM image of silicon fin etched in 25% TMAH solution at 85°C, with silicon nitride hard-mask. Thickness of deposited low-stress silicon nitride layer is 50 nm. The surface of the fin sidewall is very smooth. Fin cross-section is shown on the right side.

mobility. However, the smooth sidewalls achieved by TMAH etching, evident from the SEM images, are expected to decreases surface scattering, with positive influence on carrier mobilities.

The TMAH etched silicon fins are approximately 690 nm high and 24 nm wide, resulting in the aspect ratio of approximately 29:1, much higher than the typical values for RIE fins [5]-[8]. This makes the presented nitride spacer hard-mask and TMAH etching combination an attractive choice for the processing of FinFETs with high current density per used wafer surface.

IV. Conclusion

Standard processing steps like LPCVD and reactive-ion etching are used for spacer fabrication. Spacer width is controlled by the deposited layer thickness, allowing for very thin spacers. The silicon nitride spacer hard-mask is applicable to the silicon fin-etching with fins thinner than 30 nm. The silicon fin-etching by RIE gives high aspect-ratio, with sidewalls at an angle to the surface. The wet silicon-etching in crystallographic TMAH solution requires <110> wafers and gives vertical silicon walls on <111> planes. The achieved aspect-ratio is extremely high with smooth sidewalls. The improvement in sidewall quality remains to be proved by characteristics of devices processed on silicon fins.

Acknowledgment

The authors wish to thank Yann Civale on his contributions during processing and scanning electron microscopy.

References

[1] Yuan Taur and Tak H. Ning, , “Fundamentals of modern VLSI devices”, Cambridge University Press, 1998, ch. 3, 4, 5

[2] James D. Plummer, Michael D. Deal, and Peter B. Griffin, “Silicon VLSI technology”, Prentice Hall, 2000, ch. 2, 5, 9

[3] Digh Hisamoto, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu, “FinFET-a self-aligned double-gate MOSFET scalable to 20 nm”, *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320-2325, December 2000.

[4] H.-S. Philip Wong, “Beyond the conventional transistor”, *IBM Journal of Research and Development*, vol. 46, no. 2/3, pp. 133-168, 2002.

[5] Yang-Kyu Choi, Tsu-Jae King, and Chenming Hu, “A spacer patterning technology for nanoscale CMOS”, *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 436-441, March 2002.

[6] Jakub Kedzierski, Meikei Ieong, Edward Nowak, Thomas S. Kanarsky, Ying Zhang, Ronnen Roy, Diane Boyd, David Fried, and H.-S. Philip Wong, “Extension and source/drain design for high-performance FinFET devices”, *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 952-958, April 2003.

[7] T. Park, S. Choi, D. H. Lee, J. R. Yoo, B. C. Lee, J. Y. Kim, C. G. Lee, K. K. Chi, S. H. Hong, S. J. Hyun, Y. G. Shin, J. N. Han, I. S. Park, U. I. Chung, J. T. Moon, E. Yoon, and J. H. Lee, “Fabrication of body-tied FinFETs (Omega MOSFETs) using bulk Si wafers”, *Digest of Technical Papers 2003 Symposium on VLSI Technology*, June 10-12, 2003, pp. 135-136

[8] Wen-Shiang Liao, Chih-Ning Wu, Shiao-Shien Chen, Chia-Rung Hsu, and Wei-Tsun Shiau, “A novel high aspect ratio FinFET with cobalt silicided gate structure”, *Proc. 2005 IEEE VLSI-TSA Intl. Symposium on VLSI Technology*, April 25-27, 2005, pp. 114-115

[9] Y. X. Liu, K. Ishii, T. Tsutsumi, M. Masahara, H. Takashima, and E.Suzuki, “Ultra-narrow rectangular cross-section Si-fin channel double-gate MOSFETs fabricated by using orientation-dependent wet etching”, *Proc. Device Research Conference*, June 23-25, 2003, pp. 31-32

[10] Yongxun Liu, Meishoku Masahara, Kenichi Ishii, Toshihiro Sekigawa, Hidenori Takashima, Hiromi Yamauchi, and Eichii Suzuki, “A highly threshold voltage-controllable 4T FinFET with an 8.5-nm-thick Si-fin channel”, *IEEE Electron Device Letters*, vol. 25, no. 7, pp. 510-512, July 2004.

[11] K. Sato, M. Shikida, T. Yamashiro, K. Asaumi, Y. Iriye, and M. Yamamoto, “Anisotropic etching rates of single-crystal silicon for TMAH water solution as a function of crystallographic orientation”, *Proc. MEMS 1998 The Eleventh Annual Intl. Workshop on Micro Electro Mechanical Systems*, Jan. 25-29, 1998, pp. 556-561

[12] Mitsuhiro Shikida, Kazuo Sato, Kenji Takoro, and Daisuke Uchikawa, “Comparison of anisotropic etching properties between KOH and TMAH solutions”, *Proc. MEMS 1999 Twelfth IEEE Intl. Conference on Micro Electro Mechanical Systems*, Jan. 17-21, 1999, pp. 315-320