Channel Length and Oxide Thickness Scaling Effects on Low Frequency (1/f) Noise in Metal / High-κ sub-micron MOSFETs

P. Srinivasan[1], E. Simoen[2] and C. Claeys[1,2]

[1] IMEC, Belgium.

[2] Electrical Engg. Dept., KU Leuven, Belgium.

SEEDS FOR TOMORROW'S WORLD

© imec 2005

Outline

- Low-Frequency (1/f) noise
  - Importance of the study
  - 1/f noise in high-κ MOSFETs
- Scaling Effects on 1/f noise
  - Scaling elements in MOSFET
  - How 1/f noise is affected ?
- Experimental Conditions
- Results
  - Channel length dependence of 1/f noise
  - Oxide thickness dependence of 1/f noise
    - High-κ layer dependence
    - Interfacial layer dependence
- Conclusion and Summary

LF noise study - Importance

- For analog applications
  - One of the reliability measures
  - Noise minimization will be the key issue.

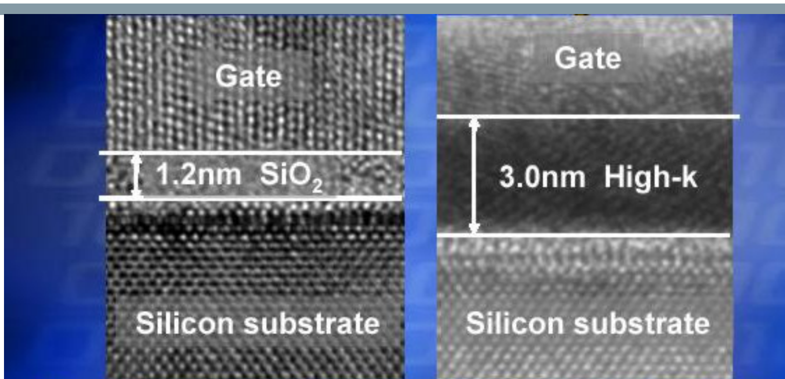
- Tool for device lifetime and reliability
  - Strongly technology sensitive parameter
    - Mobility limited scattering
    - Oxide defect limited trapping
- Important in RF and microwave regions
  - Phase noise of nonlinear circuits and devices in the GHz region is affected by LF noise

Need for metal gate / high-κ

1. Gate oxide (SiO_2) in MOSFETs approach scaling limits
   1. $C = \varepsilon_0 \varepsilon_{Si} A / t_{ox}$
   2. Reliability of these devices ?

Soln: Replace with gate oxide of higher dielectric constants

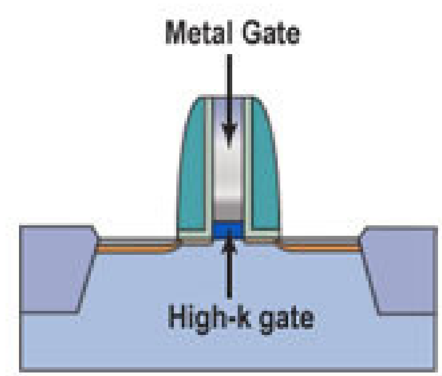
2. Typical elements - Oxides of Hf, Zr, Al etc.
3. Poly-depletion effects with poly-Si gate electrodes
4. Reliability of the devices of high-κ oxides ?
   3. One of the reliability factor for analog – 1/f noise
5. This study – Scaling effects on 1/f noise in high-κ oxides



Benefits compared to current process technologies

	High-k vs. SiO_2	Benefit
Capacitance	60% greater	*Much faster transistors*
Gate dielectric leakage	> 100x reduction	*Far cooler*

Source: Intel

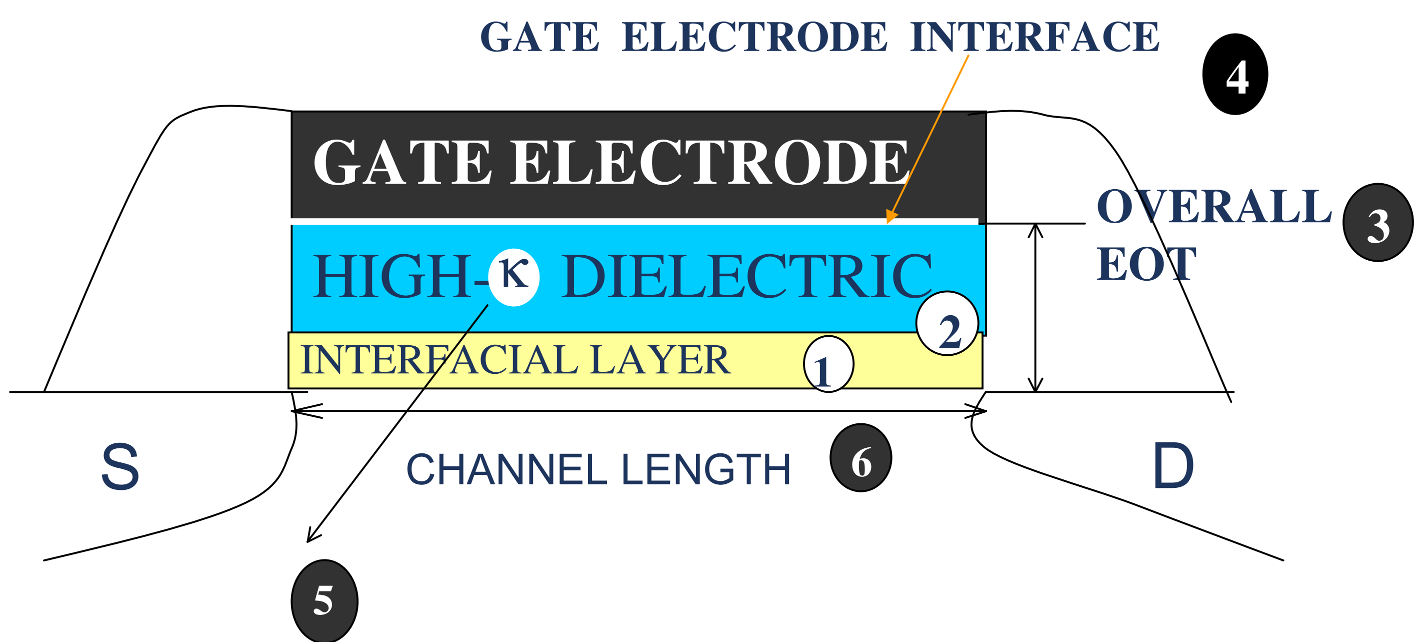


© imec 2005

Scaling Elements

Typical scaling elements that may affect 1/f noise

(1) Interfacial layer (SiO_2) oxide thickness - t_{IL}
(2) High-κ gate dielectric thickness - $t_{high\text{-}k}$
(3) Overall Equivalent Oxide Thickness (EOT)
(4) Gate Electrode/High-κ interface
(5) κ-value of high- κ oxide layer
(6) Width - W and Length - L of the device.



Theory – Gate Length Scaling

	ΔN theory	$\Delta\mu$ theory
S_{id}/I_d^2	$[t_{ox}]^2\ [V_{gs} - V_t]^2\ [1/WL]$	$[t_{ox}]\ [V_{gs} - V_t]\ [1/WL]$
$S_{id,sat}$	$[V_{gs}-V_t]^2\ [W/L^3]$	$[V_{gs}-V_t]^3\ [1/t_{ox}]\ [W/L^3]$
S_{vg}	$[t_{ox}]^2\ [1/WL]$	$[t_{ox}]^2\ [V_{gs}-V_t]\ [1/WL]$

- **Device-to-device spread among the devices**
- **Noise spectrum changes its character from 1/f-like to a Lorentzian ($1/f^2$) [GR spectrum]**

Theory – Gate Oxide Scaling

	ΔN theory	Δμ theory
S_{id}/I_d^2	$[t_{ox}]^2$ $[V_{gs} - V_t]^2$ $[1/WL]$	$[t_{ox}]$ $[V_{gs} - V_t]$ $[1/WL]$
$S_{id,sat}$	$[V_{gs}-V_t]^2$ $[W/L^3]$	$[V_{gs}-V_t]^3$ $[1/t_{ox}]$ $[W/L^3]$
S_{vg}	$[t_{ox}]^2$ $[1/WL]$	$[t_{ox}]^2$ $[V_{gs}-V_t]$ $[1/WL]$

- **n-MOSFETs - ΔN theory, p-MOSFETs - Δμ theory**
- **Gate voltage dependence**
  - **For thicker oxides S_{vg} is independent of $|V_{gs}-V_t|$,**
  - **For thinner oxides S_{vg} is quadratically dependent on the $|V_{gs}-V_t|$**
- **The proximity of the gate electrode, which can induce a so-called $1/f^{1.7}$ noise.**

Devices

- W= 10 μm n- and p-channel MOSFETs.
- Channel lengths L = 1 to 0.25 μm
- All the wafers received a chemical oxidation based on ozone chemistry.
  - The interfacial layer thickness (t_{IL}) ~0.4 nm or ~0.8 nm of SiO_2.
- High-κ gate oxide deposition - Metal-Organic Chemical Vapor Deposition (MOCVD) process.
  - Oxide Thickness $t_{high\text{-}k}$ – 1,2 and 3 nm
- Gate electrode deposition – Physical Vapor Deposition
  - TiN metal gate and TaN capping layer

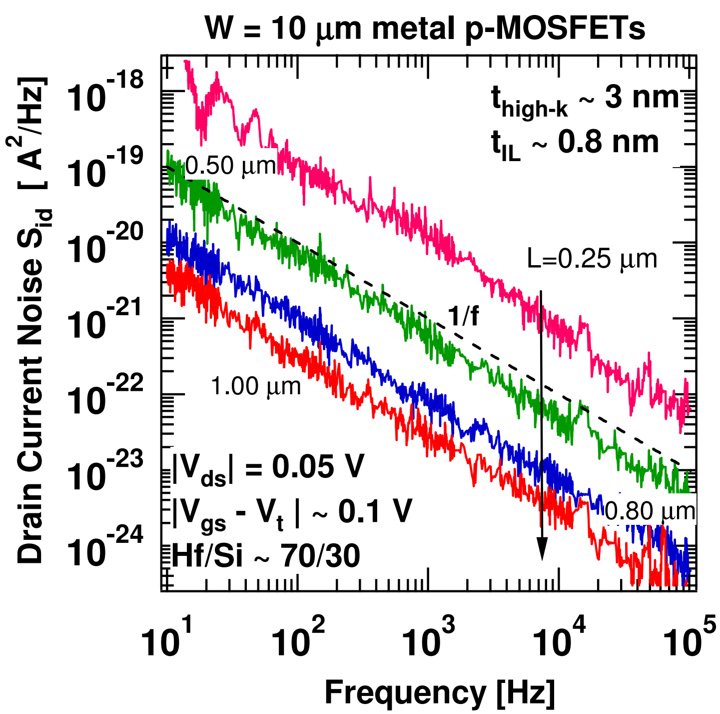
Experimental

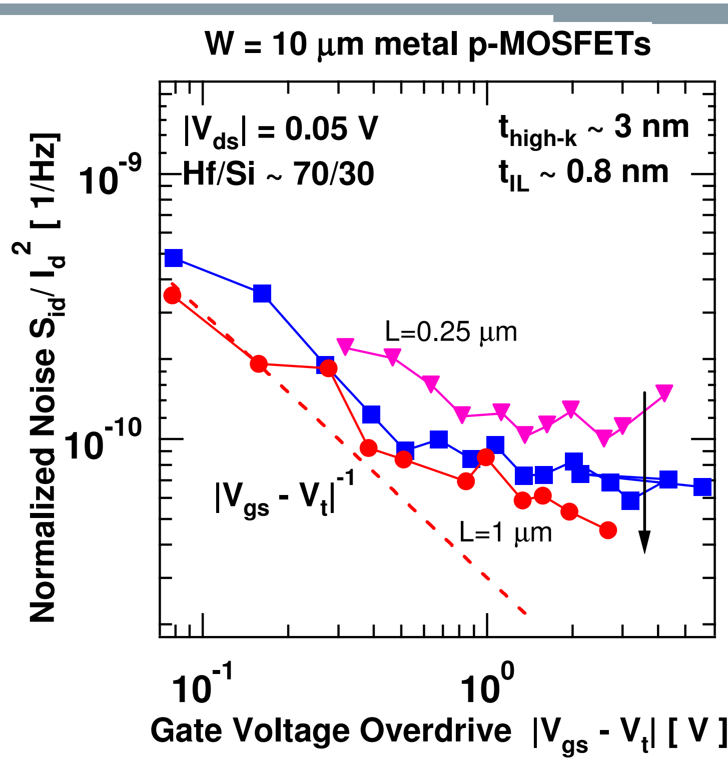
- Noise in linear region of MOSFET (V_{DS} = 0.05 V, 0.6 V ; 0.3 < V_{GS} < 1.5 V)

- On-wafer noise measurements were performed
  - Hardware
    - BTA9812 pre-amplifier with noise analyzer and
    - HP35665A spectrum analyzer
  - Software
    - NoisePro from Cadence.

- Parameters for study:
  - Drain Current Noise Spectral Density – S_{id} (A^2 / Hz)
  - Normalized spectral density – S_{id} / I_d^2 (1/ Hz)
  - Input referred noise spectral density – $S_{vg} = S_{id} / g_m^2$ (V^2 / Hz)

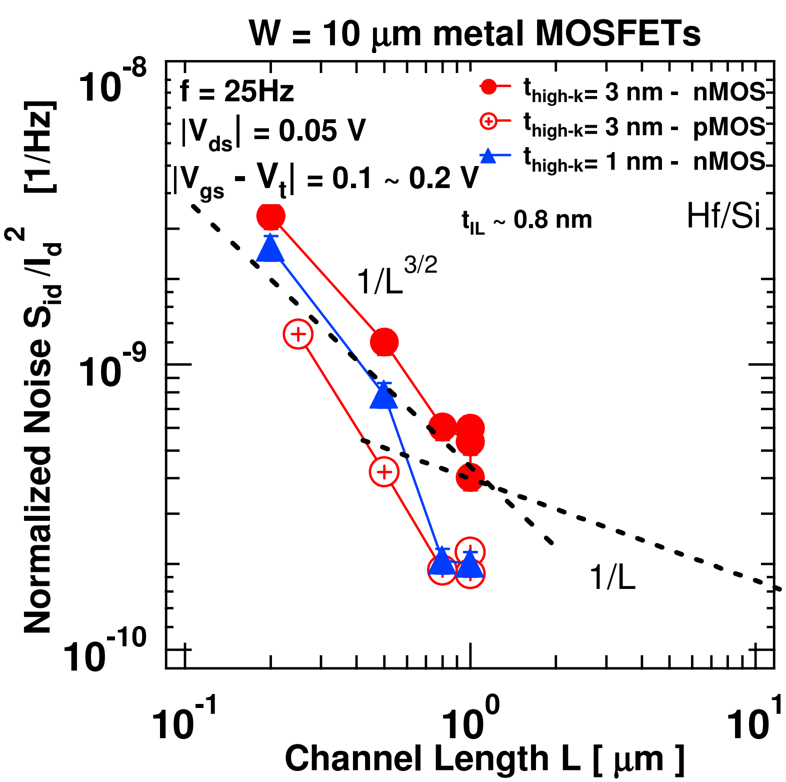
Gate (Channel) Length Dependence (L)

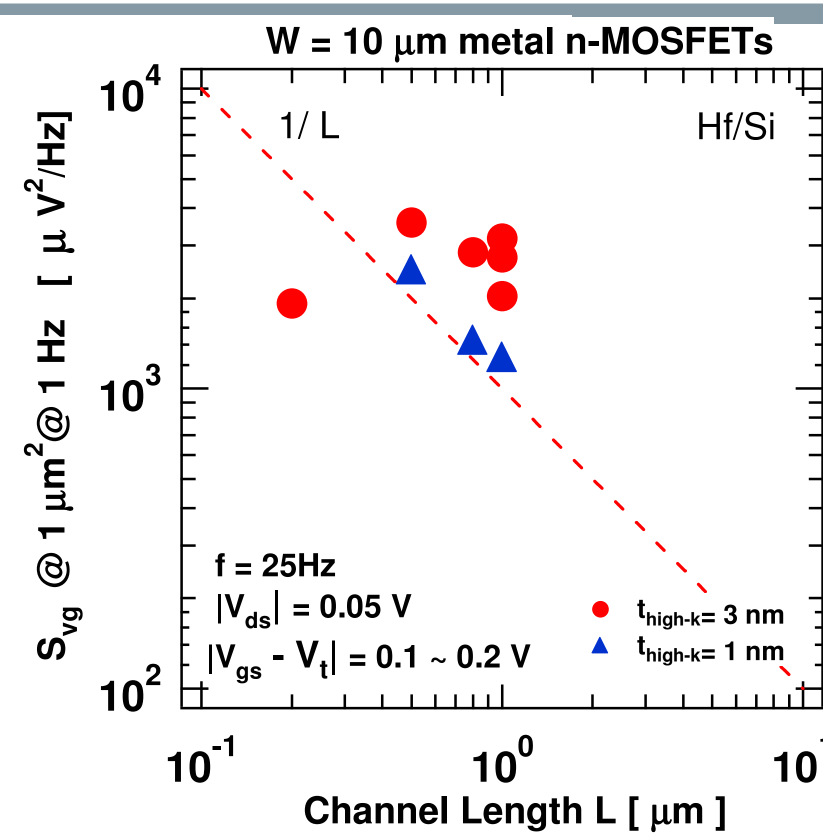




- Spectra look $1/f^{\gamma}$ like, with γ between 0.9 ~ 1.05.
- 1/f noise S_{id} ↓ Channel length (L) ↑
- S_{id}/I_d^2 ↓ Channel length (L) ↑

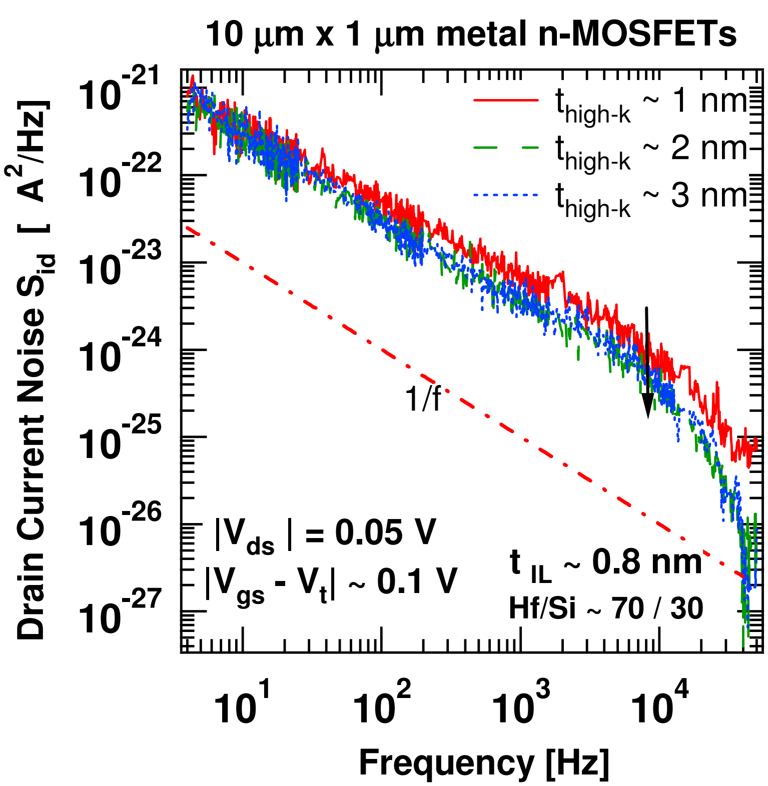
Gate (Channel) Length Dependence

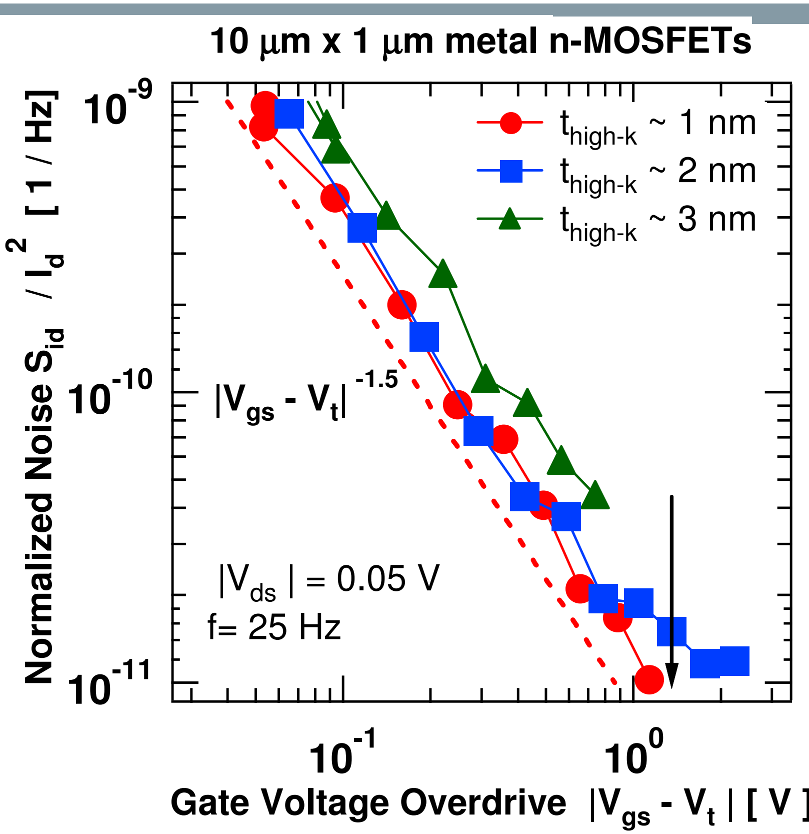




- Deviation from 1/L for S_{vg} and S_{id}/I_d^2, where a stronger dependence on L is observed ($1 / L^{3/2}$) for lower L .
- Role of series resistance ?

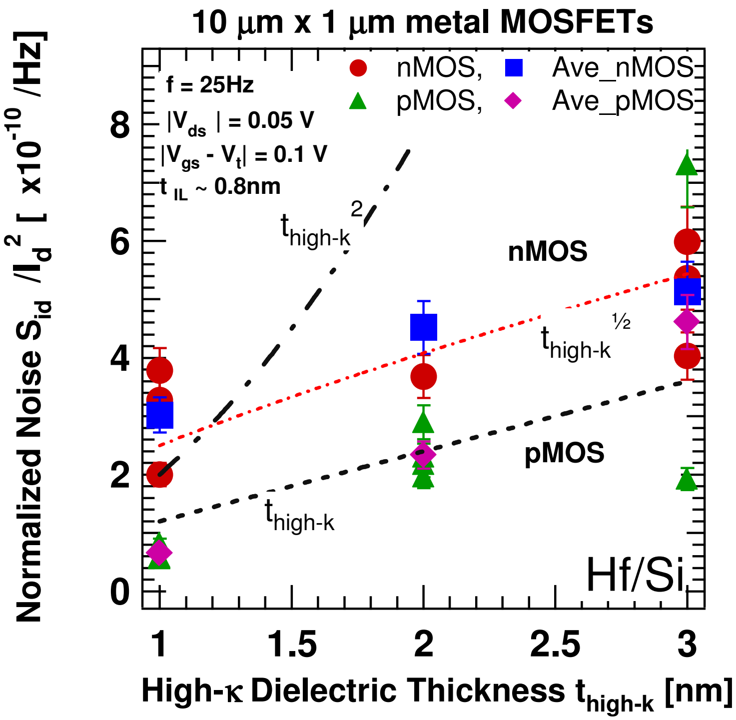
High-κ Thickness Dependence t_{high-k}

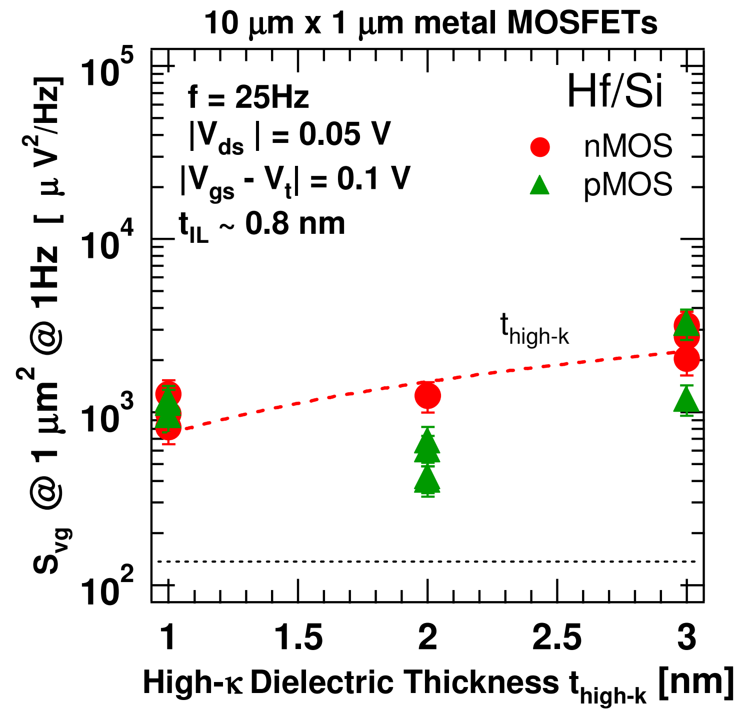




- **Effect of high-κ dielectric layer thickness on 1/f noise is found to be marginal.**
- **Normalized noise is proportional to a factor of 1.5**

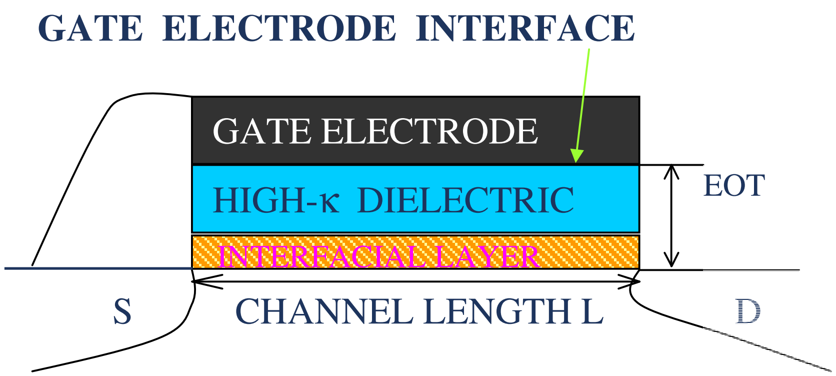
High-κ Thickness Dependence $t_{high\text{-}k}$

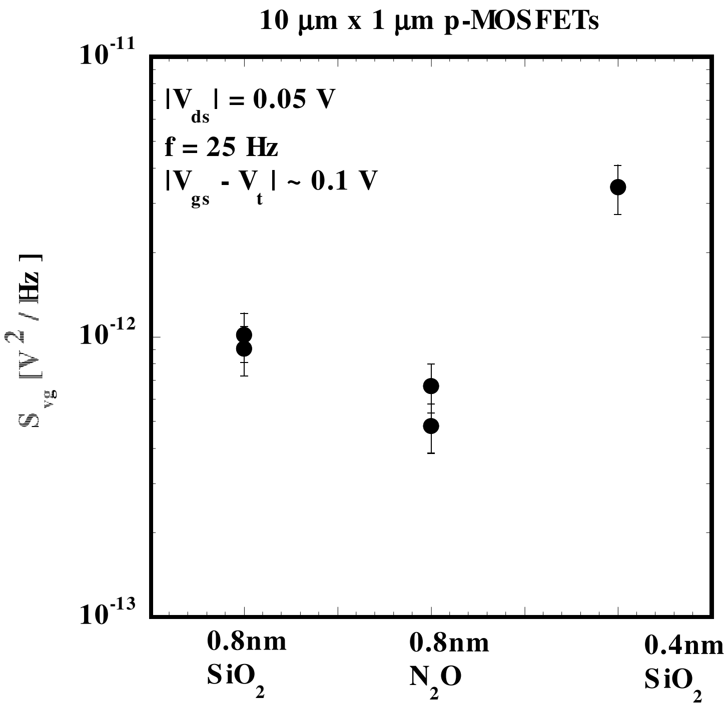




- Noise values are lower for p- than n-MOSFETs
- For p-MOSFETs, the $t_{high\text{-}k}$ dependence of S_{id}/I_d^2 and S_{vg} are clearly visible
- For n-MOSFETs, $t_{high\text{-}k}$ dependency is found to be between $t_{high\text{-}k}^{1/2}$ and $t_{high\text{-}k}$.

Effect of Interfacial Layer Thickness t_{IL}





- Interfacial layer thickness t_{IL} ↑ EOT ↑ 1/f noise ↓
- HfO_2 as a high-κ dielectric
  - 1/f ↑ almost by 5X when 0.8 nm t_{IL} → 0.4 nm t_{IL}
- Strong impact on 1/f due to scaling t_{IL} than t_{high-k}

Conclusions

• High-κ based gate stacks have impact on the low-frequency (1/f) noise behavior. Both n-and p-devices exceed the ITRS specs by about an order of magnitude.

• For both n- and p-MOSFETs, a stronger gate length dependence (L) on 1/f noise was observed for lower L values.

• While high-κ p-MOSFETs follow the Δμ theory for thickness dependence, deviations are observed for n-MOSFETs.

• Stronger impact on 1/f due to scaling t_{IL} than $t_{high\text{-}k}$

•No 1/f noise models exist. Observed differences should be taken into account for a better modeling.