Simulation of a Nanolink Hot-Plate Device

Alfons W. Groenland, Alexey Y. Kovalgin, Jisk Holleman, and Jurriaan Schmitz

***Abstract*—In this work, a miniaturized hotplate device with a low power consumption of a few milliwatts and a CMOS compatible fabrication process is proposed and analyzed. This micro hotplate is based on a nanoscopic conductive link (Ø 10-100 nm) created between two electrodes separated by a SiO_2 layer and can be used as chemical sensor and actuator. A typical foreseen application is a gas sensor (i.e. Pellistor) for hydrocarbons (butane, methane, propane, etc.) based on temperature changes due to the catalytic combustion of hydrocarbons. In this paper, simulation results are presented showing the electrical and thermal properties of these newly designed nanoscopic–link based devices.**

***Index Terms*— Hot Surface, Chemical Sensor, Chemical Actuator, Pellistor, Microreactor**

I. INTRODUCTION

There is a great demand in silicon-processing compatible, simple and low-cost micro hotplates consuming a power of a few milliwatts. Micro hotplates are devices with a surface of typically 1-10000 μm^2 that can be electrically heated (often resistive heating) to 100-600 °C with small time constants (10^2 µs). Such micro hotplates are often used in chemical sensors [1] or mass flow meters [2] based on temperature changes. Because of the elevated operating temperatures, the devices can also behave as chemical actuators, i.e., microreactors providing energy in the form of heat to initiate thermo-activated chemical reactions [3]. Optionally, devices are coated with catalytically active surface coatings to achieve chemical selectivity and/or a lower reaction temperature.

An important example of a micro hotplate device is a gas sensor for hydrocarbons (butane, methane, propane, etc), the so-called Pellistor [1, 4]. Such a sensor is based on temperature changes due to the catalytic combustion of hydrocarbons. The combustible gas reacts with oxygen on the hot catalytic surface, due to elevated temperature of the surface. The combustion process leads to a higher local temperature, which is detected by a change in the electrical resistance of the heater. In other words, the micro hotplate simultaneously acts as a thermal actuator to heat the catalytic surface, and as a thermal sensor to monitor the surface temperature. Both functionalities require a well defined and stable electrical resistance (R) of the heater, and the known temperature coefficient of the resistance (TCR). The catalyst is conventionally incorporated to enable the selective detection of a gas in a mixture, and more importantly, to lower the reaction temperature of the combustion process below the lower explosive limit (LEL) of the gas. The latter means that the gas is only combusted locally at the catalytic surface, without the risk of explosion of the entire gas volume. This is generally referred to as the 'safe' detection of combustible gases [5].

One significant drawback of conventional Pellistors is their relatively high power consumption. Commercially available platinum wire based ('classic') devices require a power around 100 mW [4]. Other types of Pellistors that are fabricated in the last decennium using microtechnology, based on a suspended membrane with a platinum thin film resistor, still require 20-40 mW [5].

Recently, a new generation of Pellistor type micro hotplate devices is reported, with a power consumption of only a few milliwatts [6, 7]. In that approach, the heat is generated by a conductive nanoscopic link: a conductive part with a diameter of 10-100 nm. Situated between two polysilicon electrodes separated by a thin silicon oxide layer, the link is formed in the so-called 'anti-fuse process'. In this process, a large voltage is applied to the polysilicon electrodes, leading to a high electric field and hence a dielectric breakdown of the thin oxide layer. The conductive link, often referred to as the 'anti-fuse', is subsequently enlarged, as a result of the applied current stress. The low power consumption of the resulting device is attributed to the high relative electrical resistance of the link, compared to the resistance of the contact leads (i.e., high R_{link}/R_{tot} ratio), and the minimized heat losses to the substrate.

It was found that the performance of the anti-fuse based devices was limited by several problems, including a time consuming (individual) electrical device programming procedure, poorly reproducible link characteristics and limited long-term stability of the hot plates, most likely due to thermodynamic instabilities of the link material at high temperatures. Furthermore, modeling of anti-fuses is difficult because the dimensions and chemical composition of the link are not well known [8].

In this work we make steps towards developing a new micro hotplate design, to overcome these problems. We aim at creating the nanoscopic link in a better controlled fabrication process that is compatible with standard CMOS processing.

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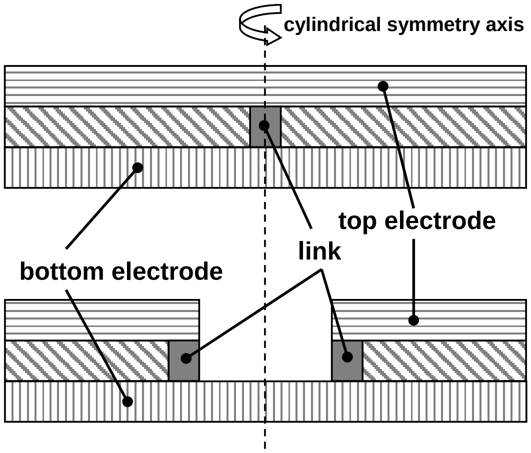

Fig. 1. Completely filled link (top) and partially filled link design (bottom).

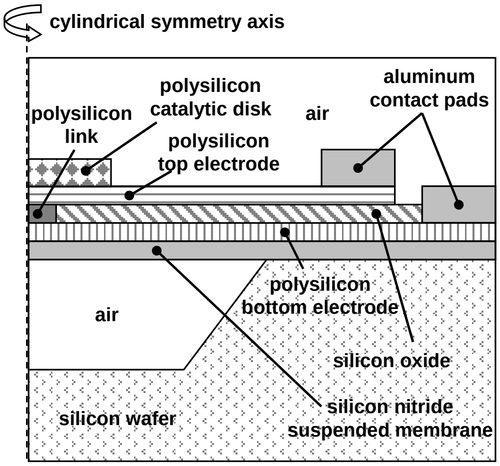

Fig. 2. Cylindrically symmetrical structure used for modeling.

II. DEVICE DESIGN AND SIMULATIONS

The new nanolink based micro hotplates will be fabricated in a so-called 'drill-and-fill' process. This process includes etching a *nanoscopic hole* in a SiO_2 layer on top of the first electrode, and filling this hole in with the second electrode material. This approach is referred to as the 'completely filled link' approach (see Fig. 1). It yields three technological challenges: definition of the nanoscopic hole with lithography, etching the nanoscopic hole in the SiO_2 layer and filling the hole with electrode material.

Currently we explore the possibility to use e-beam lithography in combination with the wet chemical etching of SiO_2 (HF based) and chemical vapor deposition (CVD) of in-situ doped polysilicon (or atomic layer deposition (ALD) of TiN).

The process can be simplified by the definition of a *micron sized hole* in the SiO_2 layer with standard UV lithography and the wet chemical etching of SiO_2 followed by ALD of a thin layer of electrode material (typically 10-20 nm). In case the electrode material has a good step coverage (e.g., ALD of TiN), this results in the conductive link of a hollow cylindrical shape and relatively high resistance. This approach is referred to as the 'partly filled link' approach (see Fig. 1).

The electrical and thermal properties of nanolink based devices were investigated in simulations with ATLAS code (SILVACO international, [9]) including a GIGA module for lattice heat flow and general thermal environments. The module accounted for the temperature dependence of materials and transport parameters on the lattice temperature. The lattice temperature model included Joule heating, heating and cooling due to carrier generation and recombination, and the Peltier and Thompson effects. Free convection and radiative heat transfer were not included in the model.

The devices were simulated with a cylindrical symmetrical quasi 3D structure (see Fig. 2). Current-voltage (*I-V*) curves and temperature distributions were simulated by applying a voltage in small steps and calculating the current and temperature. For a boundary condition, two thermal contacts at 300 K were specified at the silicon substrate and in the air region covering the device, approximately 100 µm away from the link region.

A typical cylindrically symmetrical structure used for modeling of the completely filled link device is shown in Fig. 2. The device has two 100-nm thick polysilicon electrodes (in situ doped with 10^{20} at/cm^3 phosphorus) separated by a 20 nm (CVD) SiO_2 layer. The polysilicon nanoscopic link (in situ doped with 10^{20} at/cm^3 phosphorus) has a diameter ranging from 10 to 100 nm. A 100 nm thick, low stress, silicon rich nitride (SiRN) membrane is realized over a 15 µm deep air gap (created using sacrificial etching of polysilicon in TMAH), for better thermal insulation. A 200-nm thick polysilicon disk (Ø 10 µm) is placed on top of the electrodes as a catalyst support. The disk is electrically insulated by a 20 nm SiRN layer. Aluminum electrodes of 1 µm thickness are used to provide electrical contacts to the polysilicon contact leads.

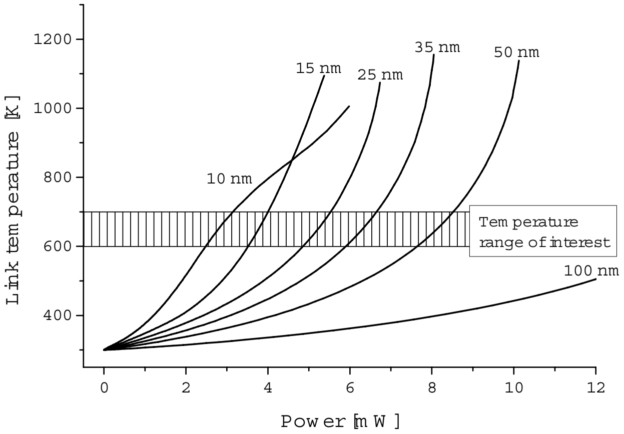

Fig. 3. Modeled maximum device temperature (i.e., link temperature) versus applied power for the cylindrically-symmetrical structure shown in Fig. 2 for various link diameters.

Fig. 3 represents the simulated results for the links of various diameters between 10 and 100 nm. It is observed that the power consumption can be strongly influenced by the link diameter: the smaller the link, the higher the $R_{\text{link}}/R_{\text{tot}}$ ratio and therefore the lower the power consumption. For the link-temperature range of interest, i.e. 600-700 K for Pellistor type devices, 2-7 mW is needed.

One should bear in mind that we used a 2D simulator (a 3D version was not available) with the ability to simulate a cylindrically symmetrical “quasi 3D” structure. For such a structure, the lateral heat losses via the electrodes and membrane are expected to be higher than for the real 3D structure having two crossing beam-shaped electrodes, connected by the link in the centre only. In contrast to this, the simulated electrodes have the shape of two parallel disks. To account for the real electrode shape, we carried out the simulations with an adapted device model, wherein the electrode thickness was reduced in such a way that the total electrode volume (and hence the thermal resistance) resembled that of the beam-shaped electrode volume. This approximation is valid as long as the (electrical) link resistance is much larger compared to the electrode resistance; i.e., the thermal and electrical resistances of the structure are decoupled [6].

During these simulations we observed that for the scaled electrode thickness (ca. 10 nm), the electrical resistance of the electrodes increased dramatically, resulting in self heating of the electrodes and hence a totally different temperature behavior. The results of the simulations appeared to be unrealistic and are therefore omitted. Currently we are working on problems with convergence of the simulator (occurring at very small device dimensions and higher voltages, current densities, and temperatures) which hinder the simulation process significantly.

III. CONCLUSIONS

A new design approach to low-power nanolink based micro hotplates is presented with the aim to improve the previously published devices [6, 7]. The new design aims to overcome the limitations of those devices, including a time consuming (individual) device programming procedure, poorly reproducible link characteristics and limited long-term stability of the hot plates, most likely due to thermodynamic instabilities of the link material at high temperatures. Simulations are presented showing link temperatures of 600-700 K with 2-7 mW power consumption.

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