A Binary-To-Thermometer Decoder with redundant switching sequences

Georgi I. Radulov, *Student Member IEEE*, Patrick Quinn, Member IEEE,
Hans A. Hegt, *Senior Member IEEE*, Arthur H.M. van Roermund, *Senior Member IEEE*

***Abstract*— This paper presents a practical realization of a binary-to-thermometer decoder with redundant output switching sequences. Its particular application is to decode the DAC segmented MSB part. In the presented realization, 4 MSB binary bits are decoded to 15 thermometer bits through 2 different thermometer switching sequences. The end-user can choose the decoding switching sequence, according to the distribution of the mismatch errors of the DAC signal current sources. Therefore, the chip yield $Yield_{INL}$, which is defined as the percentage of DAC samples that meet some specifications, is expected to improve by more than 12% for barriers $Yield_{INL} > 95\%$. The presented realization proves the efficiency of this approach based on two main considerations: area and power consumption. The silicon area of the decoder is increased by only 50%, while for the whole DAC area, this increase is under 3%. On the other hand, the power consumption of the decoder is doubled but it is still under 0.5% of the entire DAC power consumption. These results prove not only the efficiency of the presented particular realization but also the high efficiency of the redundant switching sequences for the DAC MSB thermometer current sources. The article concludes with general discussion and further possible enhancement of the new decoder and the presented realization.**

Index Terms— Binary-to-thermometer decoder, current-steering DACs, flexibility, redundancy.

I. Introduction

BINARY-to-thermometer decoders are used in the segmented and fully thermometer digital-to-analog converters. Their main function is to convert the binary coded input digital word into a thermometer coded digital word. A short example of 3 binary to 7 thermometer decoder as a conversion matrix is given by (1). The columns of the binary decoder are weighted with the powers of 2, while all the columns of the thermometer decoder have the same weight. The binary coding has higher efficiency. The thermometer coding has an inherent redundancy.

$$\begin{matrix}3&2&1\end{matrix} \quad \leftarrow weight \rightarrow \quad \begin{matrix}1&1&1&1&1&1&1\end{matrix}$$
$$\begin{bmatrix}0&0&0\\0&0&1\\0&1&0\\0&1&1\\1&0&0\\1&0&1\\1&1&0\\1&1&1\end{bmatrix}_{binary} \xrightarrow[3b\rightarrow 7th]{decoder} \begin{bmatrix}0&0&0&0&0&0&0\\0&0&0&0&0&0&1\\0&0&0&0&0&1&1\\0&0&0&0&1&1&1\\0&0&0&1&1&1&1\\0&0&1&1&1&1&1\\0&1&1&1&1&1&1\\1&1&1&1&1&1&1\end{bmatrix}_{thermometer} \qquad (1)$$

Theoretically, the thermometer coding redundancy means that the input digital codes can be equivalently represented by more than one combination of bits. For example, code 1 can be represented by 7 different combinations, e.g. 0000001, 0000010…, etc. Notable exceptions are codes 0 and full-scale, where only a single bit combination exists.

In practice, these coding matrices control the switching of the DAC analog signal currents (analog entities, in general). Therefore, the weights of (1) should be modified by adding the current mismatch (2):

$$\begin{matrix}b_3&b_2&b_1\end{matrix} \quad \leftarrow weight \rightarrow \quad \begin{matrix}t_7&t_6&t_5&t_4&t_3&t_2&t_1\end{matrix}$$
$$\begin{bmatrix}0&0&0\\0&0&1\\0&1&0\\0&1&1\\1&0&0\\1&0&1\\1&1&0\\1&1&1\end{bmatrix}_{binary} \xrightarrow[3b\rightarrow 7th]{decoder} \begin{bmatrix}0&0&0&0&0&0&0\\0&0&0&0&0&0&1\\0&0&0&0&0&1&1\\0&0&0&0&1&1&1\\0&0&0&1&1&1&1\\0&0&1&1&1&1&1\\0&1&1&1&1&1&1\\1&1&1&1&1&1&1\end{bmatrix}_{thermometer} \qquad (2)$$

According to (2), every thermometer code combination generates in reality a different analog output, because of the particular mismatch errors of the current sources. Thus, codes 0000001 and 0000010 generate different output analog current with mismatch errors respectively t_1 and t_2 for the same input digital number. In practice, it is not possible to predict the current mismatch errors and hence the exact weights t_k. Rather, the mismatch errors can be measured after the chip is manufactured. This knowledge allows determining which thermometer code combination (called also switching sequence) combines so the mismatch errors that they cancel each other and produce DAC analog output with the smallest possible mismatch error. Such a best case scenario requires a hardware realization of the binary-to-thermometer decoder that can realize all possible switching sequences. In principle, the hardware costs would be huge. However, note that such implementations exist [1].

Instead of realizing all possible switching sequences and

Manuscript received September 1, 2006. This work was supported by the Dutch Technical Foundation STW, ECS.6098.

Georgi I. Radulov is a PhD student at the Department of Electrical Engineering of the Eindhoven University of Technology (TU/e), EH5.15, P.O. Box 513, 5600MB Eindhoven, the Netherlands, tel: +31 40 247 3242, e-mail: g.radulov@tue.nl.

Patrick J. Quinn is an senior design manager at the Xilinx Ireland.

Johannes A. Hegt is an Associate Professor at the Department of Electrical Engineering of TU/e, e-mail: j.a.hegt@tue.nl.

Arthur H.M. van Roermund is a Full Professor at the Department of Electrical Engineering of TU/e, e-mail: a.h.m.v.roermund@tue.nl.

paying the big hardware price, this paper suggests to realize only a few switching sequences. The increase in the hardware is very small, while the rate of DAC linearity improvement is high. For example, if two switching sequences are compared to the usual only one, then the number of possible error distributions is doubled. However, if another switching sequence is added, then the number of possible distributions is again increased but only by half. Thus, for every extra switching sequence, the rate of improvement decreases. Therefore, it makes greater sense to implement a few possible switching sequences, instead of implementing all the possibilities for the price of a huge hardware investment. The theoretical framework of these approaches is elaborated in [1] and [2]. It is shown that a decoder with more than one switching sequence can improve DAC yield.

For the industry, the yield is among the most important figures. Poor yield makes the manufactured chips more expensive, because the production costs for the "bad" devices must be calculated in the price of the "good" devices. Production tolerances, which can result in random mismatch and gradient errors, are among the main reasons for lower yields. For DACs, yield is primarily defined by static performance, which is the percentage of devices that meet some pre-defined INLmax specifications. The random mismatch of the analog elements is a main error contributor to DAC INL, providing that any systematic and gradient errors are minimized through careful layout. The INL errors depend on both the element mismatch errors and their distribution.

This paper shows that redundancy in the binary-to-thermometer decoder can relax the DAC mismatch requirements with respect to yield. The improvement is achieved for little additional resources. It may not offer a lot of switching sequences, but statistically it pays back with substantial yield improvement for the whole D/A Converter. The latter makes the proposed solution much more area and power efficient. The proposed solution improves chip yield and DAC static linearity. It does not deteriorate in any way the dynamic DAC performance.

Section II presents the proposed decoder architecture with 2 built-in switching sequences. Section III presents a practical realization and simulation results. Finally, conclusions are drawn.

II. DECODER WITH REDUNDANCY

The conceptual diagram of a binary-to-thermometer decoder with two switching sequences is shown in figure 1. For the second decoding level, instead of the usual ORAND gate, an ORORAND decoding cell is used. ORORAND gate has inputs that are balanced between the decoder rows and columns. Symmetrical decoding cells allow two operation modes, i.e. two switching sequences instead of only one.

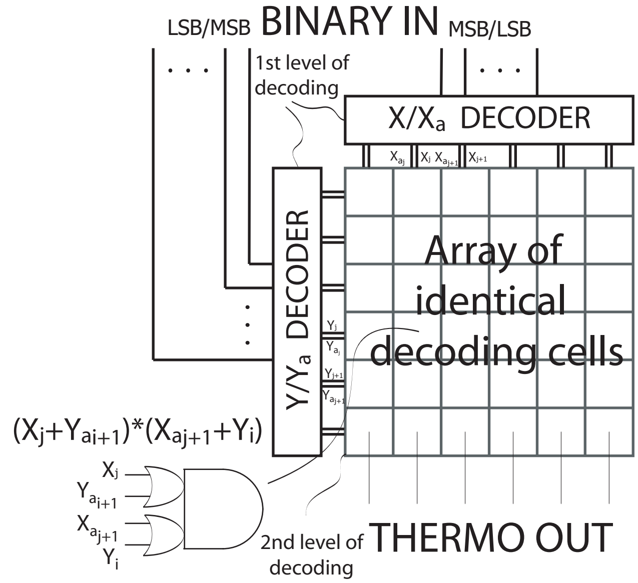

Figure 1 - A decoder with two built-in switching sequences.

To select the switching sequence, extra control signals need to be embedded in the first decoding level. These signals control the second decoding level and set the chosen switching sequence. The logic equations of the second decoding level are:

$$T_{ij} = (X_j + Ya_{i+1}) \cdot (Xa_{j+1} + Y_i), \quad \text{with} \begin{cases} Mode\ \ 1: Ya = Y, \quad Xa = 0; \\ Mode\ \ 2: Ya = 0, \quad Xa = X. \end{cases} \tag{3}$$

The information for the mode of operation is provided by the X_a and Y_a decoders. In Mode 1, all thermo Y_a signals are equal to Y signals, and all thermo X_a signals are zero. The symmetrical decoder operates as a Row-Column Decoder with X_j being C_j and Y_i being R_i. In Mode 2, all thermo Y_a signals are zero and all thermo X_a signals are equal to X. The symmetrical decoder operates as a Column-Row Decoder with X_j being R_i and Y_i being C_j. Figure 2 shows how the symmetrical ORORAND gate is transformed to an ORAND gate with different connectivity in the two modes of operation.

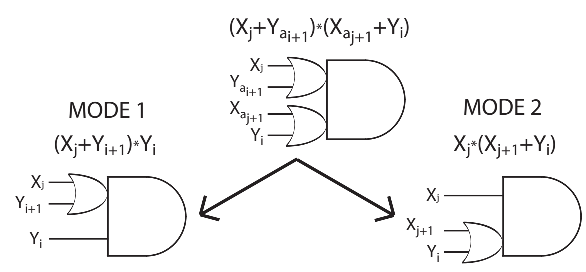

Figure 2 – A functional view of the 2nd level decoding in mode 1 and 2.

As discussed, mode 1 and mode 2 generate different thermometer switching sequences. Figure 3 shows a geometrical example of the two switching sequences for a 4-to-15 binary-to-thermometer decoder. These switching sequences are realized in practice. Note how in mode 1 the thermometer code develops horizontally, while in mode 2 the thermometer code develops vertically.

a)

1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	

b)

8	12		4
5	9	13	1
6	10	14	2
7	11	15	3

Figure 3 - Switching sequences: a) for mode 1; b) for mode 2.

III. PRACTICAL REALIZATION

The redundant binary-to-thermometer decoder is implemented in a flexible current-steering DAC based on 4 parallel 12b sub-DACs. The architecture of the DAC is similar to the basic DAC architecture used in [3, 4], see figure 4. Each of the 12b sub-DACs is segmented to 8b LSB binary part and 4b MSB thermometer part (15 thermometer currents).

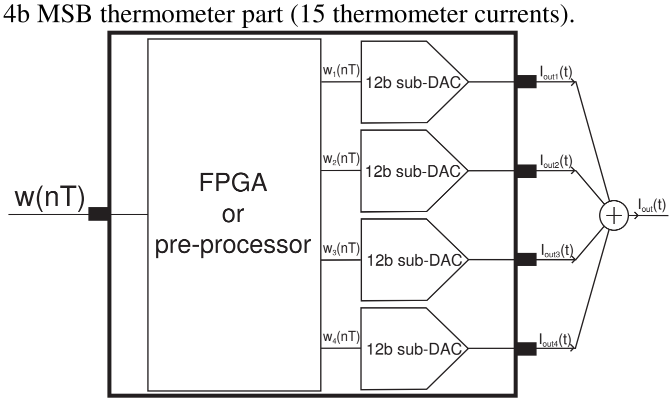

Figure 4 – Flexible 14b DAC architecture based on 4 parallel 12b sub-DACs.

The sub-DACs thermometer currents are controlled by a redundant binary-to-thermometer decoder. Its whole implementation consists of 4 instances of 4-to-15 binary-to-thermometer decoders with 2 switching sequences for each. The two switching sequences generate two different INL DAC characteristics, as shown in figure 5 for a single 12b sub-DAC.

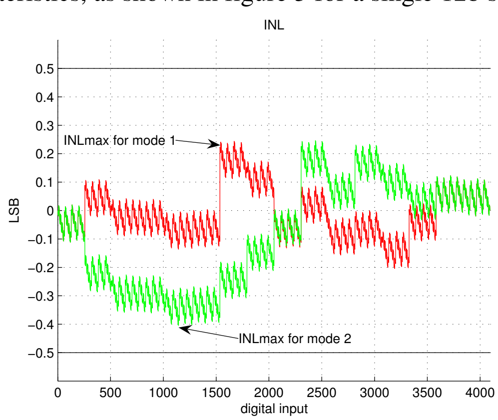

Figure 5 – An example of the 2 INL charactertisitcs of a 12b sub-DAC.

If for every DAC sample the better INL characteristic is chosen out of the two possible, then an improvement in the DAC $Yield_{INL}$ can be achieved. Figure 6 shows the DAC INL yield for a 12b sub-DAC with the proposed decoder.

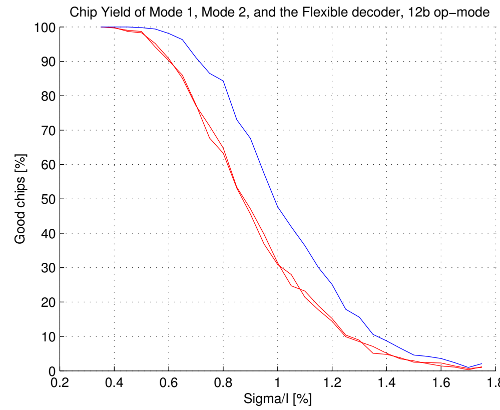

Figure 6 - DAC $Yield_{INL}$ against the currents matching for 12b op-mode.

Statistically, the two switching sequences produce the same results. However, if the better switching sequence is always chosen for a given DAC sample, then the DAC yield can be significantly improved. For the basic 12b sub-DAC, the yield improvement can reach up to 20% for moderate yield barriers

For the 13b mode of operation, when two 12b sub-DACs work in parallel to produce 13b resolution, the improvement is even greater. The possible switching sequences from the basic 2 types are now 8 (each sub-DAC has 2 possible switching sequences and can work either on the LSB or on MSB part of the 13b transfer characteristic). Figure 7 shows the DAC INL yield for a 13b op-mode. Statistically, the two switching sequences produce the same results. However, if the better switching sequence is always chosen for a given DAC sample, then the DAC yield can be significantly improved. The yield improvement can reach up to 30% for moderate yield barriers.

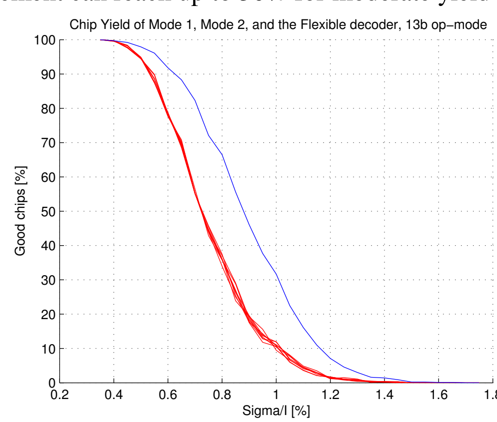

Figure 7 - DAC $Yield_{INL}$ against the currents matching for 13b op-mode.

The decoder is realized in CML logic to operate at speeds of up to 500MS/s. For one instance of the 4-to-15 binary to thermometer decoder, the first level decoders are each 3 gates, i.e. 12 all. The second decoding level consists of 16 ORORAND gates and 15 buffers and 1 OR gate that combines the 3rd thermo bit with the missing 16th bit, see figure 3. The overall current consumption is 1.2mA per decoder instance (30µA per gate). The increase of the power consumption with respect to the usual implementation is about 50%. The layout implementation of one instance of the decoder is shown in Figure 7. The silicon area of the decoder is increased by only 50%, while for the whole DAC area, this increase is under 3%, see figure 9. On the other hand, the power consumption of the decoder is doubled but it is still under 0.5% of the entire DAC power consumption

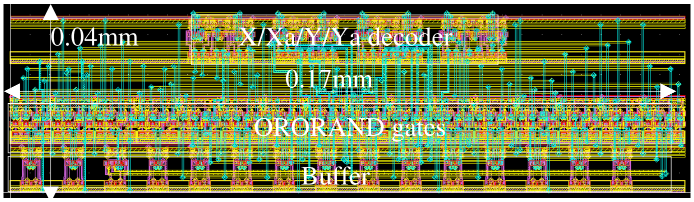

Figure 8 – The layout implementation of one instance of the decoder.

The full layout of the 14b flexible DAC chip is shown in figure 8. The area of the binary-to-thermometer decoder is around 3% of the whole chip area.

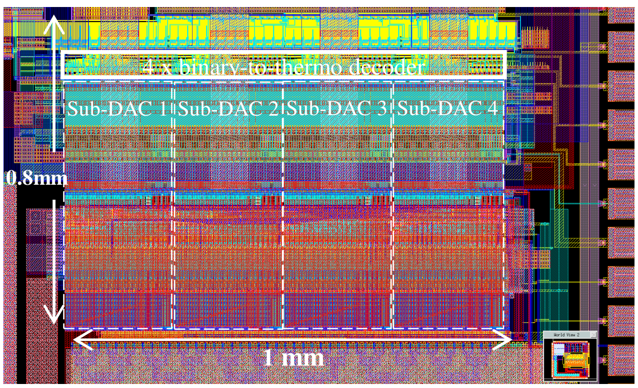

Figure 9 - 14b flexible DAC based on 4 parallel 12b sub-DACs

IV. Conclusion

A new flexible binary-to-thermometer decoder for segmented D/A Converters was presented. Instead of the conventional only one thermometer switching sequence, the proposed decoder can generate two different switching sequences. Such a built-in redundancy affects the whole DAC by allowing two different INL characteristics. A practical realization of a 4-to-15 bit binary-to-thermometer decoder in a 14b flexible DAC based on 4 parallel 12bit sub-DACs has two switching sequences for 12b op-mode, 8 switching sequences for a 13b op-mode, and 32 switching sequences for 14b op-mode. Simulations show that the improvement of the chip yield can reach up to 20% for 12b op-mode and up to 30% for the 13b op-mode. As concluded from the layout realization, the improvement is achieved for little redundant hardware resources, which makes the proposed decoder architecture very area and power efficient. Ultimately, the proposed decoder may lead to an improved chip yield and hence to reduced price of the segmented D/A Converters of all types: resistor based, switched capacitors, or current-steering type.

Acknowledgment

The authors would like to acknowledge the Dutch technology Foundation STW for the financial support of the project ECS.6098.

References

[1] Chen, T.; Geens, P.; Van der Plas, G.; Dehaene, W.; Gielen, G.; “A 14-bit 130-MHz CMOS current-steering DAC with adjustable INL”, Solid-State Circuits Conference, 2004. ESSCIRC 2004. Proceeding of the 30th European 21-23 Sept. 2004 Page(s):167 – 170

[2] Radulov, G.L.; Quinn, P.J.; van Beek, P.C.W.; Hegt, J.A.; van Roermund, A.H.M.;“A binary-to-thermometer decoder with built-in redundancy for improved DAC yield”, Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on, 21-24 May 2006 Page(s):4 pp.

[3] R.A.T. van den Hoven, G.I. Radulov, J.A.Hegt, A. van Roermund, “*A parallel current-steering DAC architecture for flexible and improved performance*”, ProRISC 2005, Veldhoven 17-18 Nov. 2005.

[4] Radulov, G.L.; Quinn, P.J.; Harpe, P.; Hegt, J.A.; van Roermund, A.H.M.; “Parallel current-steering D/A Converters for Flexibility and Smartness”, submitted to 2007 IEEE International Symposium on Circuits and Systems, 2007. ISCAS 2007.