Analysis of the base-collector junction breakdown voltage in silicon-on-glass bipolar transistors

G. Lorito and L. K. Nanver

***Abstract*—Silicon-on-glass (SOG) back-wafer-contacted vertical bipolar process developed at DIMES is investigated with regard to the device reliability. In particular, it is demonstrated that the back-wafer implanted and laser-annealed collector contacting can lead to device degradation in terms of reduction in the open-base emitter-collector breakdown voltage. This detrimental effect is a consequence of the back-wafer implantation damage and is expected to increase as the base-collector junction is closer to the back-wafer contact. Moreover, it is shown that back-wafer Schottky contacts are a valid alternative in order to eliminate the reliability degradation.**

***Index Terms*— Silicon-on-glass vertical bipolar transistors, breakdown voltage, impact ionization current, base-collector junction defects, excimer laser annealing, residual implantation damage.**

I. Introduction

THE silicon-on-glass (SOG) back-wafer-contacted vertical bipolar technology developed at DIMES [1][2] is a very attractive and promising low-cost process for the fabrication of advanced high-frequency (mono- and heterojunction) transistors. The low-ohmic back-wafer collector contacts placed directly below the emitter regions eliminate the conventional bulk buried layer contacts and considerably reduce the device size. This minimizes several parasitic effects (i.e. series resistance and capacitance) that usually degrade the device operation, and allows to achieve better compromises for the common performance trade-offs thanks to much more flexibility in the device design than the comparable bulk silicon processes. For example, a complementary bipolar process containing 25 GHz NPN and 5 GHz PNP silicon transistors has been easily implemented [3].

However, it has been observed that the innovative back-wafer contacting technique can degrade the reliability of the devices [4]. In this paper, the influence of the back-wafer contact design on the avalanche generation mechanism in the base-collector depletion region of SOG transistors is investigated by means of measuring the impact ionization current and the open-base breakdown voltage. More specifically, devices with two different collector contact designs are compared. Beside the standard implanted and laser-annealed back-wafer contacts, SOG transistors with Schottky collector contacts [3] are considered.

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II. Back-Wafer Collector Contacts and Device Reliability

The DIMES silicon-on-glass back-wafer-contacted complementary vertical bipolar process is illustrated in Fig. 1.

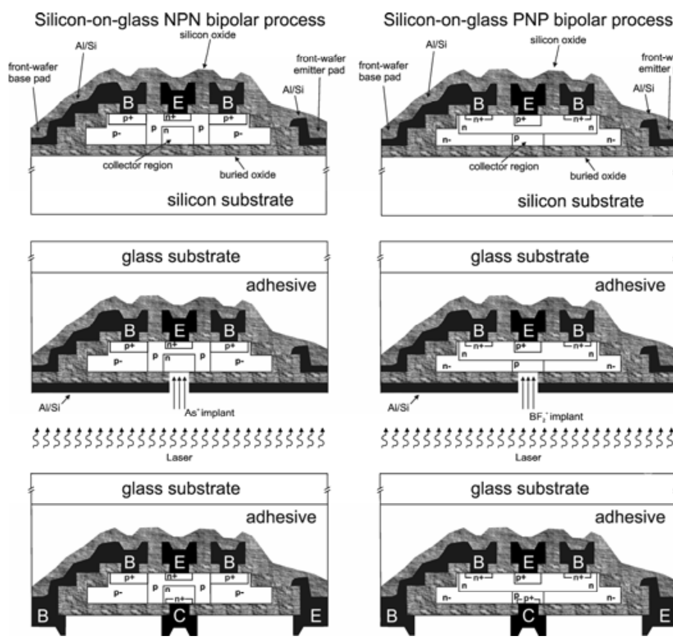

Fig. 1. Schematic process flow of the DIMES silicon-on-glass back-wafer-contacted complementary vertical bipolar technology.

The starting material is an SOI wafer with 0.2 µm intrinsic mono-crystalline silicon on a 0.4 µm buried oxide (BOX) layer. The top Si layer thickness is increased by epitaxy to 0.94 µm and trench etching is used to define islands electrically isolated by SiO_2. In such silicon islands the fully-implanted transistors are fabricated. The SIMS of the doping profiles of the NPN and PNP intrinsic regions are shown in Fig. 2. The collector region and the emitter-base regions are formed during the processing of the front side of the wafer (front-wafer) but only the emitter and the base are contacted by the front-wafer metallization. An alloy step at 400°C is performed to passivate all oxide-silicon interfaces. Afterwards, the front-wafer is glued to a glass substrate and the bulk silicon is removed by selective wet etching using the BOX as the etch-stop layer. In the back-wafer process, low-ohmic contacts are formed by high-dose low-energy implantations of As and BF_2 for NPN's and PNP's, respectively, into the contact windows opened directly on the intrinsic collector regions. Then, the dopants are activated by high-energy excimer laser annealing [5]. Note that this is the only annealing technique suitable in the back-wafer process since the adhesive layer on the front-wafer cannot tolerate a temperature higher than 300° C. In addition, simply eliminating the back-wafer implantations, bipolar devices with a Schottky junction as collector contact can be fabricated.

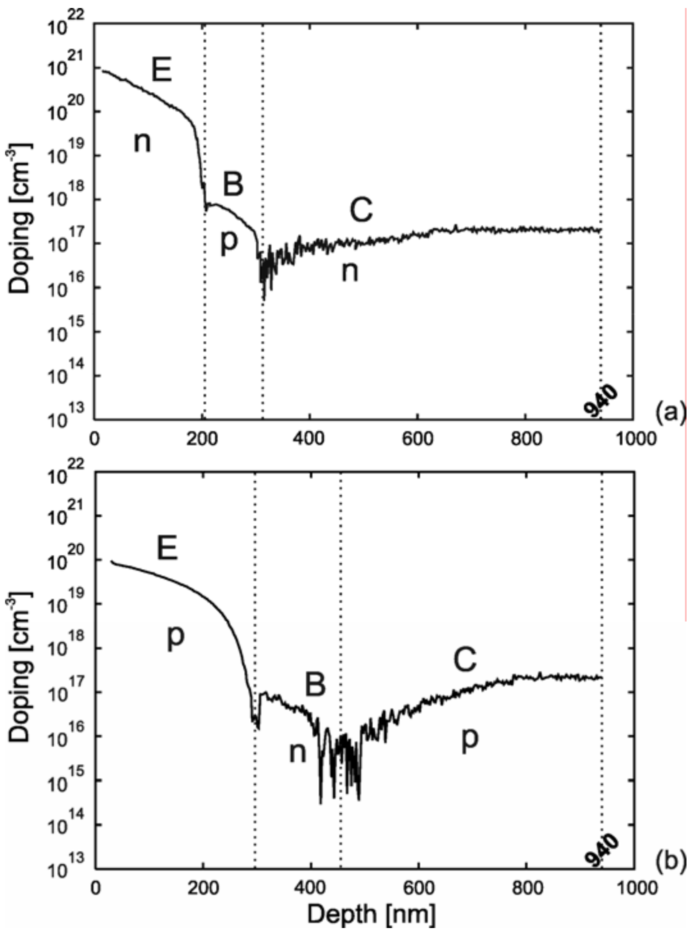

Fig. 2. SIMS of the doping profiles in the E-B-C intrinsic regions for SOG NPN's (a) and PNP's (b) after the front-wafer process.

During the back-wafer implantations, Si interstitials are injected from the implanted surfaces into the device active regions [6] and, since they can travel easily in the silicon lattice, they create defects not only in the vicinity of the collector contacts. A previous work on silicon-on-glass varactors has shown that in these devices the arsenic-implanted back-wafer contact induces defects at least as far as 0.2 µm from the contact [7]. A comparable result for BF_2 implantation has been demonstrated by means of the positron annihilation Doppler broadening analysis of the defect distribution created by such a process [8].

Therefore, the back-wafer-implantation damage is not totally repaired by the laser annealing [9], which only recrystallizes a few tens of nanometers deep region at the collector contact surface [10]. Detrimental effects on the device reliability can arise when a significant amount of residual defects is located very close to or even inside the base-collector depletion region. Indeed, in the above mentioned silicon-on-glass varactors, an appreciable reduction in the breakdown voltage has been measured if the diode depletion region extends into the defect region [7]. This suggests that in defected depletion regions the carrier impact ionization is facilitated and thus the avalanche carrier generation under reverse biasing voltage is stronger.

III. Experimental Measurements and Results

Due to the relatively low base doping, the PNP's are not suitable for studying the impact ionization and the resulting avalanche carrier generation at the base-collector junction. Indeed, increasing the reverse base-collector voltage, these devices break down because of the base punch-through mechanism. Moreover, the available SOG transistors are not provided with heat-sinks [11] and thus the measurements on the NPN's must be performed at low and medium current regimes because at high current level the self-heating of the transistors contributes significantly to carrier generation rate.

According to the results on the SOG varactors, it is expected that in the case of bipolar transistors the presence of back-wafer implantation residual defects could reduce the open-base breakdown voltage BV_{CEO}, which is related to the avalanching mechanism in the base-collector depletion region. To investigate this issue we have analyzed NPN devices with two different back-wafer collector contact designs. Beside the standard implanted and laser annealed contacts, we have considered device with Schottky collector contacts. In the latter transistors the back-wafer contact implantation is omitted and, hence, the associated damage is eliminated.

Firstly, we have compared the impact-ionization current extracted from the base current in forward mode I_{BF} at medium current level for increasing values of V_{CB}. An example of forward Gummel plots used in this measurement is shown in Fig. 3. In forward mode the base current at low and medium current regimes can be expressed as:

$$I_{BF}(V_{BE},V_{BC}) = I_{p,B-E}(V_{BE}) + I_{B,leakage}(V_{BE}) - I_{ion}(V_{BE},V_{BC}) \quad (1)$$

where $I_{p,B-E}$ is the biasing hole current from the base to the emitter, also referred to as the ideal base current, $I_{B,leakage}$ is the leakage current due to the recombination in the emitter-base depletion region and I_{ion} is the hole current to the base as a result of generation processes in the collector-base depletion region. The I_{ion} current can be measured by defining

$$I_{ion,M}(V_{BE},V_{BC}) = I_{BF}(V_{BE},V_{BC}=0) - I_{BF}(V_{BE},V_{BC}) \quad (2)$$

which is valid since the base-leakage current is only dependent on V_{BE}. I_{ion} at V_{BE} = 660 mV for transistors with the two different collector contacting methods is plotted in Fig. 4. To ensure a correct comparison the measured devices have the same forward current gain. Note that, as it can be seen in Fig. 3, the device self-heating is negligible at V_{BE} = 660 mV. The data reported in Fig. 4 live up to the expectations, that is the impact-ionization current at base-collector junction is lower if the back-wafer-implantation damage is absent.

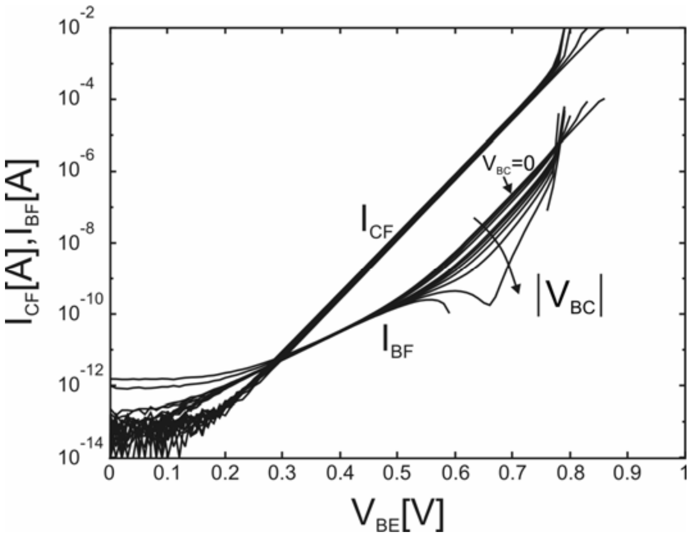

Fig. 3. Measured forward Gummel plots of SOG NPN's for increasing values of base-collector reverse voltage. The emitter contact area is 40×1 μm^2.

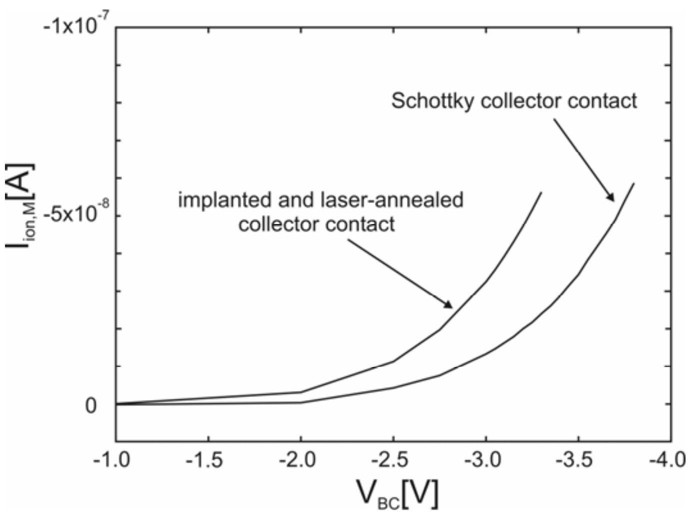

Fig. 4. Impact-ionization current versus base-collector reverse voltage at medium current regime (V_{BE} = 660 mV) for SOG NPN's with different collector contact designs. To ensure a correct comparison, the investigated devices have the same forward current gain.

For further confirmation, we have also measured the open-base emitter-collector breakdown voltage, BV_{CEO}. Note that the extraction of BV_{CEO} from the I_C-V_{CE} output characteristics is not correct since the device self-heating gives a significant contribution to the steep rise of I_C. Therefore, we have derived BV_{CEO} at low current regime from the I_B-V_{CB} plots for fixed and low values of V_{BE}. The results for V_{BE} = 570 mV are shown in Fig. 5. Again, the indication is that the device reliability is that the device reliability is better in the Schottky collector-contact transistors.

IV. Conclusions

The DIMES silicon-on-glass back-wafer-contacted vertical bipolar process has been investigated with regard to the device reliability. Experimental measurements of the impact-ionization current at base-collector junction and the open-base emitter-collector breakdown voltage, BV_{CE0}, on SOG NPN's have shown that the back-wafer implanted and laser-annealed collector contacting technique can degrade the device reliability. This detrimental effect is a consequence of the back-wafer implantation damage and is expected to increase if the transistors are vertically scaled-down. Therefore, this issue assumes great importance in the design of advanced high-frequency SOG (mono- and heterojunction) BJT's where the collector-base metallurgic junction is formed relatively close to the collector contact since a very low collector resistance is required. It is also demonstrated that the back-wafer Schottky contacts are a valid alternative in order to eliminate the reliability degradation. Nevertheless, in the latter case other speed versus collector-contact-resistance trade-offs are introduced.

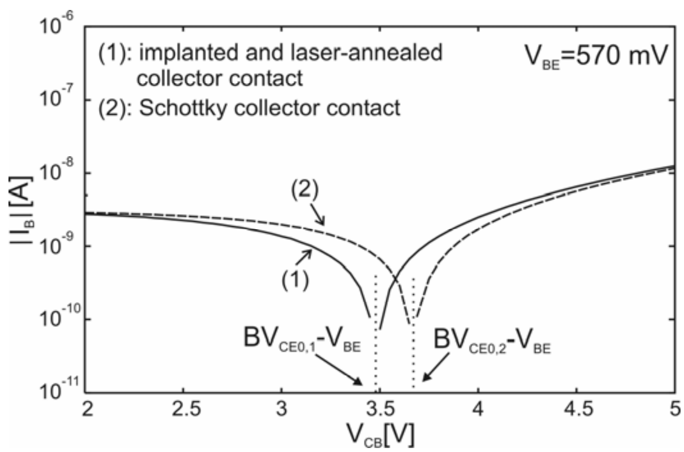

Fig. 5. Measured I_B-V_{CB} characteristics at V_{BE} = 570 mV for SOG NPN's with different collector contact design. The emitter contact area is 40×1 μm^2.

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