

# Small-Delay Fault BIST in High-Speed Chip Interfaces

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**Abstract**— During the past years, due to the decrease of the minimum feature size in CMOS technology, the on-chip clock frequencies have increased dramatically, ranging into the GHz domain. This increase has also pushed the need for higher data-transfer rates between high-speed ICs, in order to optimize the entire PCB system. As a result, the clock/data skew can span tens of clock cycles. In order to cope with this skew, synchronization strategies have been developed which rely on either analogue or digital multi-tap delay-lines. In order for the synchronization mechanism to function properly, all tap-delays of the delay-line should have the same values within few percentages.

This paper presents a technique, based on the oscillation method, to measure tap-delays of a delay-line with an accuracy of  $\pm 10$  ps. A chip has also been implemented in an UMC 0.18  $\mu$ m CMOS technology to prove our assumption. The measurements carried out on the chip confirmed the above mentioned accuracy.

**Keywords**— Delay-fault testing, BIST, High-Speed Chip Interfaces, Oscillation-based

## I. INTRODUCTION

SoC designs being facilitated by the development of new deep-sub-micron technologies. More and more cores can be squeezed on the same die, resulting in ever more complex systems. While the number of devices per SoC is increasing at an exponential rate, the number of access pins of the SoC is not. A huge amount of information generated/received by the SoC should pass via a small number of pins. In order not to hinder the SoC design strategy, the transfer rate per pin should be increased dramatically. High-speed synchronization strategies between ICs have been developed to address this issue.

This paper is organized as follows: section II will provide an overview of some existing high-speed inter-chip synchronization strategies. The main part of every synchronization module is found to be a high-speed multi-tap delay-line. A DFT-aware implementation of such a delay-line will be shown in section III. Section IV will present how an oscillation technique can be used to measure tap delays. The next section V will present the real scheme implemented in the UMC 0.18  $\mu$ m CMOS process. The obtained measurement results are shown in section VI. Fi-

nally, the conclusions are given in section VII.

## II. FUNCTIONAL DESCRIPTIONS OF HIGH-SPEED INTERFACES

Many papers [7, 5, 4, 10] have been published that address the high-speed data synchronization between SoCs. All of the synchronization mechanisms have something in common, being a delay-line either digital or analogue, controlled or not, tapped or not. The synchronization mechanism is dependent on these delay-lines and any manufacturing fault, either catastrophic or not, will hamper the functionality of the synchronization mechanism.

A generic architecture of a high-speed synchronization mechanism is presented in Figure 1. The data can be trans-

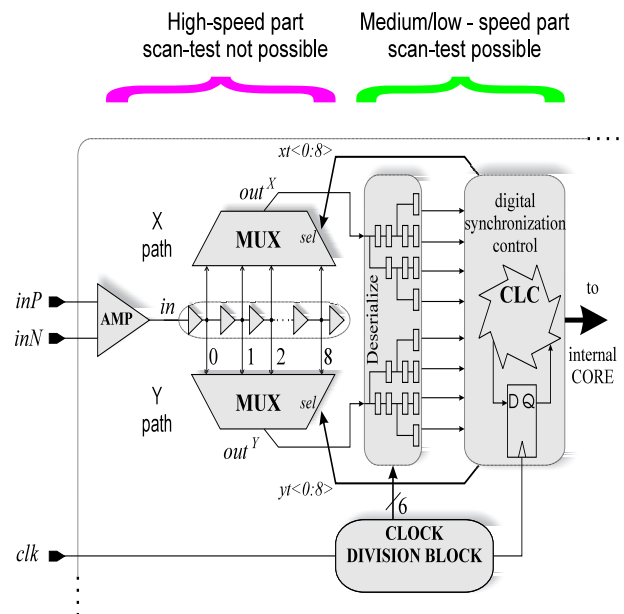


Fig. 1  
 GENERIC ARCHITECTURE OF A HIGH-SPEED  
 SYNCHRONIZATION MECHANISM

mitted from one chip to another using low-voltage differential signaling (LVDS). In Figure 1, the differential inputs are represented by the "inP" and "inN" signals. The transmitted data is synchronous with the clock signal "clk" but

the skew between the data and the clock can span many clock cycles. The differential signal is transformed on-chip in a single-ended signal ("in") by the AMP operational amplifier. This signal then passes a multi-tap delay-line. Different delayed versions of the "in" signal can be selected by the two MUXs. There are two symmetrical paths. These two paths are necessary for the digital synchronization control module, seen on the right side of Figure 1. Following the selection of a certain tap, the data is transformed from serial to parallel by the deserialiser module (Figure 1). This module comprises of only i-ops, which are clocked by different phases and frequencies of the initial clock "clk". The clock division block is the one that takes care of the generation of the clocks for the whole design.

The digital synchronization control module is generating all the select signals for the two access MUXs. In this block, the correct sampling point of the incoming data is calculated and the proper tap is selected.

Testing these type of interfaces in general, and the delay-line in particular is very difficult while using a classical scan-test method. A list of reasons is given below why the scan-test technique cannot be easily applied:

- 2 Most of the time, the high-speed interface design comprises some analogue modules, while the scan-tests intended for digital testing only.
- 2 Even if the synchronization mechanism is pure digital, scan-test cannot be applied due to the negative impact on the speed performance of the interface.
- 2 Scan-test has been mainly designed for stuck-at faults. However, for a high-speed interface especially delay faults are crucial.
- 2 At-speed test using the scan-test strategy can be prohibitively expensive because it can only be performed using costly high-speed ATE systems.
- 2 Scan-test of a delay-line will introduce several undetected stuck-at faults due to the inability to provide different inputs to the access multiplexers [8, pages 48-49].

The digital synchronization module requires that all tap-delay values should be very well matched at the layout level. Therefore a technique to accurately measure these tap-delays within an accuracy of  $\pm 10$ ps had to be developed in our case. The following sections will present a delay-line used as a core part in a high-speed synchronization mechanism together with the differential oscillation technique which is able to measure the tap-delay values with the requested accuracy. In reference [9], a similar measurement accuracy is achieved in simulations by using a mutual exclusion (MUTEX) element. However, an accurately calibrated delay line is required to obtain this accuracy.

### III. BLOCK SCHEME OF A MULTI-TAP DELAY-LINE

Figure 2 shows a multi-tap delay-line scheme used in a high-speed synchronization mechanism. For the time being, the reader should ignore the shaded transmission gates which belong to the DfT hardware. They will be referred to in the next section. An intrinsic buffer, as the one between the "a" and "b" signals, is comprised of an odd number of inverters, where the exact number is application specific. Usually the number of inverters inside a buffer is 2; therefore the delay associated with these tap-delays is very small (around 400ps).

In functional mode, the signal "data\_in" is propagating to the output signals "out<sup>X</sup>" and "out<sup>Y</sup>" via a certain number of taps selected by one of the signals "xt < 0>" :: "xt < 8>" and "yt < 0>" :: "yt < 8>". Only one of the signals "xt < 0>" :: "xt < 8>" can be logic one at a certain moment. This also holds for the signals "yt < 0>" :: "yt < 8>".

### IV. TAP-DELAY MEASUREMENTS USING A DIFFERENTIAL OSCILLATION TECHNIQUE

Oscillation techniques have been extensively used in the past to characterize, measure and analyze delays. The ring oscillator was probably the first design utilized to characterize the speed of a new technology using the oscillation technique. Since then, the same oscillation technique has been also used to test analogue and digital circuits [2, 1]. The power of this technique lies in the fact that twice the average delays, between falling and rising propagation delays, in an oscillation loop is equal with the oscillation period. Therefore, if the oscillation period or the frequency is precisely known, the averaged delay of the oscillation loop can be calculated.

Our aim is to measure the tap-delays of a delay line and not the delay of an oscillation loop. Therefore a plain oscillation technique is not very useful for determining these tap-delays. Instead, a differential oscillation technique as explained below, is used.

The shaded transmission gates in Figure 2 are belonging to our inserted DfT hardware. Their purpose is to generate shorter oscillation periods by closing the oscillation loops inside the delay-line. These short oscillation periods permit an increase in the measurement accuracy due to a smaller influence of the power supply and temperature [8, page 137].

Let us presume that an oscillation loop  $T_{8i6}^X$  (Figure 2) is activated by selecting tap #8 (signal "xt < 8>" is logic one) and closing the loop in front of tap #6 (signal "xf < 6>" is logic one). At the same time the transmission gate in front of tap #6, controlled by signal "xyp < 6>" should be







