SPICE Modeling with NQS effect of Single-Grain Si TFTs using BSIMSOI

Alessandro Baiano, Ryoichi Ishihara, Nobuo Karaki, Satoshi Inoue, Wim Metselaar, and Kees Beenakeer

***Abstract*—Single Grain Thin-Film Transistors (SG-TFTs) fabricated inside a location-controlled grain by μ-Czochralski process exhibit SOI-FETs like performance. To model them, BSIMSOI with a proper modification of the mobility is proposed. The model has been verified for n- and p-channel DC and low frequency AC conditions by comparison with measurement results. Furthermore, the relaxation time approach to model the Non-Quasi-Static (NQS) transient effect of SG-TFTs is also implemented into the BSIMSOI and verified by 2D device simulation.**

***Index Terms*— BSIMSOI, Coincident Site Lattice Grain-Boundary, Non-Quasi-Static Effect, Single-Grain Thin-Film Transistor.**

I. Introduction

SINGLE Grain Thin-Film Transistors (SG-TFTs) fabricated inside a location-controlled grain by μ-Czochralski technology using an excimer laser have reached Silicon-on-Insulator (SOI) performance despite low temperature fabrication (<350 °C) process [1]-[3]. Digital circuits as well as analog and RF circuits could be integrated with display or into vertical direction for applications of Flexible-Electronics or 3D ICs, respectively. Challenges now are to design and to fabricate those circuits by using this technology. To achieve these goals a proper model for circuit simulations is of crucial importance.

Polysilicon TFT models [4]-[7] cannot be employed because they are based on classical long-channel formulation and cannot capture the characteristics of near-submicron TFTs necessary to realize analog and RF circuits; above all, these models use a mobility model that only takes into account the thermionic emission effect across random grain boundaries (GBs). In these models, the mobility increases as a power law for low gate voltages and then becomes constant for high gate voltages. These models cannot be adapted to SG-TFTs by μ-Czochralski technology, as shown in fig. 1. The SG-TFTs show readily increases and gently decreases of g_m-V_{Gate} characteristic, which is very similar to that of SOI MOSFETs owing to the absence of the random GBs. Instead, the SG-TFT channel consists of large silicon crystals separated by few Coincident Site Lattice Grain Boundaries (CSL-GBs), which have much lower electronic activity than random GBs [8]. As a consequence, a model that explicitly takes into account of silicon crystals and CSL-GBs has to be developed. A model of large grain polysilicon has been performed [9] but it is based on the classical long-channel formulation. In this work, a modeling based on BSIMSOI developed by University of California Berkeley [10] is proposed for the modeling of the SG-TFTs. The BSIMSOI is a physically based on SOI model and has been used by many industries for circuit simulation of advanced SOI process. Due to the similarity between SG-TFTs and SOI MOSFETs, lots of the physical effects such as self-heating effect, floating body effect are common to both. BSIMSOI also includes good short channel effects and fully-depletion model important for scaling viewpoint. Furthermore, the model extensively uses smoothing functions, which guarantees continuous and smooth behavior of the model description across all regions of device operation. That ensures

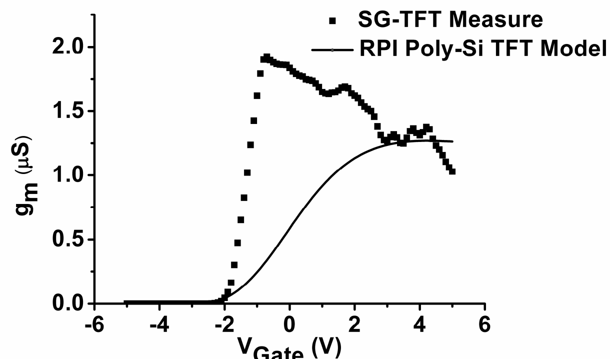

Fig. 1. Mismatch between the measured transconductance characteristic of n-channel SG-TFTs with W = 5 μm and L = 5 μm and 0.05 V drain voltage and the simulated one by using RPI Poly-Si Model.

the model to be robust and efficient when implemented in a SPICE simulator. However, modification of BSIMSOI mobility model is indispensable in order to be adapted to SG-TFTs by the μ-Czochralski technology describing the effect of CSL-GBs present in the channel. This modification is introduced by smoothing function still guaranteeing

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continuous and smooth behavior of equations across of regions. Furthermore, an analysis of the transient effect of SG-TFTs is realized for the first time. For transient condition, the quasi-static (QS) approximation falls down and the non-quasi-static (NQS) effect becomes no negligible any longer. In this work, the relaxation time approach in order to model the NQS effect is proposed and the verification is obtained by comparing with 2D device simulator (DESSIS).

II. Mobility Model Formulation

It has been known that in the SG-TFTs fabricated inside a location-controlled grain by μ-Czochralski process the channel possesses the CSL-GBs. It was suggested that some of these boundaries are electrically active, although the degree is much lower than that of the random grain boundaries in the polysilicon [8]. The motion of carriers across GBs is well known to be described by thermionic emission effect [6]-[7]. The thermionic emission effect has to be taken into account in the BSIMSOI mobility model and that is carried out by a semi-empirical model, which introduces some fitting parameters in the physically based model. Considering a number n of CSL-GBs and n silicon crystals within the channel, according to the standard MOSFET theory corresponding to the on-current condition, and following the same procedure of [9], the channel resistence R_{ch} will be:

$$R_{ch} = nR_G + nR_{GB} = \frac{L}{W\mu_{eff}Q_{invG}} = \frac{nL_G}{W\mu_G Q_{invG}} + \frac{nL_{GB}}{W\mu_{GB}Q_{invGB}} \tag{1}$$

where L and W is channel length and width, respectively, L_G average intra-grain length, L_{GB} average CSL-GB length, μ_{eff} effective carrier mobility in the SG-TFT channel, μ_G is the mobility in the silicon crystal and μ_{GB} is the mobility in the CSL-GB, Q_{invG} is charge in the inversion layer referred to the silicon crystal, and Q_{invGB} is the one referred to the CSL-GB. It is related to the one in the grain by thermionic emission effect [7], [9]:

$$Q_{invGB} = \exp(-qV_b/kT)Q_{invG} \tag{2}$$

Therefore, we can obtain the following relation:

$$\frac{L}{\mu_{eff}} = \frac{L - nL_{GB}}{\mu_G} + \frac{nL_{GB}}{\mu_{GB}\exp(-qV_b(V_{Gate})/kT)} \tag{3}$$

That can be rewrite as following:

$$\frac{1}{\mu_{eff}} = \frac{1-\alpha}{\mu_G} + \frac{\alpha}{\mu_B} \tag{4}$$

with $\alpha = nL_{GB}/L$, μ_G is the mobility expressed in the BSIMSOI and it comes down from universal mobility model and depends on gate voltage as following [10]:

$$\mu_G = \frac{\mu_0}{1 + U_a\left(\frac{V_{gsteff} + 2V_{th}}{T_{ox}}\right) + U_b\left(\frac{V_{gsteff} + 2V_{th}}{T_{ox}}\right)^2} \tag{5}$$

where μ_0 is the zero-field carrier mobility in silicon (equal to 670 cm^2/Vs for NMOS and 250 cm^2/Vs for PMOS), U_a and U_b the fitting parameters used to model the amount of degradation due to the average normal electric field, V_{th} the threshold voltage, V_{gsteff} the smoothing functions that approaches to V_{gs} - V_{th} and T_{ox} the gate oxide thickness. μ_B is the typical thermionic emission relation:

$$\mu_B = \frac{\mu_{GB}}{\exp\left(\frac{qV_b}{kT}\right)} \tag{6}$$

V_b is the potential barrier height, which depends on the gate voltage [7]. For simplicity, the potential barrier height is described by an empirical equation that utilizes the V_{gsteff} smooth function as following:

$$V_b = \frac{V_{max}}{1 + \theta V_{gsteff}} \tag{7}$$

where V_{max} is the maximum potential barrier height. θ is a fitting parameter that describes grain boundary potential lowering when gate potential increases. α describes the quantity of CSL-GBs in the channel and unifies polysilicon and SOI models. It becomes zero when no CSL-GBs are in the channel and the model approaches to the basic BSIMSOI. It can only be used as fitting parameter because the number of CSL-GBs cannot be known.

III. DC and Low Frequency AC Simulation Results

The changes described above are included to the basic BSIMSOI model by using Verilog-A implemented in ADS simulator (following the approach of [11]). DC and low frequency Capacitance-Voltage (CV) characteristics are simulated and compared to measurement results. In order to extract the parameters, optimization algorithm is used. A group device extraction strategy is carried out in order that a complete set of model parameters necessary also for channel length scalability is extracted. Fig. 2 shows measurement and simulation results of transfer and output characteristics of n- and p-channel SG-TFTs with 5 μm channel length and width. As shown in figures, a good agreement between measurements and model is obtained. Fig. 3 shows the transconductance

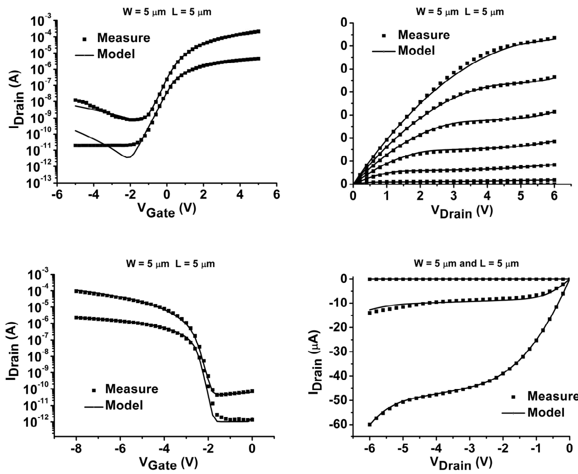

Fig. 2. Measurement and simulation results of n-channel (top) and p-channel (bottom) SG-TFTs transfer and output characteristics.

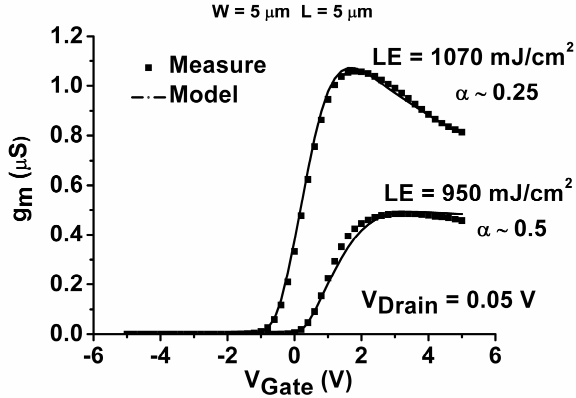

Fig. 3. Measurements of transconductance characteristics of n-channel SG-TFTs with W = 5 μm and L = 5 μm for 0.05 V drain voltage and different laser energy used for the silicon crystallization and simulations for α equal to 0.25 V and 0.5 V.

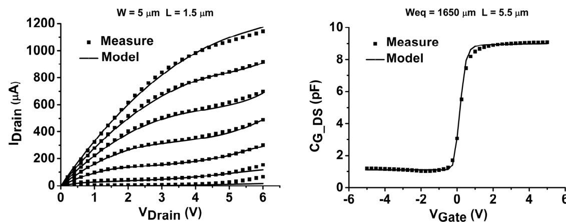

Fig. 4. Output characteristics (left) of n-channel SG-TFTs with W = 5 μm and L = 1.5 μm and capacitance characteristics (right) between gate and drain/source connected together.

measurements of n-channel SG-TFTs by using different energy densities of excimer laser (LE) for the silicon crystallization. The transconductance increases by higher laser energy. That is due to reduction of CSL-GBs in the channel. This effect is well modeled by reducing α from 0.5 down to 0.25, whereas the rest of parameters are fixed. Fig. 4 (left), on the other hand, shows the agreement between measurement and simulation results of output characteristics of n-channel SG-TFTs with a shorter channel length (1.5 μm). That confirms the short channel effects are properly modeled by BSIMSOI. Fig. 4 (right) also shows agreement between measurement and simulation results of low frequency (1Mhz) capacitance-voltage (CV) characteristics between gate and drain-source connected together of 300 SG-TFTs with 5.5 μm channel length and width connected in parallel.

IV. Non-Quasi-Static Effect for Transient Simulations

Circuit simulations are generally based on the quasi-static (QS) approximation, ignoring the carrier transit time along the channel. However, the QS approximation causes enormous error in simulation results with fast time-varying applied voltage as shown in fig. 5. To predict circuit performance accurately for transient and high frequency conditions, a non-quasi-static (NQS) model considering the carrier-transient delay is needed. The delay mechanism could be modeled by

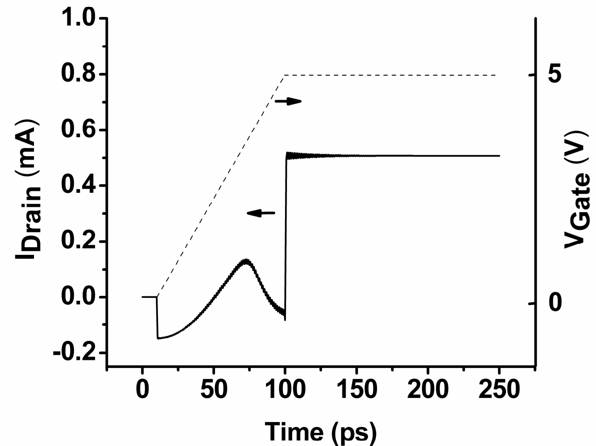

Fig. 5. Drain current response for switching on the gate voltage from 0 V to 5 V using the QS approximation.

segmenting the channel in *n*-pieces, and each piece corresponds to an independent device. However, this modeling incredibly enhances the calculation time due to the increase of the number of transistors to be considered. BSIMSOI, on the other hand, models a physical effective gate resistance incorporating the first order NQS effect as well as the distributed gate electrode resistance for accurately predicting the RF performance [10], [12]. However, this model is not adapted for transient condition comparing with 2D device simulation results, as shown in fig. 6. The 2D device simulations are performed solving the current, continuity and traps equations. The traps are considered uniformly distributed into the channel and their density of state (DOS) are extracted by fitting with DC characteristics. As can be observed in fig. 6, the NQS BSIMSOI model with different α values such as zero and 0.25, where α equal to zero corresponds to SOI-TFT, does

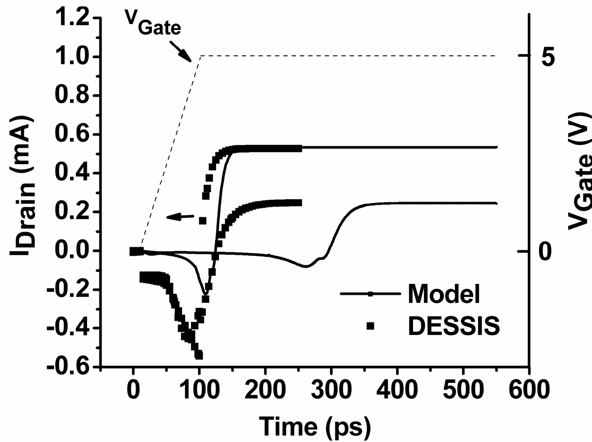

Fig. 6. Mismatch of the drain current response for switching on the gate voltage using the NQS model based on physical effective gate resistance incorporating the first-order NQS effect and the distributed gate electrode resistance for RF application. BSIMSOI is executed by α equal to zero (SOI-TFT) and 0.25.

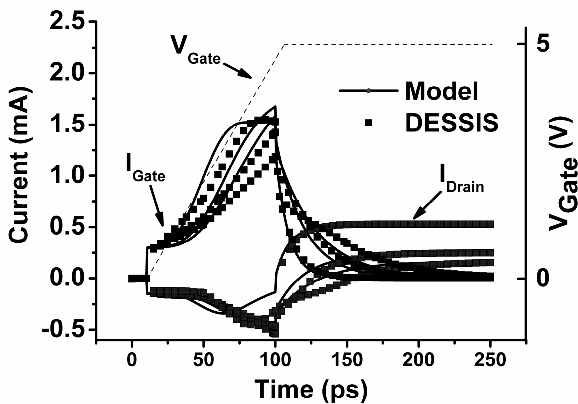

Fig. 7. Drain and gate current response for switching on the gate voltage using the NQS model based on the channel charge relaxation approach. BSIMSOI is executed by α equal to zero (SOI-TFT), 0.25 and 0.5.

not show an agreement with transient of 2D device simulation by changing the DOS of traps into the channel. In fact, 2D device simulation result carries out that, the drain current reached the equilibrium value as a first order RC circuit, and this current rise becomes more gradual by increasing the DOS of traps. The NQS BSIMSOI model, on the other hand, simulates the DOS increase of traps through a longer delay. To adapt the transient model to the 2D device simulation, a NQS model based on the channel charge relaxation approach [13], [14] is implemented in BSIMSOI model by Verilog-A. In this model, an internal node is created to keep track of the amount of deficit or surplus channel charge necessary to reach equilibrium [14]. As shown from fig. 7, a good agreement between the model with α equal to zero, 0.25 and 0.5, and 2D device simulation is obtained. The modeled drain current rise coincides with the 2D simulation one as well as the gate current fall, especially for the range of low α values that is corresponding to the SG-TFT technology. Instead, the increase of DOS produces mismatch because first order of approximation falls down.

V. Conclusion

SPICE modeling of SG-TFTs fabricated inside a location-controlled grain by μ-Czochralski process has been developed. The model employs most of the essential MOS physics from BSIMSOI with an essential modification in order to account the CSL-GBs in the channel. The validity of the proposed mobility model has been demonstrated by comparisons with measurement results. Furthermore, NQS model based on the channel charge relaxation approach has been implemented into BSIMSOI in order to model the transient effect needed for digital circuit design. The agreement between 2D device simulation and NQS model has been shown for a range of DOS of the traps into the channel.

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