Modeling and Scanning Probe Microscopy on Local Electrical Properties of Coincidence Site Lattice Boundaries in Location-Controlled Silicon Islands

Nobuyuki Matsuki, Ryoichi Ishihara, Chen Tao, Yasushi Hiroshima, Satoshi Inoue, Wim Metselaar and Kees Beenakker

Abstract— **We have applied atomic modeling and scanning probe microscopy to investigate electrical activity of coincidence site lattice boundaries (CSLBs) in a location-controlled silicon island that is fabricated by μ-Czochralski method. Scanning capacitance microscopy (SCM) exhibits that capacitance at Σ9 CSLB is less than that of random boundary; this suggests that Σ9 CSLB has less electrical activity than random boundary. This fact can be the evidence for a reason why thin-film transistors fabricated on location-controlled silicon islands by μ-Czochralski method can have SOI-FET like performance despite the CSLBs remain inside the islands.**

Index Terms—**coincidence site lattice boundary, Poly Si, thin-film transistor (TFT), μ-Czochralski.**

I. INTRODUCTION

POLY-silicon (poly-Si) thin films formed from amorphous silicon by excimer-laser crystallization (ELC) process have been extensively applied to fabricate thin-film transistors (TFTs). The most significant advantage on the ELC process is that the highest process temperature can be suppressed at 350 °C or lower, which is appreciable to glassy substrates. A crucial problem desired to be solved for ELC process is how to enlarge the size of silicon grain as well as reduce grain boundaries (GBs). A size of a crystalline grain obtained by conventional ELC methods has stayed less than 1 μm, thus obtained poly-Si TFTs contain a number of random boundaries (RBs) inside the channel (Fig. 1a). RBs become critical electrical barriers, which make carrier mobility decreased significantly; therefore the silicon grain size is highly desired to be enhanced sufficiently larger compared to a channel size. Various methods have been proposed to enhance the grain size such as substrate heating [1], dual-beam method [2], and metal induced (lateral) crystallization (MI(L)C) [3], [4]. No matter how we enlarge the grain size, we still can not avoid chances for boundaries lying in the channel unless if we do not control the location. The grain location is controlled in one-dimensional direction by the lateral growth of the molten Si; such as sequential super lateral growth (SLG) [5], selectively enlarging laser crystallization (SELAX) [6], continuous-wave (CW) laser lateral crystallization [7], and phase-modulated eximer laser annealing (PMELA) [8]. These lateral growth methods enables the channel to be positioned parallel to the GBs (Fig. 1b). The field-effect electron mobility of TFTs approaches 400 cm^2/Vs by these methods. However, the numbers of these parallel GBs vary from device to device; this leads to large variations in the TFT characteristics. The best solution would be eliminating these GBs completely from active channel of the device, i. e. controlling the location of the silicon grains precisely at predetermined positions (Fig. 1c). We have developed μ-Czochralski (grain filter) process that enables controlling positions as well as enlarging the silicon grains [9], [10]. The diameter of a grain can be excess of 9 μm

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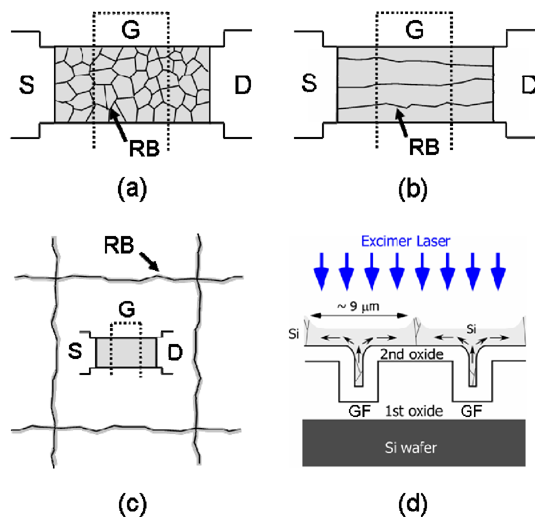


Fig. 1. (a)-(c): Schematic illustration for size and location of grains and random boundary (RB) by different ELC methods. S, D, and G represent source, drain and gate electrode, respectively. (d): Schematic illustration of μ-Czochralski process. GF represents grain filter.

at predetermined positions using the same method (Fig. 1d) [11]. TFTs fabricated in the silicon grains showed 597 cm^2/Vs of field-effect mobility for electrons (μ_{FE}) as the average value. Variation of the mobility is as low as 10%. These high mobility and homogeneous characteristics are attained by the complete location-control of silicon grains. Although the random GBs are almost all eliminated, still some of special boundaries so-called coincidence site lattice boundaries (CSLBs) are present in the silicon grains. Major CSL boundaries observed in the grains are {111}Σ3 and {122}Σ9 CSLBs [12], [13]. The {111}Σ3 is regarded as electrically inactive due to the perfect symmetric twin structure. Theoretical studies predict that {122}Σ9 has no density of states inside the energy gap [14]-[16]; however, an electrical influence on TFT characteristics, which could be caused by tail states for instance, is still unclear. Previous studies on GBs in TFTs have mainly addressed random GBs but not the CSLBs.

In this study, we focused on direct characterization of the electrical properties of the CSLBs in a locarition-controlled silicon grain fabricated by μ-Czochralski method. Atomic modeling with ab-initio calculation and scanning capacitance microscopy (SCM) were applied to estimate the electrical activity of CSLBs.

II. Simulation

We applied ab-initio calculation based on density functional theory (DFT) to calculate density of states (DOS) of {122}Σ9 CSLB. DFT with local density approximation method has advantages especially on calculating covalent materials having strong exchange-correlation effects [17]. A simulation package of MedeA (Material Design co ltd.), which includes “interface builder” and “VASP (Vienna ab-initio simulation package)”, is utilized for this study. First we obtained a basis interface structure using the interface builder and then modified this with referring previous literatures. A unit cell dimensions used to the calculation measures a=3.83 Å, b=11.50 Å, c=19.35 Å and $\alpha=\beta=\gamma=90^o$, and includes 44 atoms. The modeled structure is a {122}Si Σ9 CSL boundary consists of five- and seven-membered rings [18]. These foreign bonds other than normal six-menbered silicon bonds create distortion of short-range order and periodicity of silicon crystalline structure; this could lead to create states at valence and conduction band edges. In the calculation result, Fig. 2, one can see that DOS of the {122}Σ9 CSL boundary has higher DOS concentration at valence and conduction band edges compared to that of a bulk Si model, which consists of 2x2x2 of unit cells with 64 silicon atoms. The deep states extended toward the center of the band gap can become carrier traps. Thus we suppose that the {122}Σ9 CSL is electrically active and would be detected by SCM.

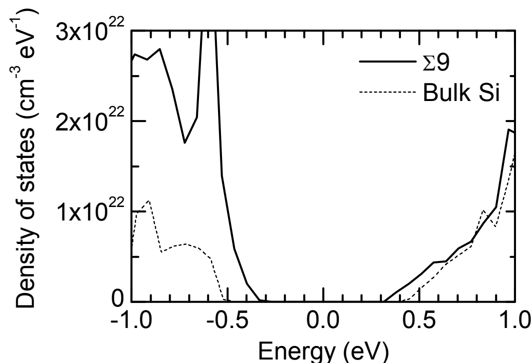


Fig. 2. DOS profile of bulk Si and Si{221}Σ9 CSLB, obtained by ab-initio calculration.

III. Experiment

A. Sample preparation

Fig. 3 shows a schematic cross-section of the sample. A 750-nm-thick of oxide layer was grown on n-type silicon (100) wafer (4 inch of diameter) by the thermal oxidation. Then, grids of holes (1 μm in diameter) were patterned on the oxide layer by reactive ion etching (RIE) in a CHF_3-C_2F_6 plasma. Followed by this oxidation, a 645-nm-thick of oxide layer was deposited by plasma enhanced chemical vapor deposition (PECVD) using tetraethylorthosilicate (TEOS) precursor in order to reduce the diameter of the holes down to around 100 nm [11]. These steps described above lead to form grain filter. An amorphous silicon (a-Si) film with the thickness of 250 nm was sequentially deposited on top of the grain filter in a conventional horizontal hot-wall low pressure chemical vapor deposition (LPCVD) at 550ºC. Consequently, boron was implanted to the a-Si layer with 2.5×10^{11} ions/cm^2. After that, the a-Si film was crystallized by a single shot of XeCl excimer laser with wavelength and duration time of 308 nm and 50 ns, respectively. This laser crystallization was performed with the energy density of 1000 mJ/cm^2 at a temperature 450ºC.

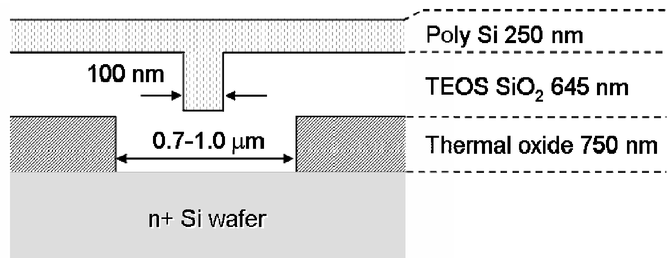


Fig. 3. Schematic cross-section of the sample.

B. Electron Backscatter Diffraction

Prior to SCM measurement, electron back scatter diffraction (EBSD) analysis was carried out to identify CSLBs in the location-controlled silicon grains. An orientation imaging microscopy (OIM^{TM}) system, which is equipped with a scanning electron microscope (SEM) (PHILIPS SEM 525M), was employed for the analysis.

C. Scanning Capacitance Microscopy

SCM was developed by C.C. Williams and his colleagues [19]-[20]. Initially, this method has been utilized for the purpose to investigate doping profile or density of trapped charge [19], [21]-[23]. More recently, this method was applied to observe electrical properties of grain boundaries in

polycrystalline material [24]. We employed a SCM system produced by NT-MDT Co., which was a multi-purpose scanning microscope available for atomic force microscope (AFM), SCM, Kelvin force microscope (KFM), scanning spreading resistance microscope (SSRM) and scanning tunneling microscope (STM). A typical capacitance presenting between a cantilever and a sample (C_{sample}) is as small as 10-40 aF; this value is quite smaller compared to that of the stray (background) capacitance (C_{stray}), which exists between a cantilever and a sample, on the order of sub-pF. In order to eliminate the C_{stray}, a special compensation electrode and circuit [25] was equipped with the unit (Fig. 4). A bias voltage (V_{bias}) ranging from -10 V to +10 V was applied to the sample. A modulation frequency used for the capacitance measurement was 10 MHz. A platinum-coated silicon tip with a silicon cantilever was used as the scanning probe. A scan was made by moving the sample attached on a sample stage that was driven by piezoelectric actuators. SCM detected the local capacitance generated by metal (tip)-insulator (surface native oxide)–semiconductor (silicon) structure. A frequency modulation circuit connected to a cantilever converted a change of the surface capacitance, i. e. a change of surface impedance, to output voltage. A surface morphology was measured by a typical AFM scheme. The SCM and morphology profiles were concurrently acquired and displayed at the same scan.

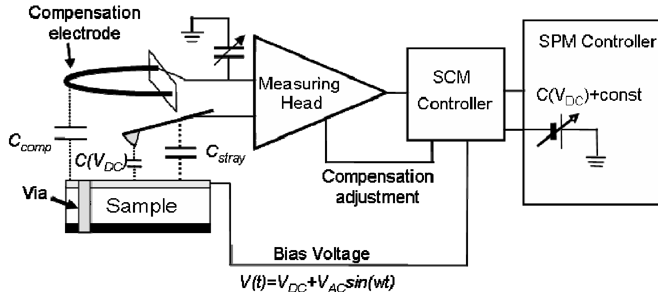


Fig. 4. Schematic diagram of SCM. Compensation electrode plays an important role to reduce the effect of stray capacitance and improve the signal.

IV. Results and Discussion

Fig. 5 shows a SEM image of location-controlled silicon grains. Grains having approximately 5 µm of the square size are formed regularly with centering at grain filter positions. Fig. 6 exhibits EBSD and SCM images of one of the silicon islands. The most and second frequent CSLBs observed by EBSD were Σ3 and Σ9, respectively. This tendency is consistent with our previous result obtained by transmission electron microscopy [13]. Σ3 CSLBs are known to be formed on {111} and {112} planes. Probability of existence of the {112}Σ3 CSLB is quite lower compared to that of the {111}Σ3 due to its instability with a high energy configuration consisting of low density of coincidence site with 5- and 7-membered rings. Σ9 CSLBs has different formation on {122}, {114} and {111}/{115} planes.

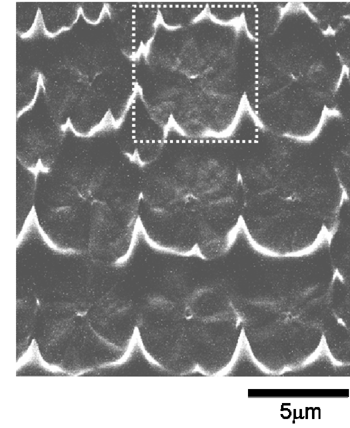


Fig. 5. SEM image of location-controlled silicon grains. A grain enclosed by dotted square is utilized for EBSD analysis and SCM in Fig. 6.

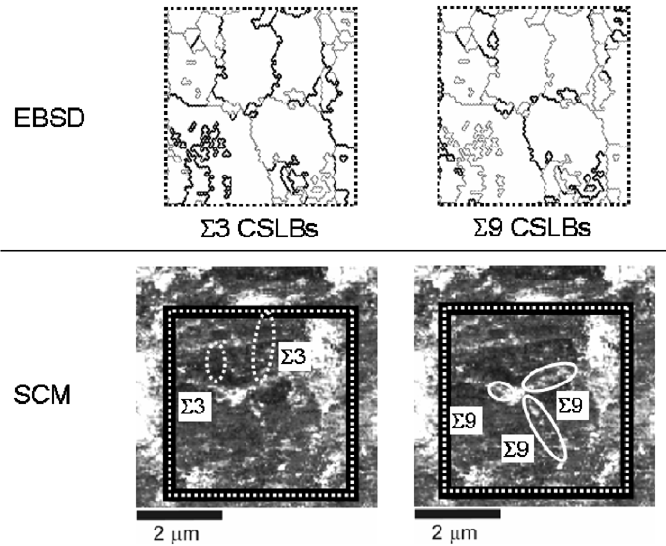
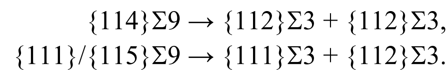


Fig. 6. EBSD analysis results (upper) and SCM images (bottom) of a location-controlled silicon grains. Σ3 CSLBs (left) do not appear on the SCM; on the other hand, Σ9 CSLBs (right) is clearly seen on the SCM.

The {122}Σ9 and {114}Σ9 are the most and second densest coincidence lattice planes (CLPs), respectively. The {111}/{115} has much lower density of CLP. Referring to [12], {114}Σ9 and {111}/{115}Σ9 CSLBs dissociate according to the following reactions:



$$\{114\}\Sigma9 \rightarrow \{112\}\Sigma3 + \{112\}\Sigma3,$$
$$\{111\}/\{115\}\Sigma9 \rightarrow \{111\}\Sigma3 + \{112\}\Sigma3.$$

Hence, from the discussion mentioned above, we presumed that the observed CSLBs are {111}Σ3 and {122}Σ9.

The SCM was performed at V_{bias} = -2 V. Brighter and darker colors in the SCM image represent higher and lower capacitance regions, respectively. One can see that regions corresponding to {122}Σ9 CSLBs exhibit larger capacitance, in contrast, {111}Σ3 CSLBs do not show any evidence of redundant capacitance. More bright (white) regions are concentrated at the periphery of the island. This region is proper for high density of random boundaries, which were generated due to collisions of crystallization frontiers of

adjacent islands. The absence of redundant capacitance at the {111}Σ3 CSLBs is consistent with previous predictions; a {111}Σ3 CSL boundary has no electrical activity due to absence of irregular atomic bonds at the boundary. The experimental results described above verify that {122}Σ9 CSLBs have certain degree of electrical activity but not as high as that of the random grain boundary, that has many defect states in the forbidden gap. This is consistent with our prediction by simulation and previous assumptions.

CONCLUSION

We have calculated density of states of {122} Si Σ9 CSLB using the density functional theory and predicted that the {122}Si Σ9 CSLB has no gap states but certain amount of tail states at the valence and conduction band edges. EBSD analysis determined random boundary, Σ9 and Σ3 CSLBs in silicon islands fabricated by μ-Czochralski. In order to estimate electrical activity of these boundaries, we observed the same silicon islands by SCM. This leads to a conclusion that Σ9 CSL boundary has much less electrical activity than that of random boundary and less influential on performance of TFT fabricated in a silicon grain produced by μ-Czochralski method.

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REFERENCES.

[1] H. Kuriyama, T. Kuwahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, S. Noguchi, S. Kiyama, S. Tsuda, S. Nakano, S. Osumi, and Y. Kuwano., "Improving the uniformity of poly-Si films using a new excimer laser annealing method for giant-microelectronics," *Jpn. J. Appl. Phys.,* Vol. 31, pp. 4550-4554, 1992.

[2] R. Ishihara and M. Matsumura, "Ultra-large grain growth of Si films on glassy substrate,", *Electronic Letters,* vol. 31, pp. 1956-1957, 1995.

[3] S. W. Lee and S. K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Elect. Device Lett.*, vol. 17, pp. 160-162, 1996.

[4] N. Higashi, G. Nalazawa , T. Asano, M. Miyasaka, and J. Stoemenos, "Location and orientation control of Si grain by combining metal-induced lateral crystallization and excimer laser annealing, *Jpn. J. Appl. Phys*., vol. 45, pp. 4347-4350, 2006.

[5] J.S. Im and H. J. Kim, "On the super lateral growth phenomenon observed in excimer laser-induced crystallization of Si thin films, *Apl. Phys. Lett.,* vol. 64. pp. 2303-2305, 1994.

[6] M. Tai, M. Hatano, S. Yamaguchi, T. Noda, S.K. Park, T. Shiba, and M. Ohkura, "Performance of Poly-Si TFTs Fabricated by SELAX," *IEEE Trans. Electr. Devices*, vol. 51, pp. 934-939, 2004.

[7] A. Hara, F. Takeuchi, M. Takei, K. Suga, K. Yoshino, M. Chida, Y. Sano, and N. Sasaki, "High-performance polycrystalline silicon thin film transistors on non-alkali glass produced using continuous wave laser lateral crystallization," *Jpn. J. Appl. Phys.*. vol. 41, pp. L311-313.

[8] C. H. Oh, M. Ozawa, and M. Matsumura, "High-Performance Polycrystalline Silicon Thin Film Transistors on Non-Alkali Glass Produced Using ContinuousWave Laser Lateral Crystallization," *Jpn. J. Appl. Phys*. vol. 37, pp. L492-L495, 1998.

[9] R. Ishihara, P.C. van der Wilt, B.D. van Dijk, A. Burtsev, J.W. Metselaar, and C.I.M Beenakker, "Advanced excimer-laser crystallization process for single-crystalline thin film transistors ," *Thin Solid Films*, vol. 427, pp. 77-85, 2003.

[10] R. Ishihara, Y. Hiroshima, D. Abe, B.D. van Dijk, P.C. van der Wilt, S. Higashi, S. Inoue, T. Shimoda, J.W. Metselaar, and C.I.M. Beenakker, "Single-Grain Si TFTs With ECR-PECVD Gate SiO_2," *IEEE Trans. Electron Devices*, vol. 51, pp. 500-502, 2004.

[11] R. Ishihara, M. He, V. Rana, Y. Hiroshima, S. Inoue, T. Shimoda, J. W. Metselaar, and C.I.M. Beenakker, "Electrical property of coincidence site lattice grain boundary in location-controlled Si island by excimer-laser crystallization," *Thin Solid Films*, vol. 487, pp. 97-101 , 2005.

[12] A. Garg, W. A.T. Clark, and J.P. Hirth, "Dissociated, and faceted large-angle coincident-site-lattice boundaries in silicon," *Philo. Mag, A*, vol. 59, pp. 479-499, 1989.

[13] R. Ishihara, D. Danciu, F. Tichelaar, M. He, Y. Hiroshima, S. Inoue, T. Shimoda, J.W. Metselaar, and C.I.M. Beenakker, "Microstructure characterization of location-controlled Si-islands crystallized by excimer laser in the m-Czochralski (grain filter) process," *J. Cryst. Growth*., vol. 299, pp. 316-321, 2007.

[14] R.E. Thomson and D. J. Chadi, "Theoretical study of the electronic structure of a high-angle tilt boundary in Si," *Phys. Rev. B*, vol. 29, pp. 889-892, 1984.

[15] M. Kohyama and R. Yamamoto, "Theoritical study of grain boundaries in Si: Effects of structural disorder on the local electronic structure and the origin of band tails," *Phys. Rev. B*, vol. 50, pp. 8502-8522, 1994.

[16] M. Kohyama, "Computetional studies of grain boundaries in covalent materials,", *Modellin Simul. Mater. Sci. Eng.* vol. 10, pp. R31-R59, 2002.

[17] W. Kohn and L.J. Sham, "Self-consistent equations including exchange and correlations effects." Phys. Rev., vol. 140, pp. A1133-A1138, 1965.

[18] H. Sawada, H. Ichinose, and M. Kohyama, "Single atomic column onservation in silicon bounadary", *JEOL News*, vol. 38, pp.10-12, 2003.

[19] C.C. Williams, J. Slinkman, W.P. Hough, and H.K. Wickramasinghe, "Lateral dopant profiling with 200 nm resolution by scanning capacitance microscopy," *Appl. Phys. Lett*., vol. 55, pp. 1662-1664, 1989.

[20] Y. Huang and C.C. Williams, and J. Slinkman, "Quantitative two-dimensional dopant profile measurement and inverse modeling by scanning capacitance microscopy," *Appl. Phys. Lett.*, vol. 66, pp. 344-346, 1995.

[21] V.V. Zavyalov, J.S. McMurry, and C. C. Williams, "Scanning capacitance microscope methodology for quantitative analysis of p-n junctions," *J. Appl. Phys.*, vol. 85, pp. 7774-7782, 1999.

[22] H. Tomiye and T. Yao, "Nanometer-scale characterization of lateral p–n junction by scanning capacitance microscope," *Appl. Surf. Sci*, vol. 159-160, pp. 210-219, 2000.

[23] J.W. Hong, S.M. Shin, C. J. Kang, Y. Kuk, and Z. G. Khim, "Local charge trapping and detection of trapped charge by scanning capacitance microscope in the SiO_2/Si system," *Appl. Phys. Lett.*, vol. 75, pp. 1760-1762, 1999.

[24] I. Visoly-Fisherm S.R. Cohen, K. Gartsman, A. Ruzin, and D. Cahen, "Understanding the Beneficial Role of Grain Boundaries in Polycrystalline Solar Cells from Single-Grain-Boundary Scanning Probe Microscopy," *Adv. Funct. Mater.*, vol. 2006, pp. 649-660, 2006.

[25] D.T. Lee, J.P. Pelt, and B. Bhushan, "Instrumentation for direct, low frequency scanning capacitance microscopy, and analysis of position dependent stray capacitance", *Rev Sci. Instrum.*, vol. 73, pp. 3525-3533, 2002.