

A Feedforward Compensated High-Linearity Amplifier

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Abstract—An intermediate-frequency amplifier with feedforward distortion cancellation is described. The amplifier consists of a degenerated cascode compensated by differential common-gate stages. Simulations predict that the amplifier has a power gain of 12.6dB, voltage gain of 13.9dB, and IIP3 of 11.3dBm. The 50Ω noise figure varies from 4.9 to 8.9dB between 10 and 250MHz and consumes 3mA from a 2.2V power supply. Cascading three of these feedforward-compensated amplifiers, each with variable differential loads (25-2500Ω), produces a variable gain amplifier. The power gain is then adjustable between -11.5 and 48.5dB, maximum IIP3 is 7.5dBm, and a minimum 50Ω noise figure of 5.42dB is achieved using 9mA bias current.

Keywords—Feedforward Linearization, Intermodulation Distortion, IF and Baseband Amplifier

I. INTRODUCTION

In a low-IF or superheterodyne receiver, a baseband or intermediate frequency (IF) amplifier precedes the analog-to-digital converter. Fig. 1 shows a block diagram of a typical superheterodyne receiver. The IF amplifier provides gain and regulates the signal level prior to A/D conversion and baseband processing. As the input to this stage is already amplified by preceding stages (i.e., preamplifier and mixer), it must tolerate high input levels, and hence there is a greater emphasis on linearity than noise figure.

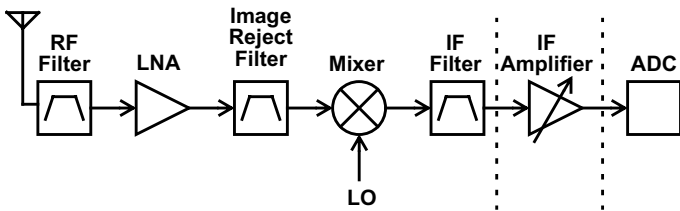


Fig. 1: A typical superheterodyne receiver.

In the IF band (10-250MHz), linearization techniques such as feedback and multi-tanh [1] are commonly implemented. Techniques such as feedforward could also

be employed, although it is almost exclusively used in power amplifier design [2].

This work describes a high-linearity amplifier with feedforward linearization that operates up to 250MHz. The input stage is a feedforward compensated CMOS transconductor [3]. The transconductor consists of two differentially-driven, degenerate common-source stages compensated by degenerate common-gate stages.

II. CIRCUIT DESCRIPTION

A schematic for the feedforward compensated amplifier is shown in Fig. 2. The transconductor stage is a feedforward compensated differential pair similar to that reported in [3]. Common-source ($M_{1,2}$) and common-gate ($M_{3,4}$) stages are used in-place of common-emitter and common-base stages to achieve feedforward distortion linearization in CMOS.

Assuming the input is a single tone excitation with amplitude V_1 , the small-signal drain-source output current is

$$i_{ds} \cong \frac{g_m}{1 + R_{deg}g_m} V_1 \quad (1)$$

where g_m is the transistor's transconductance and R_{deg} is the degeneration resistance. Due to the active devices, weakly nonlinear behaviour is also observed in the output currents. For instance, the second derivative of the small-signal drain-source output current is

$$\frac{d^2 i_{ds}}{dV_1^2} = f(g_m, R_{deg}) V_1^3 \quad (2)$$

A general function is used in eq. 2 to describe the higher-order harmonic components. The amplitude and phase of the third-order harmonic (H3) and intermodulation distortion (IM3) is a function of the degeneration resistance and bias current, as verified in simulation.

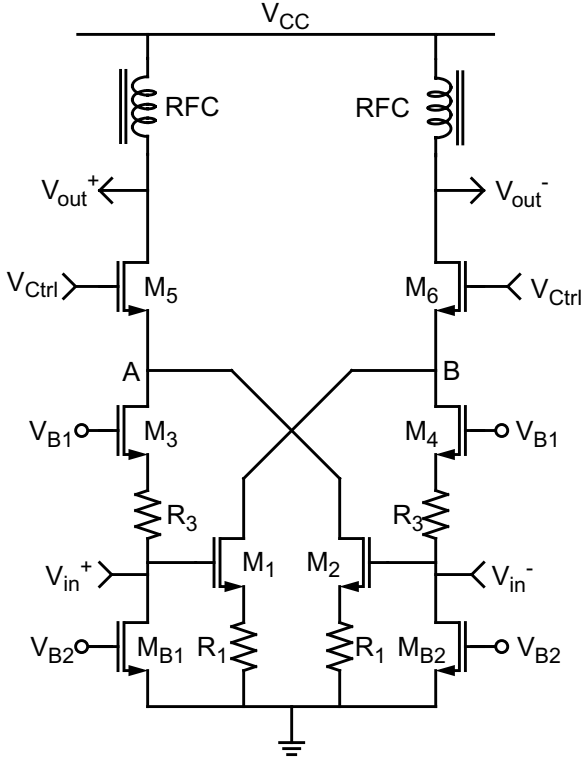


Fig. 2: Amplifier with feedforward compensated transconductance stage.

Distortion compensation for weakly nonlinear behaviour generated by the transistors is achieved by the proper selection of bias current and degeneration resistance. The values are chosen such that the third-order distortion products, both intermodulation and harmonic produced by each stage are of equal magnitude and opposite in phase. When summed at nodes A and B (as in Fig. 2), the distortion tones produced by each stage cancel, thereby producing an output current with lower distortion than for either stage alone.

Cascode transistors M_{5-6} reduce harmonic and intermodulation distortion caused by voltage swings at the drains of M_{1-4} . These transistors act as a current buffer and present an impedance of approximately $1/g_{m5,6}$ to the summing node.

III. SIMULATION

Simulations of the feedforward compensated amplifier (designed in a $0.18\mu\text{m}$ CMOS technology) were carried out using the Cadence Spectre™ simulator. NMOS transistors with a deep n-well option were used for the simulation. This allows the source and bulk terminals to be connected together, and consequently there is no body effect.

Values for transistors sizes, bias currents, and degeneration resistors were determined by iteration from two-tone intermodulation distortion simulations. The values listed in Table 1 are optimized for linearity with

two input tones at 100 and 101MHz with a differential load of $1\text{k}\Omega$

Table 1: Parameters for optimized linearity.

$(W/L)_{M_{1-4}}$	(75/0.18)
$(W/L)_{M_{5-6}}$	(30/0.18)
$(W/L)_{M_{B1-B2}}$	(100/0.50)
$I_{DS,M_{B1-B2}}$	0.75mA
$I_{DS,M_{B3-B4}}$	0.75mA
R_1	15Ω
R_3	20Ω

IV. SINGLE-STAGE AMPLIFIER

Bias currents, degeneration resistances, and transistor sizes used for performance evaluation of the feedforward compensated amplifier are listed in Table 1.

The simulated input reflection coefficient and 50Ω noise figure within the 10-250MHz band are plotted in Fig. 3. An almost constant input impedance is seen (S_{11} of approximately -8.4dB , or $111.4-j3.5\Omega$) whereas the 50Ω noise figure varies between 4.9 and 8.9dB.

Compared to an amplifier with a source-coupled pair input stage [4], the feedforward amplifier offers a closer match to 50Ω but higher noise figure. This is a direct consequence of having the degenerated common-gate stage appearing in parallel with the common-source stage at the input.

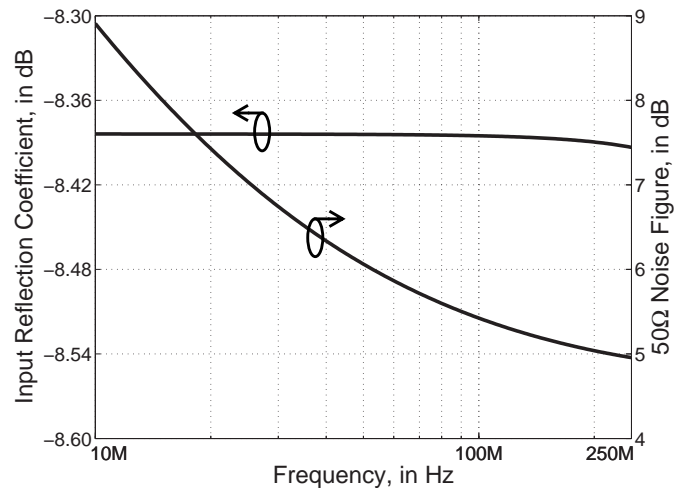


Fig. 3: Input Reflection Coefficient and 50Ω Noise Figure.

The distortion cancellation is verified using three sets of two-tone simulations. The frequencies of the input tones for these simulations were chosen to be: 100/101MHz, 10.0/10.5MHz, and 250/251MHz. The fundamental and IM3 tones for these simulations are

plotted in Fig. 4 (100/101MHz), Fig. 5 (10.0/10.5MHz), and Fig. 6 (250/251MHz) as a function of input power.

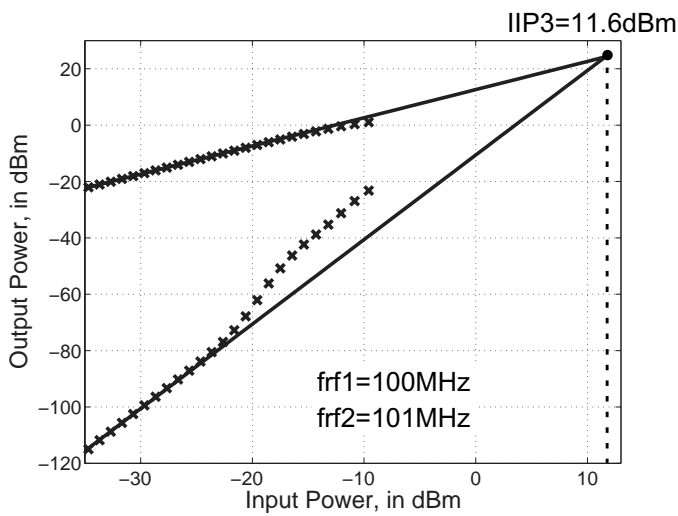


Fig. 4: IP3 plot with input tones around 100MHz.

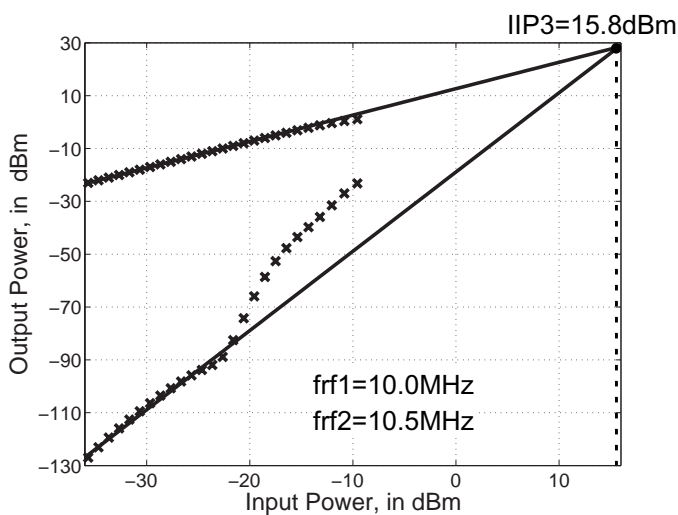


Fig. 5: IP3 plot with input tones around 10MHz.

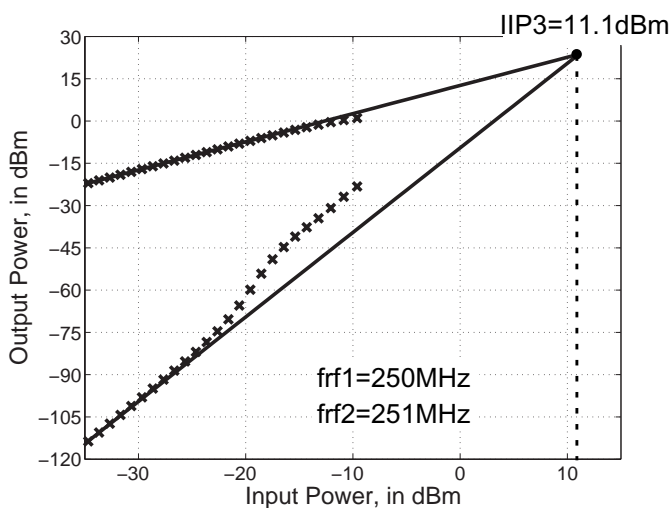


Fig. 6: IP3 plot with input tones around 250MHz.

The power and voltage gains at the three different frequencies are almost the same, at approximately 12.6dB and 13.9dB, respectively. However, the IIP3 performance decreases with increasing frequency. This degradation is caused by gate-source capacitance, since the two feedforward paths experience different phase shifts, and this difference becomes more pronounced as the frequency increases. For the intermodulation distortion simulation at 250MHz, there is approximately 10° deviation from the optimal phase shift for IM distortion cancellation. For applications in the GHz range, transistors with narrower gate widths (and hence lower parasitic capacitance) are required to provide distortion cancellation because of device bandwidth limitations.

All distortion plots show similar trends. The IM distortion slope is three for input power below -19dBm, as expected. The distortion cancellation mechanism is verified by the higher IIP3 performance realized compared to conventional design with coupled differential pairs [1].

For input power between -19 and -21dBm, the slope of the IM3 on the plots is greater than three. Simulation results reveal that mismatch between the IM3 distortion of common-gate and common-source stages is caused by differences in drain-source bias voltages between these two stages [5].

With increasing input voltage, distortion caused by drain-source voltage swing becomes dominant. Since the drain-source bias voltage of the common-gate stage is smaller, at sufficiently high input voltages it will produce more distortion. Although the distortion is now sub-optimal, it is interesting to note that the summed current has less distortion than the contributions from the individual stages.

For input power larger than -21dBm, the distortion generated by the common-gate stage dominates. Summing the drain-source output currents from the two stages results in an overall reduction in IM3, but not perfect cancellation.

V. MULTI-STAGE AMPLIFIER

Simulations of a single feedforward compensated amplifier under different load conditions (25-2500Ω) was also carried out. Results for the gain and linearity for the feedforward amplifier with various load values is shown in Fig. 7. Highest linearity occurs at 1kΩ, which is expected as the design is optimized for this particular value.

A cascade of three feedforward compensated amplifiers form a high linearity variable gain amplifier (VGA). Variable gain is realized by varying the differential load between 25 and 2500Ω for this study. Performance of this VGA is summarized in Table 2.

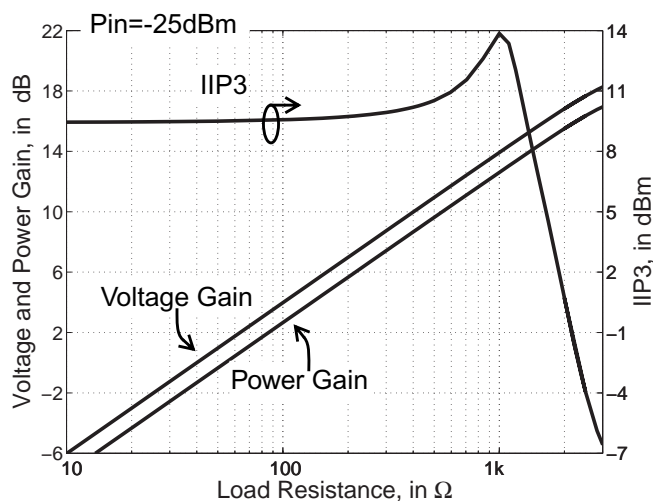


Fig. 7: Dependence of power gain, voltage gain, and linearity on differential load resistance for a single-stage amplifier.

VGAs designed with g_m -boosting differential-pair [6] and multi-tanh [7] are included in Table 2 for comparison. Comparison of the proposed VGA against recently reported designs indicate that the circuit with feedforward linearization can offer superior performance for both power and voltage gain. Linearity of the proposed VGA at 35 and 45dB power gain are -11.3 and -29.5dBm, respectively. This is an improvement of 15 and 16dB improvement when compare to the g_m -boosting differential-pair and multi-tanh designs, respectively.

Table 2: Comparison of simulated proposed circuit with recently reported results from the literature.

	This work	[6]	[7]
Technology	0.18 μ m CMOS	0.35 μ m CMOS	0.4 μ m BiCMOS
Frequency (MHz)	100	246	10.7
Power Gain min/max (dB)	-11.5/48.5	-15/45	35.5
Voltage Gain min/max (dB)	-7.6/52.5	-	-
50 Ω NF (dB)	5.4	8.7	5.2
IIP3 @min/max gain (dBm)	7.5/-35.5	-4/-46	-26.5
Bias Current (mA)	9	9	1.31
Power Supply (V)	2.2	3.5	2.4

VI. CONCLUSION

An IF amplifier intended for 10-250MHz operation was designed. Improved linearity is achieved via feedforward distortion cancellation. Simulations predict that both high gain and linearity are attainable with low-power consumption using this feedforward topology.

Simulations also indicated that a cascade of three stages can realize 7.5dBm IIP3 at a bias current of 9mA.

VII. ACKNOWLEDGEMENTS

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REFERENCE

- [1] P.J.G. van Lieshout and R.J. van de Plassche, "A Power-Efficient, Low-Distortion Variable Gain Amplifier Consisting of Coupled Differential Pairs," *IEEE J. Solid-State Circuits*, Vol. 32, No. 12, pp. 2105-2110, December 1997.
- [2] N. Potheary, *Feedforward Linear Power Amplifiers*, Artech House, 1999.
- [3] S.T. Lim and J.R. Long, "A Feedforward Compensated High-Linearity Differential Transconductor For RF Applications," *Proc. of IEEE International Symposium on Circuits and Systems*, Vol. 1, pp. 105-108, May 2004.
- [4] B. Razavi, *RF Microelectronics*, Prentice Hall 1998.
- [5] R.v. Langevelde et al, "RF-Distortion in Deep-Submicron CMOS Technologies," in *Proc. Int. Electron Devices Meeting*, December 2000, pp. 807-810.
- [6] M.A.I. Mostafa, S.H.K. Embabi, and M. Elmala, "A 60-dB 246-MHz CMOS Variable Gain Amplifier for Subsampling GSM Receivers," *IEEE Transactions on VLSI Systems*, Vol. 11, No. 5, pp. 835-838, October 2003.
- [7] D. Coffing and E. Main, "A Low-Noise Low-Power IF Amplifier with Input and Output Impedance Matching," *Proc. of IEEE BCTM*, pp. 66-69, September 2000.