

# Smart DACs: On the Road Towards Giga-Hz RF DACs

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**Abstract**—Timing errors become dominant in dynamic performance of high-speed and high-resolution current-steering Digital-to-Analog converters (DACs). To improve the dynamic performance and relax the requirements of timing errors in circuit/layout design, two smart calibration/correction techniques, based on on-chip timing error measurement, are proposed. Simulation results show that with mapping technique, the Spurious-free Dynamic Range (SFDR) is improved, e.g. 30dB for linearly distributed interconnection-related timing errors and 10dB for randomly distributed mismatch-related timing errors.

**Index Terms**— Digital-to-Analog Converters, delay control, mapping, timing error measurement

## I. INTRODUCTION

WITH the rapid development of communication and multimedia systems, high-speed and high-resolution DACs are required. New applications, such as Direct-Digital-Synthesis (DDS) and novel wireless transceivers, move DACs to the RF side. In those applications, RF DACs can directly generate RF/IF signals. Consequently, it becomes unnecessary to use traditional mixers for up-conversion. The requirements on anti-aliasing filters, mostly SAW filters, are also reduced or relaxed. These advantages brought by high speed DACs will decrease the whole system's complexity and cost.

Current-steering DACs are a suitable architecture for such applications, because of their intrinsic high speed and driving capabilities. For such DACs, a high dynamic performance (SFDR, SINAD, IMD, etc.) is required. The dynamic performance is affected by many error sources, such as the current switching transient behavior (settling, overshoot, crossing point, etc.), nonlinear output impedance, interference via supply & biasing nodes, timing errors, etc.[1-2]. These error sources introduce harmonic distortion and noise in the output signal, which affect the signal quality. Especially with continuously increasing sampling frequencies, timing errors become a critical problem. Consequently, for a good dynamic performance, timing errors should be minimal by smart design or their negative impact should be alleviated by correction. This paper aims at developing process-independent and on-

chip smart calibration techniques for timing errors.

Two new timing error calibration/correction methods based on on-chip timing error measurement, e.g. mapping algorithm and tunable delay control, are proposed to improve the dynamic performance smartly. Behavior level simulation results show that with a simple mapping optimization algorithm (simple sorting algorithm), the SFDR can be improved by 30dB if the timing errors are linearly distributed, or by 10dB if the timing errors are randomly distributed. Circuit simulation results of an on-chip timing error measurement circuit (phase detector), in a CMOS 0.18um technology, show the feasibility of 1ps timing error measurement accuracy. In section II, a description of timing errors and techniques that address them are given. In section III, a mapping technique is introduced for timing error correction and a statistical analysis of dynamic performance improvement due to mapping is given. In section IV, a calibration technique based on tunable delay buffer is given. Finally, conclusions are drawn in section V.

## II. TIMING ERRORS IN DACs

### A. Timing Error vs Dynamic Performance

Timing errors can be classified into two categories according to their characteristics: global timing errors and local timing errors (relatively different transitions between current sources). Global timing errors include supply disturbance, substrate noise, clock jitter and etc. Power supply disturbance and substrate noise are caused by many sources, such as switching noise introduced by other circuits and signal coupling through common substrate. Clock jitter, often called phase noise, is generated in oscillators, PLLs, clock buffers, etc.

If the input signal is a low frequency sinusoid signal and the output of DAC is NRZ pulse, the Signal-to-Distortion ratio (SDR) caused by clock jitter is given in [3]:

$$SDR = -20 \log_{10} \sigma f_i - 15.96 \text{ dB}$$

$f_i$  is the input signal frequency and sigma is the standard deviation of Gaussian clock jitter distribution. Clock jitter does not limit all dynamic performance [4]. Since clock jitter is independent on input signals, only SNR is affected by clock jitter, not SFDR. While the local timing error, which is input

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signal dependent, is more dominant than global timing error in SFDR. Therefore, this paper is focused on local timing error analysis and optimization. Another reason is that clock jitter is mostly reduced in clock generators, such as PLLs, which is already out of the scope of DACs.

Therefore we focus on local timing errors. Local timing error can also be deterministic and random. Deterministic local timing errors include the errors related to clock/output unbalanced interconnections and process gradients, which are rather deterministic. Examples of random local timing errors are mismatch-related errors of latches, drivers and switches. For high speed DACs, local timing errors deteriorate the dynamic performance dramatically. When the sampling frequency increases, the relative timing errors in one sampling period increase also. We expect that local timing errors can be dominant in very high-speed DAC's dynamic performance. The Matlab simulation results shown in Fig.1 confirm this expectation. The figure shows the SFDR distribution for different timing error deviations using 5000 12-bit segmented current-steering DACs. The standard deviation  $\sigma$  of timing errors was set to 2ps, 5ps and 10ps. The sampling frequency is 500MHz and the input signal frequency is 107MHz. It can be seen from Fig. 1 that larger timing errors result in worse SFDR performance. With increasing the sampling frequency to Giga-Hz, the SFDR will continuously decrease.

### B. Traditional Techniques to Reduce Timing Errors

Several techniques are introduced here, which are proposed to deal with local timing errors.

To decrease deterministic local timing errors, special layout techniques are used in clock/output interconnection, including tree-like interconnection, averaging skew and proper termination [3, 4]. By using these layout techniques, deterministic errors can be minimized at the cost of layout complexity and chip area. Circuit design techniques are also used to decrease systematic errors. For example, dummy switches are often used in a segmented DAC in order to achieve the minimum timing difference between the binary current source part and the thermometer current source part.

To decrease random local timing errors, proper circuit topology and careful optimization are required. For example, optimized latches and buffer circuits were used to avoid generating large timing errors [3, 5]. The spread of random local timing errors in current switches was given in [3]:

$$\sigma(\Delta t) = \frac{A_{VT}}{\sqrt{WLI_D}} (C_G + C_D) = \frac{A_{VT}}{\sqrt{WLI_D}} (WLC_{ox} + C_D)$$

WL is the size of switching transistors and  $I_D$  is the driving current, as shown in Fig.2.  $C_G$  is the gate capacitance of switching transistors.  $C_D$  includes the output capacitance of drivers and interconnection parasitic capacitance.  $A_{VT}$  is the threshold voltage mismatch, which is process dependent.  $\sigma(\Delta t)$  is the deviation of timing errors. A  $\sigma=3ps$  timing distribution was reported in [3]. With reasonable circuit complexity and power consumption, the absolute value of the timing error is hard to decrease below the picosecond level. As a result, developing some techniques, which can correct timing errors

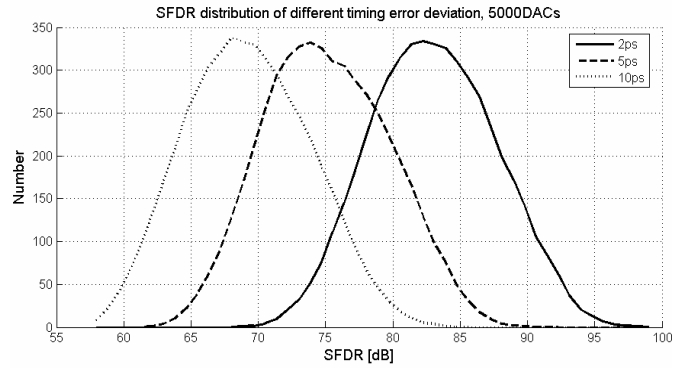


Fig. 1. SFDR distribution for different timing error deviation

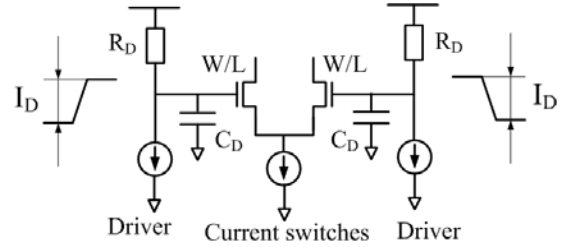


Fig.2. Current switches and drivers

in a smart way, becomes very important.

### III. MAPPING FOR TIMING ERROR CORRECTION

To overcome the physical limitations mentioned above, a mapping technique was proposed in [2,3,6] to digitally correct timing errors. Mapping is well known in the context of switching sequences, which only reduce amplitude errors. In [7], such a method was extended to all amplitude errors in a programmable way. Dynamic Element Matching (DEM) is also a kind of mapping [8]. DEM uses many different mappings to average errors in time, mainly focused on current mismatch (amplitude errors) and regardless of the actual error information. So DEM can only improve the SFDR, but not too much SINAD. However, based on the error information, we can use mapping to improve both SFDR and SINAD, significantly. Mapping was introduced in [2,3,6] to address all local errors (both amplitude and timing errors, especially for timing errors). Such mapping algorithms were reported with simulation results for deterministic local timing errors. The architecture of mapping for a 12-bit 6-6 segmented DAC, based on on-chip timing error measurement, is shown in Fig.3. Timing errors of all thermometer current sources are first measured and then stored into a memory. Based on the mapping optimization algorithm, all thermometer current sources are reordered. The information of the reordered sequence of current sources is called a map. This map is stored into a memory. The binary input will be mapped to corresponding current sources according to this map. As shown in Fig.4 and Fig. 5, behavior level simulation results show that with a simple mapping optimization algorithm (simple sorting algorithm), the SFDR can be improved by 30dB if the timing errors are linearly distributed, or by 10dB if the timing errors are randomly distributed.

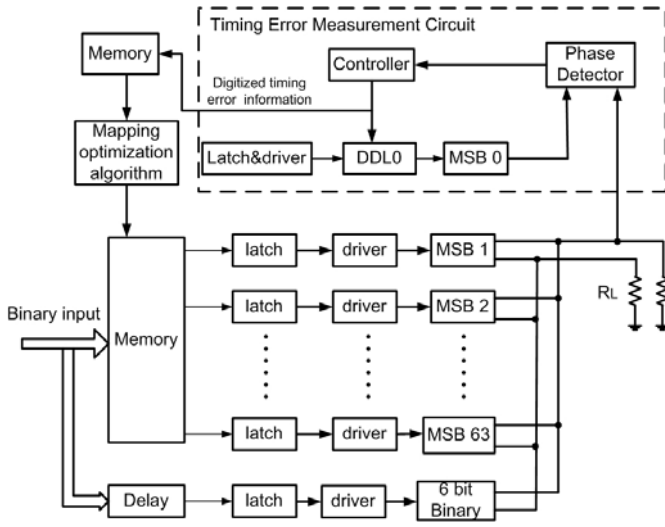


Fig. 3. Architecture of mapping technique

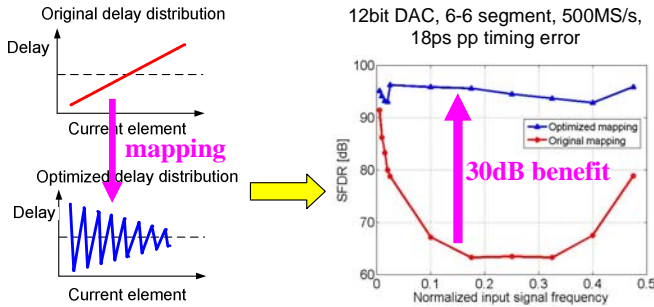


Fig. 4. Mapping for linearly distributed timing error

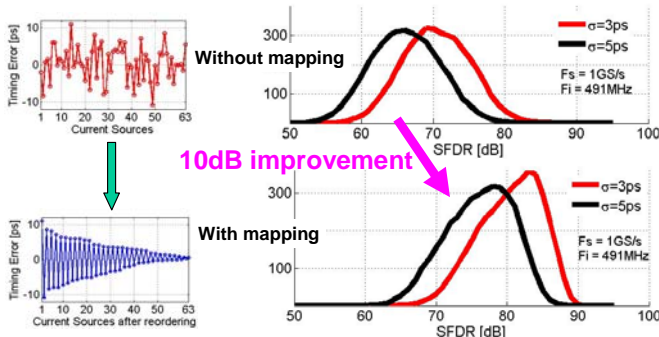


Fig. 5. Mapping for randomly distributed timing error

In Fig.4, a linear timing error distribution which is one of the worst distribution cases is used as original delay distribution. The DAC is 12-bit and 6-6 segmented. The sampling frequency is 200MHz. The maximum delay is 18ps. It can be seen that when the input signal has a very low frequency, the optimized mapping almost has the same SFDR as the original mapping. This is because at a very low signal frequency, the current sources' timing errors can not compensate each other and the current amplitude mismatch will play a dominant role. When the input signal frequency increases, the optimized mapping will reduce the low order harmonic distortion and the SFDR is better than for the

original mapping. For a high signal frequency which is above a quarter of the sampling frequency, the SFDR of the original mapping will increase, as due to the high frequency, the deterministic delay distribution will be randomized, spreading the errors in the frequency domain. However, in practice, other parasitic effects will deteriorate the SFDR at these high frequencies.

In Fig.5, a statistical analysis based on Monte-Carlo simulation is applied for mapping with randomly distributed local timing errors. This statistical analysis is based on a Gaussian timing error distribution, which is a reasonable assumption for a real DAC. It is assumed that in a segmented DAC, both binary current sources and thermometer current sources have the same Gaussian timing error distribution, which is modeled as the time delay for current sources to switch on/off. A 12-bit 6-6 segmented differential current-steering DAC was chosen as an example. The sampling frequency  $F_s$  was 1GS/s and the input signal frequency  $F_i$  was 491MHz. After mapping, the SFDR is improved by around 10dB. This 10dB benefit is almost constant for different timing error deviations with this simple mapping algorithm.

#### IV. CALIBRATION TECHNIQUE BASED ON DELAY CONTROL

The novel architecture of a 12-bit segmented differential current-steering DAC with timing error calibration and measurement circuit is shown in Fig. 6. Each current source has a digital delay buffer (DDB) inserted between its latch and switch transistors to make the delay between them tunable. The DDB's delay is controlled by a binary digital signal, as shown in Fig. 7. The basic idea of timing error calibration is to use a phase detector to measure the phase difference between each current source's output waveform and a reference waveform: if the phase detector's output is 0, it shows that the current source's output waveform comes later than the reference waveform; if the phase detector's output is 1, the current source's output waveform comes earlier than the reference waveform. So ideally, by adjusting each DDB's delay, all current sources' outputs will be synchronized to the reference waveform. The reference waveform is realized by an extra thermometer current source (MSB0). The algorithm controlling measurement and calibration is shown in Fig. 8. This timing error calibration technique is a foreground calibration. Initially, all DDB's inputs are set to mid-scale. The phase difference between MSB0 and MSB1 is measured first by the phase detector. The delay of DDB1 will be increased or decreased until the phase detector's output changes. After calibration, the whole delay of MSB1 is the same as the MSB0. Other current sources' delays will be measured one by one and will be adjusted to make their output synchronous with MSB0. All binary current sources share one DDB circuit (DDB64). They will be handled as one MSB current source and will be measured together, since only one LSB current missing will not affect the accuracy of the measurement too much.

After all current sources' calibrations are complete, there

might be a redundant delay in all DDBs, which means there is an equal delay-offset to all current sources. To minimize the whole propagation time, this redundant delay should be removed. There are two registers which record the maximum and minimum DDB's changed delay value. The offset between these two values and the adjustable range of DDBs is this redundant delay. This offset can not be subtracted directly

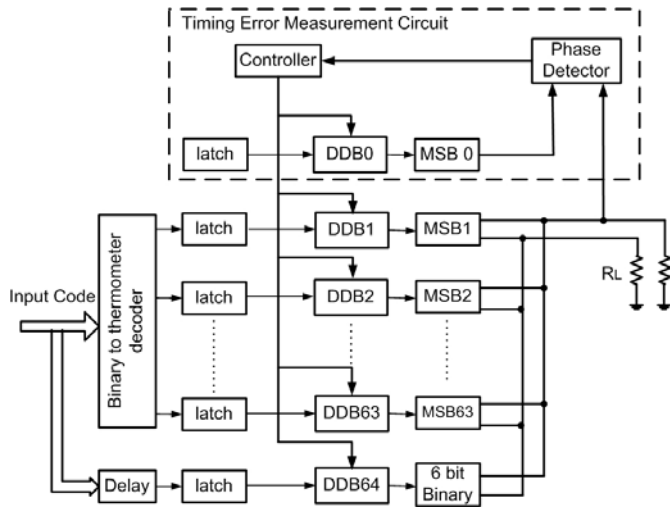
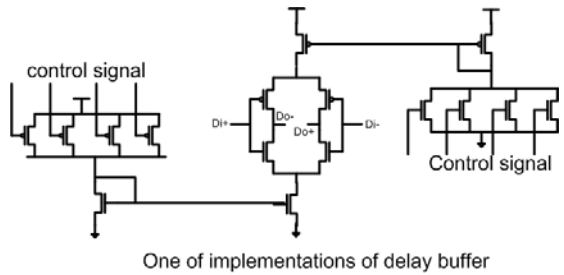


Fig. 6. Architecture for timing tuning



One of implementations of delay buffer

Fig. 7. Delay buffer

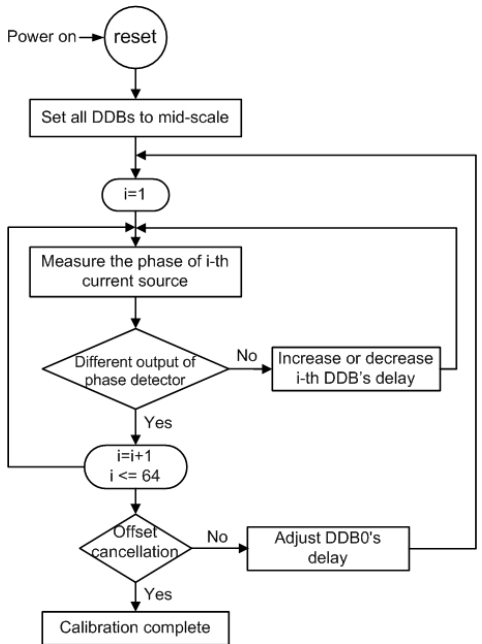


Fig. 8. Calibration algorithm

from the DDB's input because of the DDB's mismatch. DDB0 is used to adjust the reference waveform's delay to minimize this redundant delay. This offset cancellation forces to do calibration again, as shown in Fig. 8. After that, the offset cancellation status is set to YES and the calibration is complete.

The phase detector is the key circuit of the timing error measurement. Normally, the timing error is about several picoseconds to tens of picoseconds [3]-[6]. It is impossible to detect such small phase differences in one clock period. The solution is to use cumulative phase differences in many repetitive input waveforms' cycles. Taking a long time to measure the average phase difference can also eliminate the impact caused by clock jitter. The circuit of a lead-lag phase detector is shown in Fig. 9. The reference waveform and the input waveform are first amplified to get a large swing. Then the outputs of these two amplifiers are fed into two tri-state inverter chains. These two tri-state inverter chains only sample the phase difference between the input waveform's rising edges and the reference waveform's rising edges. An output amplifier will amplify this phase difference and change the output voltage. After tens of cycles, the phase detector will output the correct phase information. For example, if the input waveform is lagging to the reference waveform, the output amplifier will continuously discharge the output voltage in that phase difference time in every cycle until the output voltage reaches GND. A truth table for a lagging waveform is shown

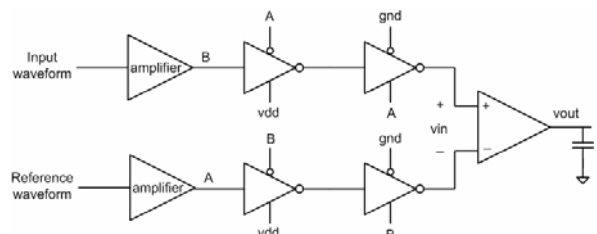


Fig. 9. The phase detector

TABLE I. TRUTH TABLE OF A LAGGING WAVEFORM

A	B	vin	vout
1	1	0	Hold
0	0	0	Hold
0	1 (lagging falling edge)	0	Hold
1	0 (lagging rising edge)	<0	Discharge

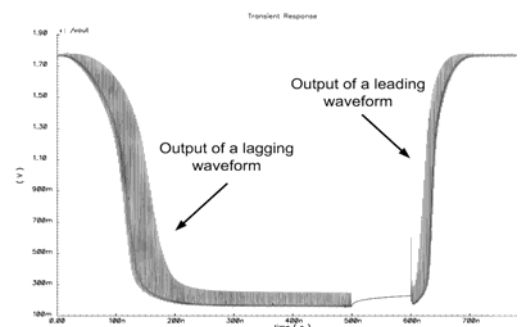


Fig. 10. The simulation results of the phase detector

in Table I. If the input waveform is leading the reference waveform, the output voltage will be charged to VDD. The circuit simulation results of the output of the phase detector are shown in Fig. 10. The circuit is implemented in a CMOS 0.18 $\mu$ m process with 1.8V supply voltage. The sampling frequency of this DAC is 500MHz and the phase difference is 2ps. The time which the phase detector needs to detect a lagging waveform is about 200ns (100 clock cycles), and the time to detect a leading waveform is about 100ns (50 clock cycles). The measurement time depends on the phase difference. A smaller phase difference will take more measurement time.

## V. CONCLUSION

In high speed and high resolution DACs, timing errors have become an important contribution to bad dynamic performance, especially in Multi-GHz range sampling frequency. Simulation results show that minimizing timing errors or alleviating the negative impact of timing errors can improve the SFDR, which has been verified by [1]-[5]. Two smart calibration techniques for timing errors were presented in this paper. These calibration techniques are based on on-chip timing error measurement. These calibration techniques can relax circuit design and layout complexity. Simulation results show that the SFDR is increased significantly after calibration. For example, the SFDR can be improved by 30dB if the timing errors are linearly distributed, or by 10dB if the timing errors are randomly distributed.

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