

Thermal Design of Multifinger Bipolar Transistors

Luigi La Spina¹, Salvatore Russo^{1,2}, Vincenzo d'Alessandro², and Lis K. Nanver¹

Abstract — Design guidelines are provided to improve the thermal stability of three-finger bipolar transistors. Experiments and simulations are conducted on silicon-on-glass BJTs varying the topography of the three fingers, type of isolation, and eventually adding AlN heatspreaders. This results into a change in selfheating and mutual thermal resistances, which are extracted through accurate 3-D numerical simulations. To avoid strong asymmetries between the mutual thermal resistances of two adjacent fingers compared to two non-adjacent fingers, a ‘hexagonal’ topography is proposed.

INDEX TERMS — Aluminum nitride, bipolar junction transistor, heatspreaders, multifinger device, silicon-on-glass.

I. INTRODUCTION

In many circuit applications, transistors have to be designed to handle an appreciable amount of current. In bipolar junction transistors (BJTs), due to the nonuniform voltage drop in the base resistance, phenomena like the emitter crowding [1] can strongly affect the behavior of the device. The most effective approach is to resort to emitter regions with a high perimeter/area ratio, and in particular to several emitter stripes, connected electrically by metallization and separated by interspersing base contacts. Devices with such geometry are known as multifinger transistors.

In modern devices, aggressive isolation schemes result in an augment of the thermal resistance of the transistors; as a consequence, selfheating and thermal coupling among the individual transistors (fingers) can produce localized hot spots in multifinger devices – as well as, more in general, in a complex circuitry – that may cause loss of reliability and eventually lead to device burnout.

Although the behavior of single- and two-finger bipolar transistors has been object of extensive study [2]-[6], the electrothermal analysis of multifinger BJTs has received a reduced attention in literature, yet limited to theoretical analysis and analytical approach [5], [7], [8]. This is the case of three-finger bipolar transistors as well [9], and only very

recently experimental evidence of the current distribution in such devices has been reported [10].

In this contribution, alternative design layouts are experimentally analyzed for three-finger BJTs. Suitable structures are fabricated and measured; all the individual collector currents are monitored simultaneously in order to analyze the electrothermal behavior of each elementary transistor and investigate the difference between a layout and the others. The discussion is supported by 3-D thermal simulations.

II. EXPERIMENTAL MATERIAL AND SIMULATION APPROACH

A. Test structures

The measurements presented in this work are performed on silicon-on-glass NPN bipolar junction transistors [11]. Such devices are in fact suitable for a throughout electrothermal analysis since the whole active area is surrounded by poor thermally conductive materials (like silicon oxide, silicon nitride, and glass) that lead to very high thermal resistance if opportune technological precautions are not taken [12]. All the elementary transistors that form the overall multifinger structure presented in the following have an emitter area of $1 \times 20 \mu\text{m}^2$; they are made in a $0.94\text{-}\mu\text{m}$ -thick silicon island and are insulated by each other by means of trenches or junction isolation. All the BJTs are NPNs with a current gain of about 100 and a description of the three-finger structures considered in this work is given in Table I.

The measurements are performed on a Cascade probe station, equipped with a thermo-chuck, with an Agilent 4156C parameter analyzer and an HP41501 SMU and pulse generator expander.

When used, AlN is deposited directly on the first metal layer of NPN silicon-on-glass bipolar transistors in the manner described in [12], [13].

B. Simulation method

Pure thermal 3-D simulations performed in Comsol [14] are used to extract the matrix of thermal resistances for each structure. The simulation approach adopted in the work is described in details in [15]. However, here the accuracy of the simulations has been improved increasing the number of elements of the mesh to be simulated. Furthermore, the simulations have been performed for a larger number of test structures and the maximum error between measurements and

¹Laboratory of Electronic Components, Technology & Materials (ECTM), Delft Institute of Microsystems and Nanoelectronics (DIMES), Delft University of Technology, P.O. Box 5053, Feldmannweg 17, 2600 GB Delft, The Netherlands. Email: L.laspina@tudelft.nl. Phone: +31-15-2782185; fax: +31-15-2622163.

²Department of Electronics and Telecommunications Engineering, University of Naples Federico II, via Claudio 21, 80125 Naples, Italy.

TABLE I.

DETAILS OF THE THREE-FINGER TEST STRUCTURES PRESENTED IN THIS WORK.

| Device | Isolation | Si area [μm^2] | Center-to-center distance between two adjacent fingers [μm] | Topography | AlN heatspreader thickness [μm] |
|--------------|-----------|-----------------------------|--|------------|--|
| T32-HOR | Trench | $3 \times (1 \times 20)$ | 32 | Horizontal | 0 |
| T15-VER | Trench | $3 \times (1 \times 20)$ | 15 | Vertical | 0 |
| T32-HOR-2AlN | Trench | $3 \times (1 \times 20)$ | 32 | Horizontal | 2 |
| T15-VER-2AlN | Trench | $3 \times (1 \times 20)$ | 15 | Vertical | 2 |
| J62-HOR | Junction | 1800 | 62 | Horizontal | 0 |
| J38-HEX | Junction | 1855 | 38 | Hexagonal | 0 |

simulations has been found to be lower than 10% in all the cases. Also, the metal lines are kept into accounting more precisely than in [15], since the mask layout is imported in Comsol and used to build directly the structure to simulate. The values of thermal conductivity employed are reported in Table II.

Separately switching on each of the three heat sources that represent the elementary transistors, it is possible to extract the values of the selfheating and mutual thermal resistances from the temperature mapping obtained, an example of which is given in Fig. 1 for the device with hexagonal topography J38-HEX. For all the devices studied in this work, the values of both selfheating and mutual thermal resistances found by simulations are reported in Table III.

TABLE II.

THERMAL CONDUCTIVITIES k_{TH} OF THE MATERIALS USED IN THE 3-D FEM SIMULATIONS.

| Material | k_{TH} [$\text{Wm}^{-1}\text{K}^{-1}$] |
|----------------|---|
| Glass | 0.6 |
| Glue | 0.6 |
| SiO_2 | 1 |
| SiN_x | 1 |
| Si | 140 |
| Al | 200 |
| AlN | 28 |

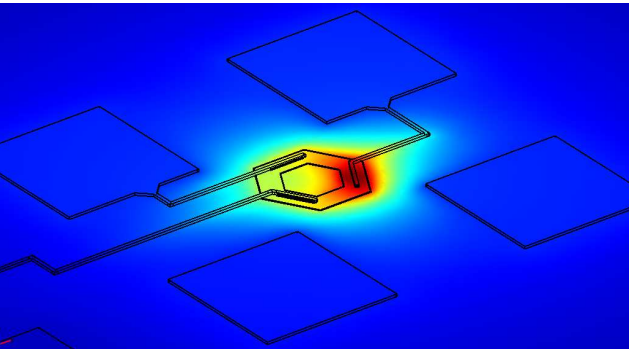


Fig. 1. Simulated temperature mapping of the transistor J38-HEX.

III. RESULTS AND DISCUSSION

Fig. 2 shows microscope images of trench-isolated three-finger silicon-on-glass NPN BJTs in horizontal [Fig. 2(a)] and vertical [Fig. 2(b)] topography. As can be read in Table I, the distances between the centers of two adjacent elementary transistors are 32 and 15 μm for the horizontal and vertical topography, respectively. This means that the emitter pitch is 12 and 14 μm for the horizontal and vertical arrangements, respectively, since each emitter stripe is $1 \times 20 \mu\text{m}^2$.

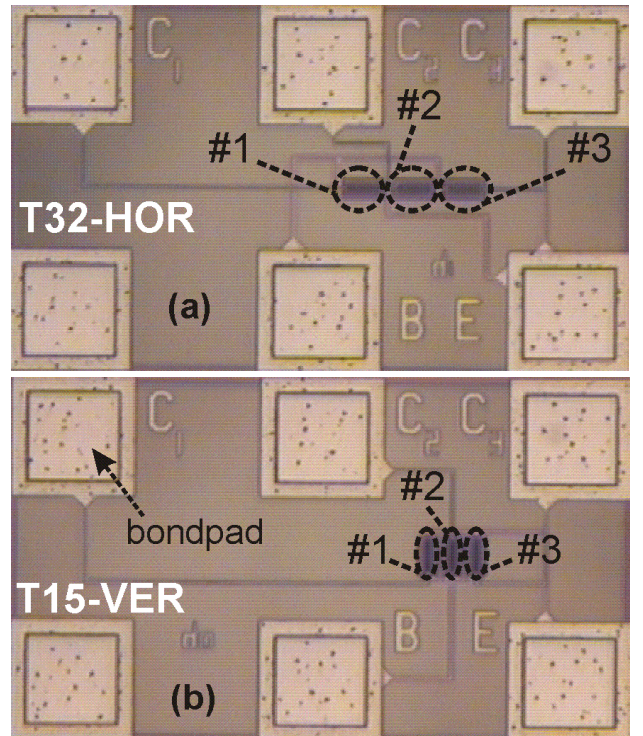


Fig. 2. Trench-isolated three-finger silicon-on-glass BJTs in (a) horizontal and (b) vertical topography.

Observing Fig. 3(a), the improvement of the vertical arrangement, from the thermal standpoint, is marginal compared to the horizontal layout for fully-isolated devices. From an exam of the thermal resistances (Table III), in the device T32-HOR the elementary transistor #3 has the highest selfheating resistance and is the one which takes the biggest amount of

TABLE III.

THERMAL RESISTANCES OF THREE-FINGER BIPOLAR TRANSISTORS AS IN TABLE I.

| Device | R_{TH11} [K/W] | R_{TH22} [K/W] | R_{TH33} [K/W] | $R_{TH12} = R_{TH21}$ [K/W] | $R_{TH13} = R_{TH31}$ [K/W] | $R_{TH23} = R_{TH32}$ [K/W] |
|--------------|---------------------|---------------------|---------------------|--------------------------------|--------------------------------|--------------------------------|
| T32-HOR | 20496 | 19332 | 21315 | 6744 | 3054 | 5619 |
| T15-VER | 18305 | 16532 | 17857 | 7902 | 4724 | 7716 |
| T32-HOR-2AlN | 6698 | 6701 | 6895 | 3382 | 2215 | 3363 |
| T15-VER-2AlN | 6593 | 6340 | 6482 | 4123 | 3172 | 4113 |
| J62-HOR | 15380 | 12697 | 15712 | 5642 | 2945 | 5784 |
| J38-HEX | 13563 | 13464 | 13635 | 8362 | 8444 | 8376 |

current after the onset of thermal instability; with the same argument, it is possible to explain why the hottest finger results to be the element #1 in the device T15-VER. When AlN heatspreaders are absent, indeed, the separation of the individual currents can be triggered by small asymmetries like, for instance, the different distance of each finger compared to the metal lines/bondpads (i.e., in turn, asymmetries in the selfheating thermal resistances of the fingers). In fact, in the case without heatspreaders, the metal lines/bondpads represent a preferential path for the heat to be transferred from the active device area.

When AlN heatspreaders are employed, as illustrated in Fig. 3(b), if compared to the horizontal situation, the thermal coupling is beneficially enhanced in the vertical design (solid lines), despite the slightly bigger emitter pitch. From Fig. 3(b), it can be also noticed that the central finger bears the highest current, since it is affected by the proximity of the two external elementary transistors. Due to the presence of AlN heatspreading layers, the values of selfheating thermal resistances are much lower than those of the corresponding devices without heatspreaders (see Table III), and their asymmetries do not play a dominant role on the onset of thermal instability.

Fig. 4 shows, instead, microscope images of junction-isolated three-finger BJTs, with comparable total silicon area (see Table I), in horizontal [Fig. 4(a)] and so-called ‘hexagonal’ [Fig. 4(b)] topography. In this latter situation, the elementary transistors are placed on a silicon area confined within two concentric regular hexagons, which are the borders of the trenches. Measurements for both situations, for the devices J62-HOR and J38-HEX, are reported in Fig. 5, where it is clear that the second case (solid lines) is much more thermally stable than the horizontal topography (dashed lines). This can be also deduced by the analysis of the thermal resistances reported in Table III. Firstly, the selfheating thermal resistance of the elementary transistor #2 in the structure with horizontal topography J62-HOR is considerably lower, almost 20%, than that of the external fingers. This is due to the fact that the finger in the middle can benefit from a much larger distance from the trenches than the other fingers. On the contrary, this is not the case of the device J38-HEX, where the spreading of the selfheating thermal resistance among the three fingers is confined within about 1%. Secondly, for the device with

horizontal topography, the mutual thermal resistance R_{TH13} between the two non-adjacent fingers is almost half of that of two adjacent fingers. For J38-HEX, instead, due to the nature of the geometry, all the values of the mutual thermal resistances R_{THij} (with $i \neq j$) are very close.

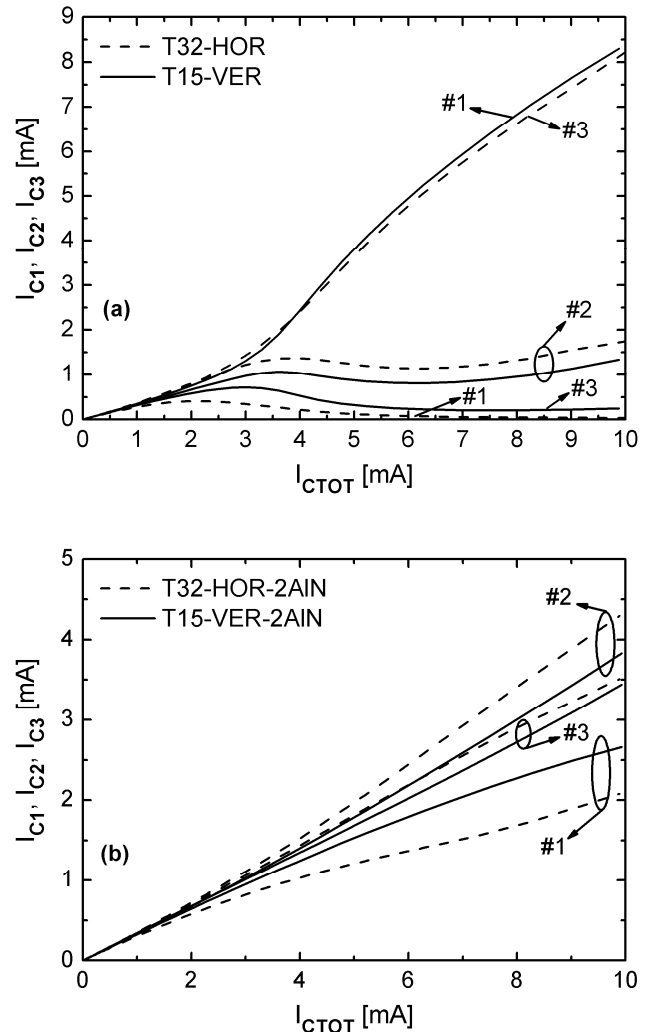


Fig. 3. Measured individual collector currents versus the total collector current I_{CTOT} for layouts as in Fig. 2: (a) fully-isolated transistors without any heatspreader, (b) with the addition of 2- μ m-thick AlN heatspreader.

Furthermore, in Fig. 5, it can be seen, as already noted also for trench-isolated devices without heatspreaders [Fig. 3(a)], that the highest individual collector current is handled by the finger with the highest selfheating thermal resistance (number #3); such asymmetry in R_{THii} is due to small differences among the elementary transistors, that is, e.g., the slightly different position of each finger with respect to the metal lines and bondpads.

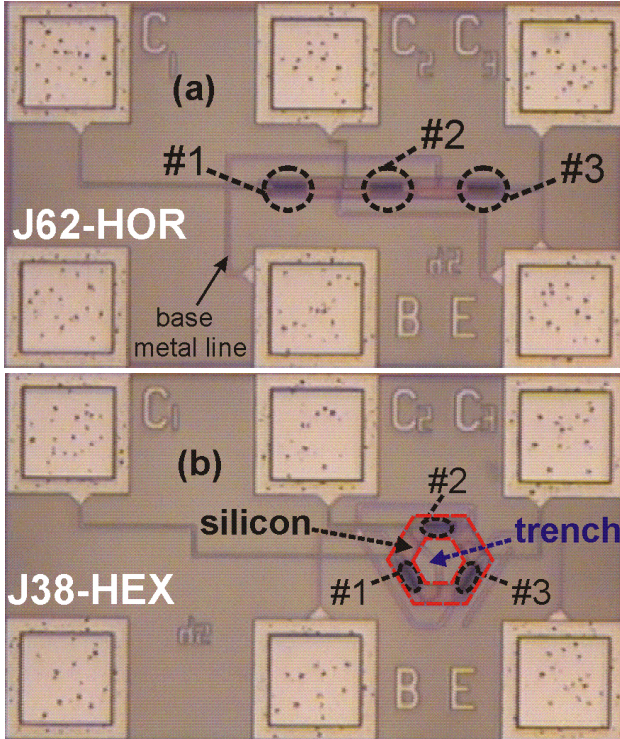


Fig. 4. Junction-isolated three-finger silicon-on-glass BJTs in (a) horizontal and (b) hexagonal topography.

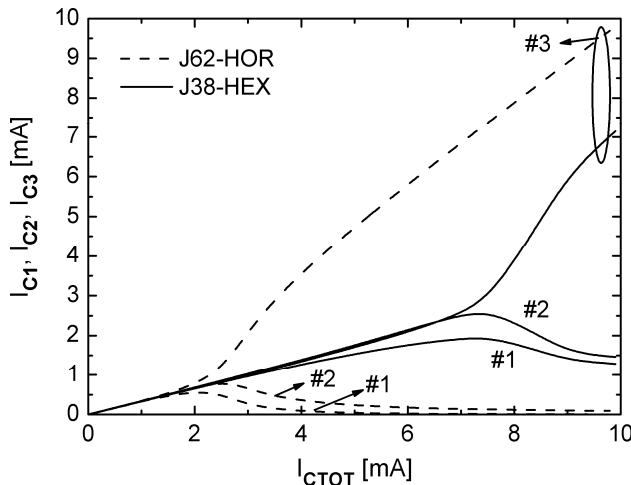


Fig. 5. Measured individual collector currents versus the total collector current I_{CTOT} for layouts as in Fig. 4.

IV. CONCLUSIONS

An experimental analysis of three-finger bipolar transistors has been performed. Suitable test structures have been fabricated with different types of isolation and geometry, as well as with or without AlN heatspreading layers. In order to improve the thermal stability, much more uniform values of selfheating and mutual thermal resistances can be achieved adopting symmetrical layouts of the individual transistors that form the three-finger device. A design where the emitter fingers lie on the three sides of a regular hexagon is suggested. The clear improvement in terms of electrothermal performance has been shown by means of experimental results and substantiated through detailed 3-D thermal-only simulations that supply the value of the thermal resistance matrix.

ACKNOWLEDGMENT

The authors gratefully acknowledge the contributions of the DIMES-ICP cleanroom/measurement-room staff.

REFERENCES

- [1] S. P. Gaur, D. H. Navon, and R. T. Teerlinck, "Transistor design and thermal stability, *IEEE Trans. El. Dev.*, 20, 6, pp. 527-534, 1973.
- [2] W. Liu, "Thermal coupling in 2-finger heterojunction bipolar transistors," *IEEE Trans. El. Dev.*, 42, 6, pp. 1033-1038, 1995.
- [3] N. Nenadović *et al.*, "A back-wafer contacted silicon-on-glass integrated bipolar process – Part II: A novel analysis of thermal breakdown," *IEEE Trans. El. Dev.*, 51, 1, pp. 51-62, 2004.
- [4] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: Part I – Single-finger devices," *IEEE Trans. El. Dev.*, 52, 9, pp. 2009-2021, 2005.
- [5] N. Rinaldi, and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: Part II – Two-finger devices," *IEEE Trans. El. Dev.*, 52, 9, pp. 2022-2033, 2005.
- [6] L. La Spina *et al.*, "Thermally induced current bifurcation in bipolar transistors," *Solid-State Electron.*, 50, pp. 877-888, 2006.
- [7] C.-H. Liao, C.-P. Lee, N. L. Wang, and B. Lin, "Optimum design for a thermally stable multifinger power transistor," *IEEE Trans. El. Dev.*, 49, 5, pp. 902-908, 2002.
- [8] D. J. Walkey, D. Celo, T. J. Smy, and R. K. Surridge, "A thermal design methodology for multifinger bipolar transistor structures," *IEEE Trans. El. Dev.*, 49, 8, pp. 1375-1383, 2002.
- [9] N. Nenadović, V. d'Alessandro, L. La Spina, N. Rinaldi, and L. K. Nanver, "Restabilizing mechanisms after the onset of thermal instability in bipolar transistors," *IEEE Trans. El. Dev.*, 53, 4, pp. 643-653, 2006.
- [10] V. d'Alessandro, L. La Spina, N. Rinaldi, and L. K. Nanver, "SOA reduction due to combined electrothermal and avalanche effects in multifinger bipolar transistors," to be presented at *IEEE BCTM 2008*, Monterey, California.
- [11] L. K. Nanver *et al.*, "A back-wafer contacted silicon-on-glass integrated bipolar process – Part I: The conflict electrical versus thermal isolation," *IEEE Trans. El. Dev.*, 51, 1, pp. 42-50, 2004.
- [12] L. La Spina, E. Iborra, H. Schellevis, M. Clement, J. Olivares, and L. K. Nanver, "Aluminum nitride for heatspreading in RF IC's," *Solid-State Electronics*, vol. 52, no. 9, pp. 1359-63, 2008.
- [13] L. La Spina, H. Schellevis, N. Nenadović, and L. K. Nanver, "PVD aluminium nitride as heat spreader in silicon-on-glass technology," *Proc. IEEE MIEL*, 2006, pp. 365-368.
- [14] Comsol Multiphysics 3.4, *User's Guide*, Comsol AB, 2007.
- [15] L. La Spina, I. Marano, V. d'Alessandro, H. Schellevis, and L. K. Nanver, "Aluminium-nitride thin-film heatspreaders integrated in bipolar transistors," *Proc. IEEE EuroSimE*, 2008, pp. 99-103.