Mix-and-match Lithography Based Ultrathin-body SOI Nanowires and Schottky-S/D-FETs

Frank Wessely, *Student Member IEEE*, Lorraine Rispal, *Student Member IEEE*, Udo Schwalke, *Member IEEE*

Abstract—**In this paper a proof of concept for a new type of devices on silicon-on-insulator material is presented. In conventional CMOS fabrication ion-implantation and subsequent high-temperature annealing steps prohibit the use of promising alternative materials, like sensitive rare earth high-κ dielectrics and metal-gate electrodes. This limitation can be circumvented by a fabrication process that completely abandon the use of implantation steps and high-temperature annealing at all. In this work we fabricate nanowires and Schottky-S/D MOSFETs and investigate their electrical behavior.**

***Index Terms*— SOI, Si-Nanowires, Schottky-Source/Drain, Tri-gate Transistor**

I. INTRODUCTION

Since conventional MOSFET technology is more and more driven towards its physical limits, novel devices – like nanowires – have been proposed for the 'beyond 10nm gate-length era'. Problems arising from the conventional fabrication of i.e. ultra-shallow source-drain-junctions (S/D), lightly doped drain structures, pocket halo implantations and retrograde body doping [1] could be circumvented by the introduction of Schottky-barrier-S/D-contacts [2].

The aim of the work is to fabricate and characterize Schottky-S/D-nanowires and tri-gate Schottky-S/D-transistors structurally and electrically. The main advance of this type of devices is that they do not require any ion-implantation and subsequent high-temperature anneals at all. The lack of heat treatment, formerly required to anneal the crystalline defects and activate doping, opens the possibility to the use of other types of gate dielectrics, like high-κ materials, that are known to be sensitive to heat, as well as different S/D-metallization.

However, the challenge lies in the compatibility of the fabrication process to the well-established CMOS fabrication processes and equipment.

Metals like gold etc. used for nanowire growth are therefore prohibited since these materials are known to be a carrier-lifetime killer in conventional CMOS technology [3]. This has particularly to be taken into account if one thinks of a hybrid silicon-nanowire/CMOS technology. Therefore the fabrication of nanowires and transistors is carried out on ultrathin-body silicon-on-insulator substrates with a corresponding top-silicon thickness of 30 and 120nm.

II. FABRICATION PROCESS

A. Preparation of the substrates

Starting from plain n- or p-type SOI substrates, a CVD-oxide of 50nm is deposited on top of the silicon surface acting as a supportive underlayer for the required alignment marks for electron beam lithography. The chromium alignment marks are patterned via standard optical lithography. The pattering takes place in $Ce(SO_4)_2$-acid, followed by a buffered HF etch to remove the supportive oxidic underlayer from the latter active area (see Fig. 1a).

B. Formation of the active area

The active area of the nanowire and tri gate devices is patterned via electron beam lithography. The electron beam lithography is performed on a Hitachi SEM type S806C which has been modified using a RAITH lithography controller unit.

Inside the $200x200\mu m^2$ sized write-fields, surrounded by the alignment marks, 80-100nm wide fins are patterned into a negative electron beam resist. The structure is transferred into the top silicon layer of the SOI substrate via a highly selective reactive ion etching step in HBr-atmosphere, performed on an Oxford Instruments Plasmalab System 100 with an inductively coupled plasma source (see Fig. 1b).

This structure defines the active area of the nanowires and Schottky-FETs. A subsequent thermal oxidation step via rapid thermal oxidation (RTO) results in the formation of the gate stack of the corresponding Schottky-S/D-tri-gate structure. Fig. 1c shows a top view of the layout of such a transistor.

C. Forming the Schottky-contact

In a following electron beam lithography step, the contact

Manuscript received October 1, 2007.

F. Wessely is with the Institute for Semiconductor Technology and Nanoelectronics at the Darmstadt University of Technology (contact information: phone:+496151163931, fax:+496151165233, email: wessely@iht.tu-darmstadt.de)

L.Rispal is with the Institute for Semiconductor Technology and Nanoelectronics at the Darmstadt University of Technology

U. Schwalke is the head of the Institute for Semiconductor Technology and Nanoelectronics at the Darmstadt University of Technology

(for more information see: www.iht.tu-darmstadt.de)

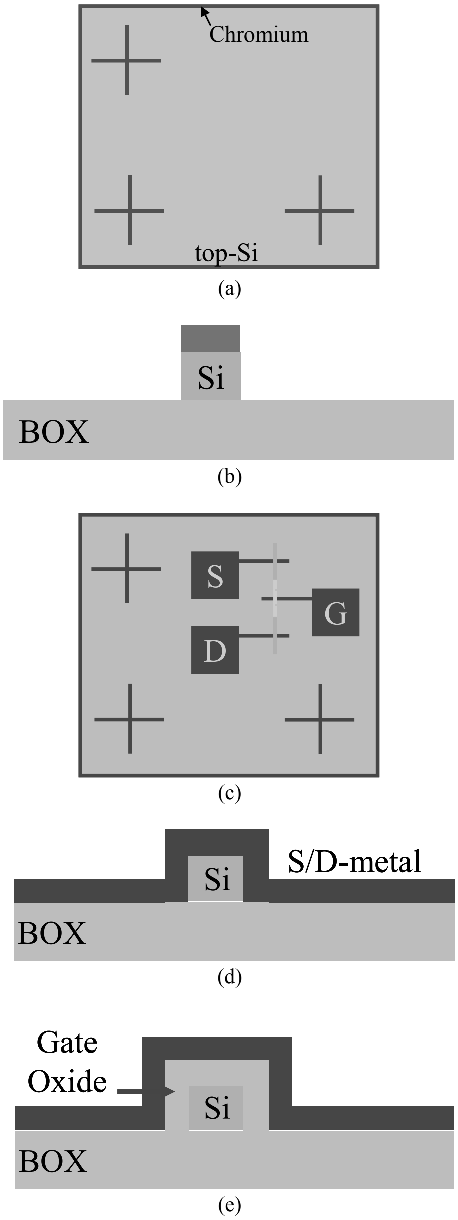


Fig. 1. (a) Patterned and structured write-field with alignment marks for subsequent electron beam lithography (b) silicon fin after HBr- plasma etching (c) top view of the layout of the Schottky-S/D-FET structure with (d) corresponding S/D region and (e) corresponding gate contact. For the nanowire structure, the gate contact is obsolete.

regions for the SOI-nanowires and the tri-gate-MOSFETs are formed alike. However, in case of the MOSFET devices, S/D-windows have to be defined and liberated from the afore thermally grown oxide (see Fig. 1d, e). The contacts are deposited via electron-gun evaporation, followed by a lift-off step and forming gas anneal at 425°C in H_2/N_2 atmosphere. The material chosen as contact defines the Schottky-barrier. Aluminum was used for our proof-of-concept devices since the evaporation and lift-of procedure is well established.

With Aluminum, a Schottky-Barrier of $\Phi_{MS,n}$=-0.3V for n-type and $\Phi_{MS,p}$=-0.9V for p-type substrates [4] is achieved with a constant top-silicon doping of $N=1\bullet10^{15}cm^{-3}$ for either n- and p-type doped material.

III. STRUCTURAL CHARACTERISATION

Structural inline process control is performed with a Dimension 3100 atomic force microscope (AFM) from Veeco Instruments as well as with the Hitachi scanning electron microscope (SEM) type S806C. The AFM is used to gain height information and three-dimensional captures (see Fig. 2a, b) of the fabricated devices. The SEM is used to characterize the line width of the fabricated active areas. The SEM characterization yields active areas of 100nm in width (see section profile in Fig. 2a). The nanowire length is characterized to 60µm. The tri-gate FETs have a W/L ratio of 25/1 for the 50nm Top-Si-SOI substrates and 500/46 (≈10/1) for the 180nm Top-Si-SOI substrates.

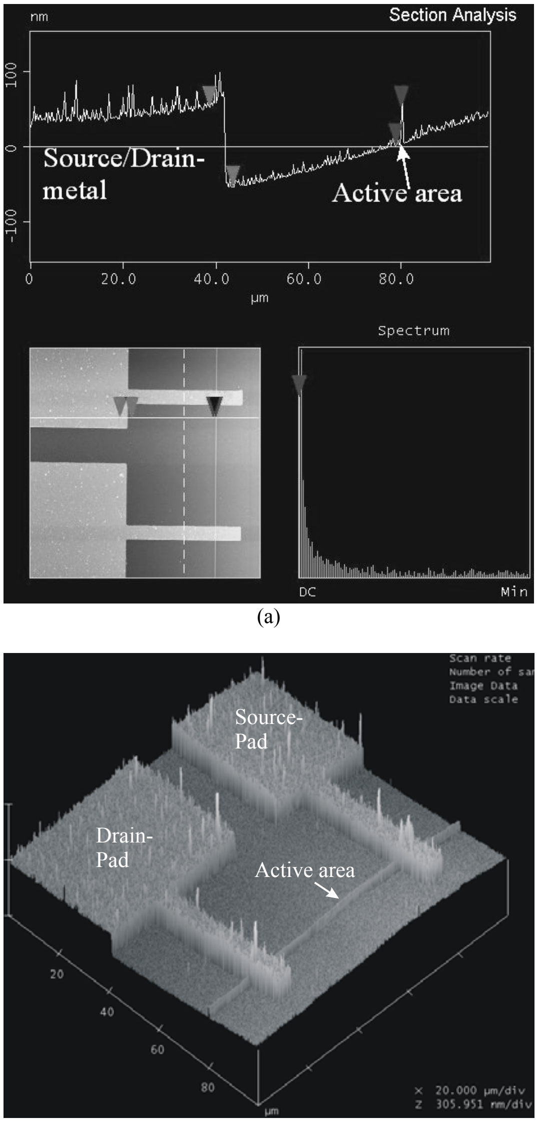
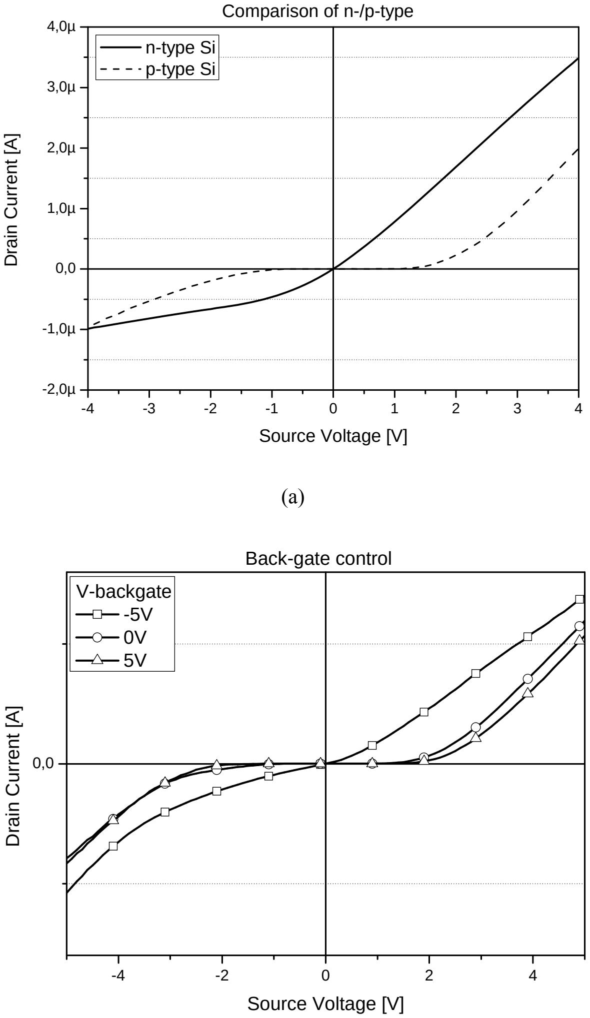


Fig. 2. (a) AFM section profile of a fabricated nanowire device. The left cursor-pair indicates a thickness of 110nm for the Al-contact Pad, the right cursor-pair gives the height of the active area with 50nm. (b) 3D plot of corresponding structure.

IV. ELECTRICAL CHARACTERIZATION

The fabricated devices were electrically characterized with a Keithley Instruments Model 4200-SCS parameter analyzer. I_S/V_D-characteristics, as well as subthreshold characteristics were obtained. Fig. 3 shows some of the collected data for an active area thickness of 50nm.



(a)

(b)

Fig. 3. Output characteristic of (a) a nanowire structure on n- and p-type silicon and (b) a Schottky-S/D-barrier FET on n-type silicon.

In Fig. 3a the two terminal nanowire is compared for n- and p-type silicon respectively. In case of p-type material the nanowire behaves almost like a normal resistor. However, in the case of n-type material it behaves like a Schottky-barrier contact. The symmetrical characteristic of the contact relies on the fact that both, source and drain, contacts are fabricated from aluminum. In Fig. 3b the n-type nanowire is additionally contacted with a gate contact. The output characteristics show depletion-mode MOSFET-like behavior, where a negative gate voltage cuts off the channel at values of $V_G < -0.6V$.

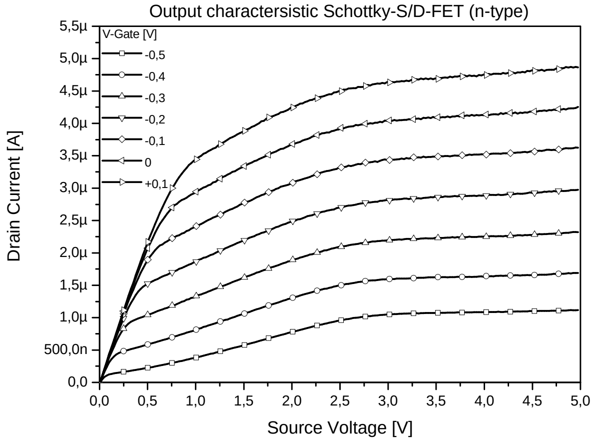


Fig. 4. Control of the n-type Nanowire channel via the back gate of the SOI-handle Wafer

Fig. 4 confirms that the Schottky-barrier height of the n-type nanowire can be modulated via the applied voltage at the backside of the SOI wafer. As a result, the total resistance can be controlled. For backgate voltages of $V_{BG} < -5V$ the Nanowire behaves like an ohmic wire, for $V_{BG} > -5V$ it remains Schottky like.

V. CONCLUSION

Schottky S/D-nanowires and tri-gate Schottky-S/D-MOSFETs have been produced as a first proof of concept. The observed electrical behavior is in agreement with the theoretical expectations. Further work will include the comparison of different CMOS compatible damascene metallization schemes, as well as the implementation of rare-earth oxides as high-κ dielectrics.

REFERENCES

[1] A.C. Lamb et.al., *A 50nm channel vertical MOSFET concept incorporating a retrograde channel and a dielectric pocket*

[2] Saitoh, W. et.al, *35 nm metal gate SOI-p-MOSFETs with PtSi Schottky source/drain*, Device Research Conference Digest, 1999 57th Annual Volume , Issue , 1999 Page(s):30 - 31

[3] Grove A.S., *Physics and Technology of semiconductor devices,* Wiley

[4] S.M. Sze, *Physics of semiconductor devices*, 2nd Edition, 1981

AUTHORS

Frank Wessely received his diploma degree in electrical engineering from Darmstadt University of Technology in 2005. Currently, he is working towards the Ph.D. degree at the Institute for Semiconductor Technology and Nanoelectronics at the same University. His dissertation focuses on the integration and characterization of novel devices and integration concepts for the beyond-CMOS-era.

Lorraine Rispal received her diploma degree in electrical engineering from Darmstadt University of Technology in 2004. Currently, she is working towards the Ph.D. degree at the Institute for Semiconductor Technology and Nanoelectronics at the same University. Her dissertation focuses on the fabrication and characterization of Carbon Nanotubes (CNT).

Udo Schwalke was awarded a Research Fellowship from the Alexander-von-Humboldt-Foundation for his Ph.D. thesis in 1984. During 1984 - 1986, he was appointed Caltech Research Fellow at the California Institute of Technology, USA. In 1987, he joined the Siemens AG, R&D Microelectronics in Munich, Germany. From 1990-1992 he was responsible for the 64Mb DRAM device design at IBM/Siemens, USA. Subsequently, at Infineon Technologies AG (the former Siemens Semiconductor Group) he worked on novel process architectures and device reliability issues. Since August 2001, Dr. Schwalke is Professor in Electrical Engineering and the Managing Director of the Institute for Semiconductor Technology at Darmstadt University of Technology. Prof. Schwalke has served as expert evaluator and reviewer for the European Commission and is a member of the IEE, IEEE and ECS. He has authored or co-authored more than 80 technical papers and holds several patents. Currently his research interests are focused on nanoscale CMOS technologies and molecular nanoelectronics.