On the Aluminum-Mediated Solid-Phase Epitaxy of Silicon at 300ºC

A. Sammak, Y. Civale and L. K. Nanver

Abstract—**A fully CMOS-compatible process, based on silicon epitaxial deposition from physical vapour-deposited amorphous Si (α-Si) through aluminium, was recently proposed. This technique has been proven to be reliable for creating low-ohmic p$^+$-contacts and ultra shallow ultra-abrupt p$^+$-n junctions. Moreover, this Al-mediated SPE-Si process is also characterized by maximum processing temperature of 400°C, for which transient-enhanced diffusion (TED) effects are avoided. However, the reduction of the process temperature down to 300 °C remains very interesting for many applications, in particular for further integration of SPE-Si modules into the silicon-on-glass (SOG) processes.**

***Index Terms*—Al-doping, elevated contacts, low-ohmic contacts, low-temperature processing, solid-phase epitaxy**

I. INTRODUCTION

THIS PAPER presents a process that can be performed from 300ºC to 400ºC, for fabricating epitaxially deposited p+ Si islands in contact windows to a monocrystalline Si (c-Si) substrate. The deposition mechanism is a solid-phase epitaxy (SPE) process: the contact window to the c-Si substrate is covered by a layer-stack of thin aluminum (Al) and amorphous Si (*α*-Si) and a furnace anneal initiates the transport/epitaxy of the latter at temperatures far below the 577 ◦C eutectic point of the Al/Si alloy. The SPE of Si from Al/Si has been first reported in the early years [1]–[3]. More recently, we presented a new solid-phase epitaxy (SPE) process based on material inversion of Al and Si that offers a new solution to ultra shallow p$^+$-type junction formation [4,5]. The use of Al as transport material in our process makes this method fully CMOS compatible. Contact windows to the Si substrate are filled with an Al-doped p+ c-Si island. The very low processing temperature, not higher than 400°C, assures an abrupt, TED-free junction formation and is also very interesting in different applications such as integration of SPE-Si modules into the silicon-on-glass (SOG) processes. Indeed, a strong limitation of the SOG back-wafer processing is the thermal budget limitation to 300°C in order to maintain the integrity of the acrylic adhesive that is employed to glue the alternate substrate, after transferring the devices fabricated on silicon-on-insulator (SOI) substrates.

II. EXPERIMENTS

The sequence of the SPE growth of Si islands in contact windows through the silicon dioxide (SiO$_2$) to the Si substrate is illustrated in Fig. 1.

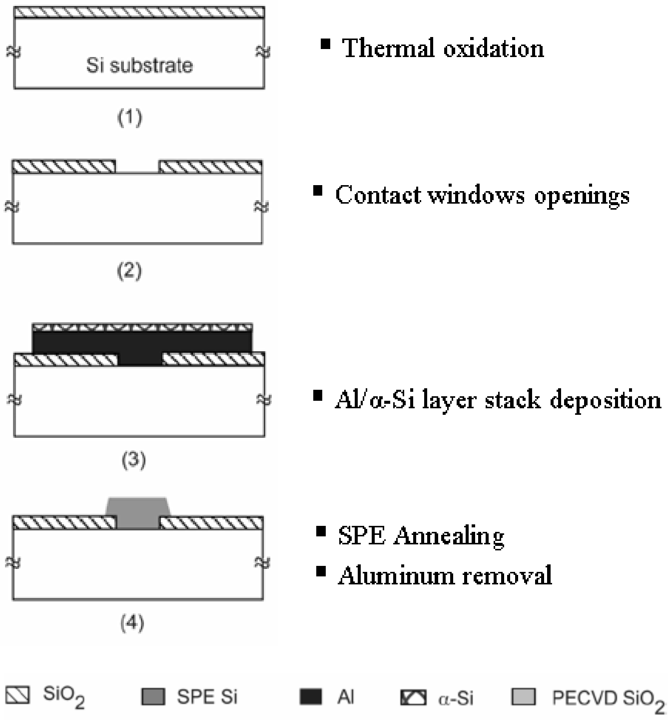

Fig. 1. Schematic of the fabrication sequence of SPE Si contacts.

Monocrystalline <100> Si substrates were used for the initiation of the SPE growth. The position of the SPE growth was determined by etching contact windows to the Si in a 30-nm-thick thermally grown SiO$_2$. Just before metallization, the native SiO$_2$ is removed by 4 min HF 0.55% dip-etch. The room-temperature physical vapour deposited (PVD) layer stack of Al (containing 1% Si) and α-Si is deposited without

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breaking vacuum. The SPE is successfully induced by thermal annealing in a nitrogen vacuum for temperatures of 300ºC and 400ºC and occurs for a variety of different ratios of Al to α-Si thickness.

The results reported below are limited to a combination of 30nm thermal SiO$_2$ isolation, 100nm Al and 75nm α-Si. The crystal-growth process can be controlled by patterning the Al/ α-Si stack in islands around the contact window. The c-Si precipitates are then preferentially initiated in the corners of the contact windows, presumably due to a stress driven process. For window sizes below 2*2 µm^2, the window filling is apparently faster because the first precipitate to form fills the window. The subsequent crystal growth is fed from the α-Si layer via a fast diffusion process in the Al layer [6]. SEM result of Al-mediated Si SPE is shown in Fig. 2 in the case of 400ºC growth for 20 minutes. As can be seen in Fig. 2, no nucleation on SiO$_2$ is observed. Upward crystal growth stops abruptly when the crystal protrudes above the 100nm thick-Al layer. Lateral growth proceeds until the contact window is filled.

The SPE Si/Si substrate interface has been analyzed by high-resolution transmission electron microscopy (HR-TEM). Fig. 3 clearly demonstrates the epitaxial growth and the absence of native SiO$_2$ at the growth interface.

The SPE Si is highly p-doped due to the incorporation of Al in substitutional lattice positions. For SPE processes, dopant incorporation is achieved during growth and doping levels higher than the solid-solubility reported in literature (1–3 x 10^{18} cm^{-3} for Al in Si [10]) can be achieved.

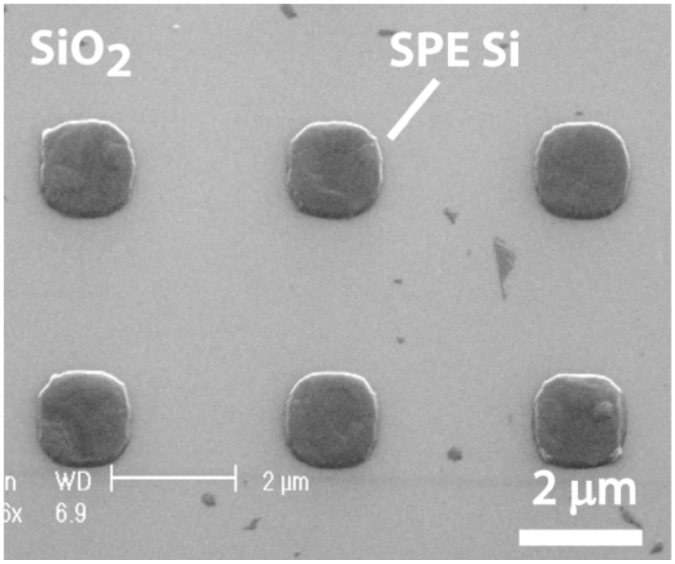

Fig. 2. Location controlled growth of SPE Si. In this case, a geometry has been chosen so that all the available α-Si is collected in the contact windows and practically no nucleation on the silicon oxide is observed.

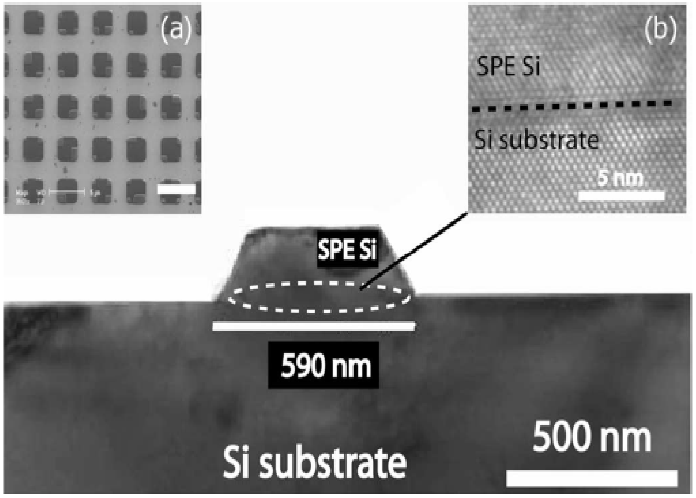

Fig. 3. Cross-sectional TEM image of SPE p$^+$ Si island showing the Si crystal facets. The inset (a) is an SEM micrograph (after wet Al removal) of the initial stages of SPE. In these larger windows, the initiation of crystallization in the corners is evident. The scale bar is 5 µm. The inset (b) is a high-resolution TEM (HRTEM) of the interface with the Si substrate demonstrating the epitaxial growth.

This reported process is also interesting at 300ºC. At this temperature, new challenges need to be investigated. In particular, due to the longer diffusion times necessary for filling contact windows, imperfections at the surface of the SiO$_2$ surrounding the contact window will have more chance to compete as nucleation centers.

In principle, by annealing the Al/α-Si layer stack first, free Si is formed at Al/α-Si interface. These free Si species will then diffuse along Al grain boundaries until they reach the Si substrate or SiO$_2$ interface. At those interfaces nucleation of Si happens. By the annealing, these nuclei's start rearranging and crystal growth occurs. With sufficient thermal energy and annealing time Si species preferentially move to Si substrate and crystal growth happens at the edges of Si substrate and SiO$_2$. Fig. 4.a represents the results of solid phase epitaxy at 300ºC with annealing time of 4 hours. As can be observed, this period is not sufficient for the crystal formation and contact filling and also nucleation on SiO$_2$ is inevitable. In this case, the annealing time is only enough for the nucleation of Si on substrate. By increasing the annealing time, these nuclei will move toward each other and start to form a crystal especially on Si substrate. In Fig. 4.b SEM results of the same sample after 16 hours annealing are shown. This period is now sufficient for the crystallization of the α-Si on Si substrates. The rectangular shape of the Si species on the Si shows this fact clearly. Also it can be seen in Fig. 4.c that a contact opening is filled completely with the condition of annealing at 300ºC for 16 hours, even though still nucleation on SiO$_2$ is unavoidable because of insufficient thermal energy at 300ºC.

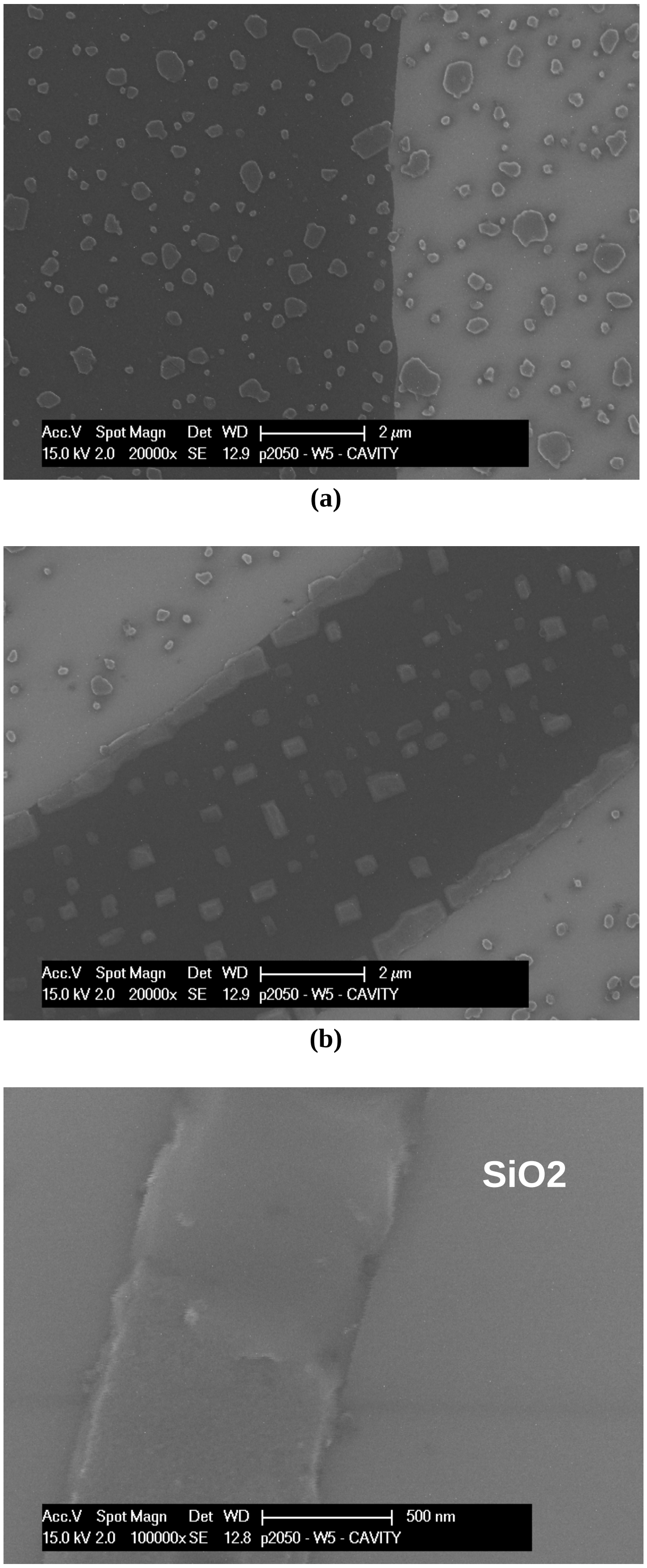
(a)
(b)
(c)

Fig.4. (a) Si nucleation after 4 hours annealing at 300ºC. (b) increasing the annealing time leads to formation of Si crystals on Si substrate. The crystals preferably grow at the Si and SiO_2 edges. (c) contact opening is completely filled at the condition of annealing at 300ºC for 16 hours.

To avoid nucleation on Silicon dioxide at 300ºC, the Al/α-Si layer stack is patterned in order to provide the optimal supply of Si for filling the whole contact window with SPE-Si. As shown in Fig.5, the amount of nucleation on the SiO_2 can thus be reduced noticeably.

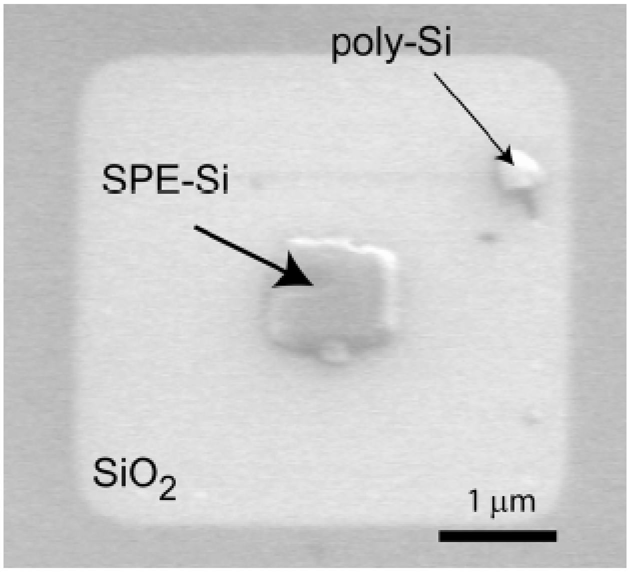

Fig.5 . SPE-Si island grown at 300 °C showing a limited parasitic poly-Si formation outside the contact window.

III. CONCLUSION

In this study we reported an aluminum-induced solid phase epitaxy of silicon mechanism. Controllable growth conditions have been found whereby the contact window was entirely filled in with an exceptionally low defect- density with bulk Si.

The ability to proceed this method at 300ºC has also been investigated. SPE at this temperature is especially interesting for silicon-on-glass (SOG) bipolar junction transistor process which are in line at DIMES laboratories.

The electrical characterization of laterally-contacted SPE-Si at 300ºC and comparison to the already-reported values for 400/500 °C SPE-Si growth processes are underway.

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