Low voltage, low power, self-clocked memory read/program-verify circuitry with adjustable operating frequency

Paola Vega-Castillo, Wolfgang H. Krautschneider

Abstract—**A memory reading and program-verify circuitry for low voltage, low power applications is presented, which performs the read, program and verify operations for a single-poly non-volatile memory. The reading circuitry performs single-ended sensing, thus no dummy cells are required.**

The circuit was fabricated using 0.35µm technology with a nominal supply voltage of 3.3V. Power consumption during reading was measured to be 4.7µW with a supply voltage of 0.75V at an operating frequency of 714 Hz.

***Index Terms*— low voltage, low power, program-verify, reading circuitry, self-clocked**

I. INTRODUCTION

FOR some applications requiring non-volatile memory, low voltage and very low power consumption are of primary importance, whereas speed is not a concern. In addition to this, for some applications self-timed circuits are required [1]. In smart labels, for example, the increasing operating frequency causes that clock extraction from the RF signal becomes very power-hungry, thus self-timed circuits are required, to avoid wasting power for deriving a clock from the RF signal, specially when low operation frequencies are required. In addition to this, non-volatile memories with lower programming and erasing voltages are required for battery-powered and mobile applications. Lowering the programming voltages also reduces the chip area required for charge pumps, which usually require much silicon area due to the size of the pumping capacitors.

In this paper, a read and program/verify circuit for low voltage and low power operation of a single-poly non-volatile memory is presented. The circuit is intended to be used for analog calibration of a smart label. It was fabricated using 350nm technology, which is usually operated at a nominal voltage of 3.3V. The circuit is self-clocked, and is level-activated, that means, the circuit becomes and remains active for a „1“ level of the activation signal. It addresses the cells in a sequential manner. The circuit can operate at supply voltages as low as 0.75V and since is self-clocked, it doesn't require any input clock. In order to control the operation frequency, capacitorless delay-stages are used which can be controlled by means of a DC control voltage.

II. CIRCUIT OPERATION

A. Circuit Operation

The block diagram of the complete system is shown in figure 1. The mode selector allows to select between the reading read (mode control signal kept at low) and the program-verify operation (mode control signal kept at high). The timing unit is responsible for the generation of all clock and control signals for the read and the program/verify operations. In order to activate the circuit, only a pulse to the reset input is required. If the reset input is kept at zero, the circuit is deactivated. If the pulse is applied, the circuit will automatically start its operation and will stop once all cells have been addressed.

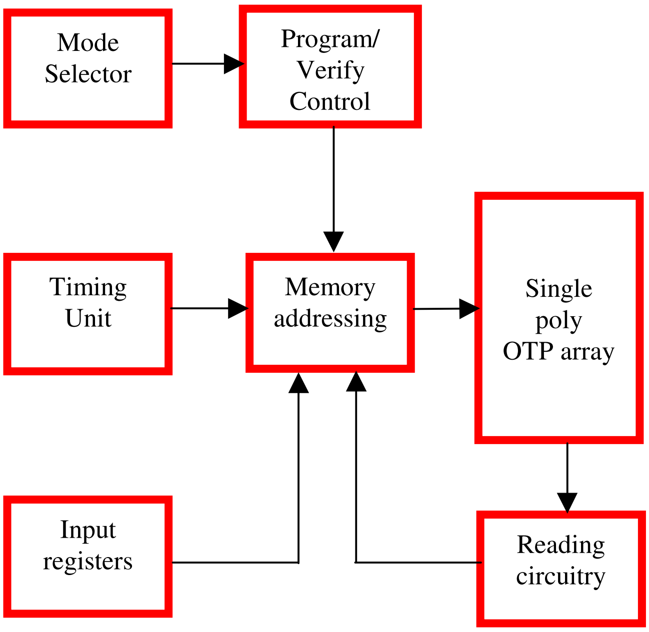

Figure 1. Block diagram

Paola Vega-Castillo is with the Department of Microelectronics, Hamburg University of Technology, Eissendorfer Strasse 38, Hamburg 21073 Germany (phone:+49-40-42878-3945; fax: +49-40-42878-2877; e-mail: paola.vega@tu-harburg.de).

Wolfgang H. Krautschneider is with the Department of Microelectronics, Hamburg University of Technology, Eissendorfer Strasse 38, Hamburg 21073 Germany (e-mail: krautschneider@tu-harburg.de).

The timing unit feeds a memory addressing unit which performs automatic, sequential addressing of the memory cells in the memory array. For the read mode, cells are simply addressed and the sense amplifier senses the cell contents at a frequency determined by a control voltage of the timing unit. Once all cells have been read, the circuit automatically stops its operation and the stored data is available at the output registers included in the reading circuitry block.

During the program/verify operation, cell addressing depends on the output of the sense amplifier and on the contents of the input registers. If a cell is to be programmed, the input data for this cell has to be ,0‘. If the cell should remain unprogrammed, the input data for this cell has to be ,1‘. In this way, programmed cells represent a zero and unprogrammed cells represent a one.

If a cell must be programmed, the programming bias will be applied to it during a fixed period of time determined by the control voltage that controls the operating frequency of the circuit. After the program bias has been applied, the cell is read. If after the programming bias the cell’s threshold voltage corresponds to that of a programmed cell, the cell will deliver enough current to set the output of the sense amplifier to the ,0‘ state. This is the verify operation. If the output of the sense amplifier is ,0‘, the next cell is addressed. If the cell to be programmed has not reached the required threshold voltage shift, this cell will be addressed again during the next cycle and thus, the programming bias will be applied to it. This operation will continue until the cell’s threshold voltage has shifted enough to obtain a current level that sets the sense amplifier to zero.

If a cell must not be programmed, the program operation will be skipped and the next cell will be addressed, without considering the output of the sense amplifier.

Although the circuit is self-timed, the only part of it that requires an external clock is the input stage, which is required only before the programming operation. It consists of a shift register where the data to be stored in the memory is input to the circuit. Once these data are loaded, the circuit will automatically start operation as explained above and the external clock is not required any more.

B. Timing Unit

The key block of this system is the timing unit. This unit must generate the control signals and controls the operating frequency of the circuit with help of a delay stage.

Figure 2 presents the circuit schematic of the delay stage. It allows the implementation of a low voltage, low power, small area delay element, since it relies solely on MOSFETs and does not include any passive element such as capacitors or resistors.

When the input signal is low, M1 and M3 are active, and thus M5 is off and M6 is on. Since the inverter conformed by M3 and M4 is powered by Vcontrol, the time that transistor M6 will require to discharge the output node can be controlled with help of Vcontrol. When the input signal is high, M2 and M4 are active, hence M5 is on and M6 is off. M5 will charge the output node up to the level of the control voltage. The time required to charge the node is controlled by Vcontrol. The complementary transistors M5 and M6 may operate down to the subthreshold region according to the magnitude of the control voltage. The time required to charge the output nodes allows to control the operation frequency.

The timing unit operates as follows: the negated input reset signal, together with a feedback signal F of the timing unit controls an NMOS transistor that resets a cross-coupled inverted latch with two outputs, O_1 and O_2. Output O_1 is taken as base signal for the activation of the sense amplifier. Output O_2 and F negated are used to control another NMOS transistor connected at the complementary output O_2, that provides a set signal for the latch. Output O2 also controls a first delay element. The output of this first delay element is fed to a second identical delay element, whose output is also negated and used as an additional control signal to synchronize the cell addressing. The output of the second delay element is negated two times in order to restore the ,1‘ and ,0‘ levels of the delay element, since these delay elements partially operate at the control voltage, which is always lower than the supply voltage of the system. The outputs of these two “restore inverters” (F and F negated) are fed back to the input stage of the timing unit, thus reseting the cross-coupled inverter latch, and starting the whole cycle again.

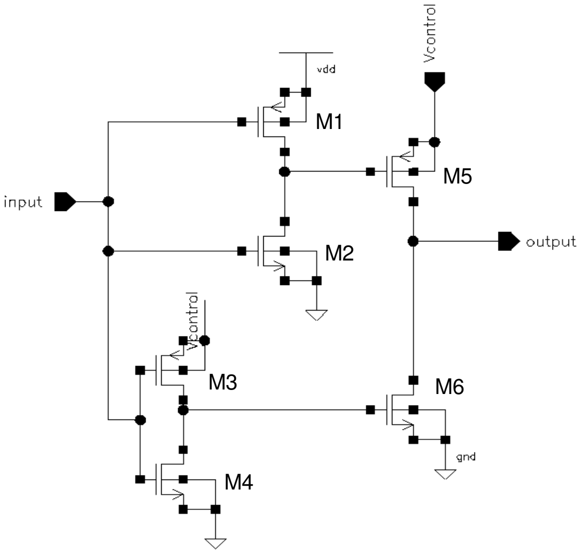

Figure 2. Delay control stage

C. Single Poly Memory Cells

A memory cell configuration was implemented, that is fully compatible with standard CMOS fabrication processes. That is, the memory can be fabricated without changing or adding any masks or process steps, since the cell is based on standard PMOS transistors. Hence, no new library elements need to be developed and no new structures must be added to the process.

In contrast to conventional non-volatile memory cells, this cell doesn’t require a double, stacked-gate process. The cell is free of latch-up risk, since only one type of transistors is used to implement the cell. This also makes the cell more compact when compared to approaches based on the use of both NMOS and PMOS transistors to implement single poly cells.

A very important additional advantage of the cell is that its programming mechanism permits operation at lower voltages in comparison with other approaches. The cell is programmed by means of drain avalanche hot electron injection and can be programmed at Vselectline=4.5V, Vwordline=1V, Vnwell=4.5V and Vbitline=0. The programming time is 15ms. The cell's schematics is presented in figure 3.

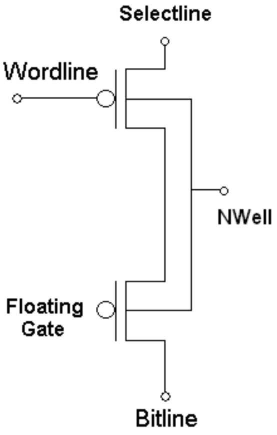

Figure 3. Single poly memory cell

The cell characteristics before and after programming are shown in figure 4 for operation at 3V and 1V. The measurement conditions were Vselectline=0..3V, Vnwell=3V, Vwordline=0V, Vbitline=0V for graphic 4a) and Vselectline=0..1V, Vnwell=1V, Vwordline=0V, Vbitline=0V for figure 4b). Figure 4b) shows that there is a clear difference in the cell current for a programmed and an unprogrammed cell for operation at 1V.

III. MEASUREMENT RESULTS

Figure 5 shows the output of the sense amplifier during the reading operation. The black signal corresponds to the reset signal. The circuit is active when the reset signal is high. The red signal corresponds to the output of the sense amplifier. When the output is low, one cell has been read whose content is zero. After that, the sense amplifier is reset and thus its output is high during the time between the reading operations. For the cases presented in figure 1 all read cells have stored a zero, in order to show the operation frequency of the system. Figure 5a) corresponds to operation at a supply voltage of 0.75V, and figure 5b) corresponds to the case of operation at a supply voltage of 0.9V.

Figure 6 presents circuit operation at a constant supply voltage of 0.85V but different control voltages to change the operation frequency.

The power consumption during the reading operation at different supply voltages is summarized in table 1. The minimum supply voltage for operation of the circuit is 0.75V. At this supply voltage, the circuit consumes 4.7µW operating at a frequency of 714 Hz.

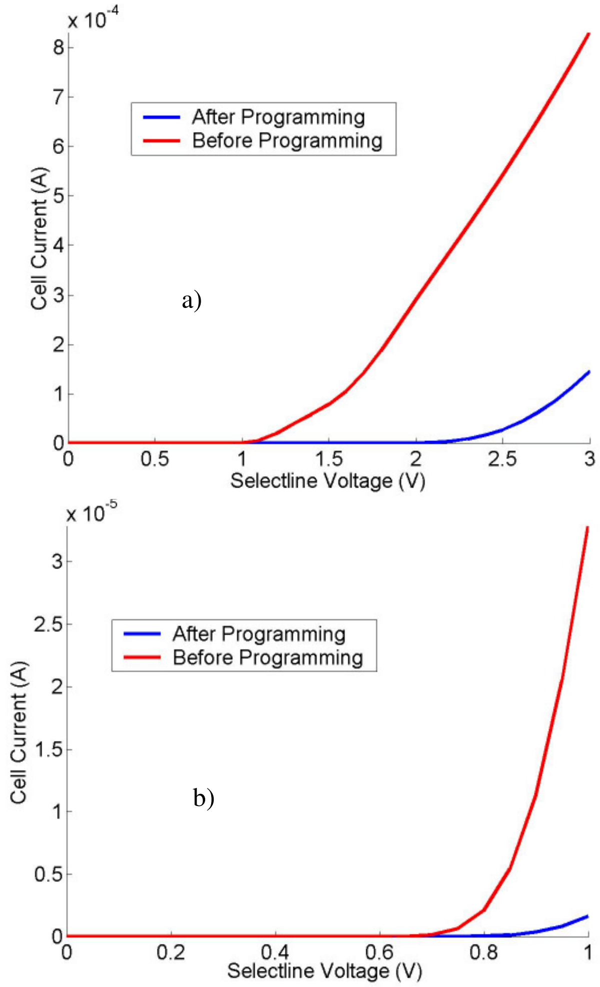

Figure 4. Cell characteristics before
and after programming for operation at a) 3V, b) 1V.

TABLE I
CONSUMED POWER DURING READING OPERATION FOR DIFFERENT SUPPLY VOLTAGES

Vdd (V)	Power Consumption (µW)
0.75	4.7
0.8	7.3
0.85	10.33
0.9	13.67

IV. CONCLUSIONS

Possible applications of the proposed circuit include configurable commercial subproducts, identification memories for wafer traceability, smart cards and labels, and specially analog calibration, due to the sequential access of the memory contents. The circuit consumes low power and can be operated at low voltage, is easy to use, and can be easily and cost-effective integrated into embedded circuits, due to the full CMOS compatibility of the memory cells.

REFERENCES

[1] J.S. Moon et al. "Low Power Sequential Access Memory Design", *IEEE Custom Integrated Circuits Conference*", 2002.

[2] P.Vega-Castillo, W.H. Krautschneider. "Single Poly PMOS-based CMOS-Compatible low voltage OTP",in *Proceedings of the 2005 Microtechnologies for the New Millenium Workshop,* Sevilla, Spain, May 9-11, 2005, pp. 953-960.

[3] Kim, G. et al. "A Low-Voltage, Low-Power CMOS Delay Element", *IEEE Journal of Solid-State Circuits*, Vol. 31, July 1996, pp. 966-971.

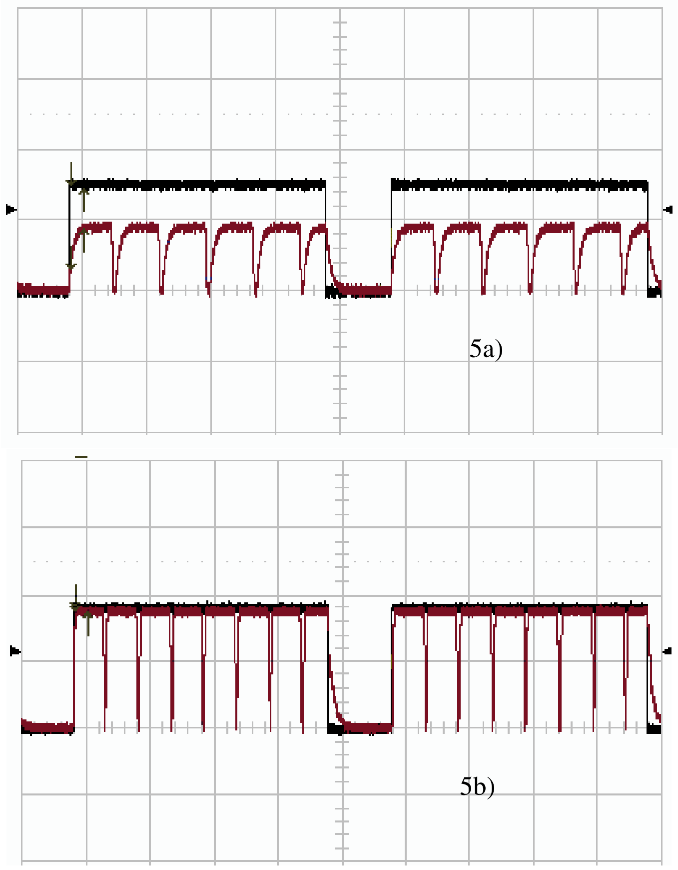

Figure 5. Oscillogram of circuit operation at a) Vdd=0.75V and b) Vdd=0.9V. The red curve corresponds to the output of the sense amplifier, and the black curve to the activation signal. Scales: 0.5V/div, 2ms/div

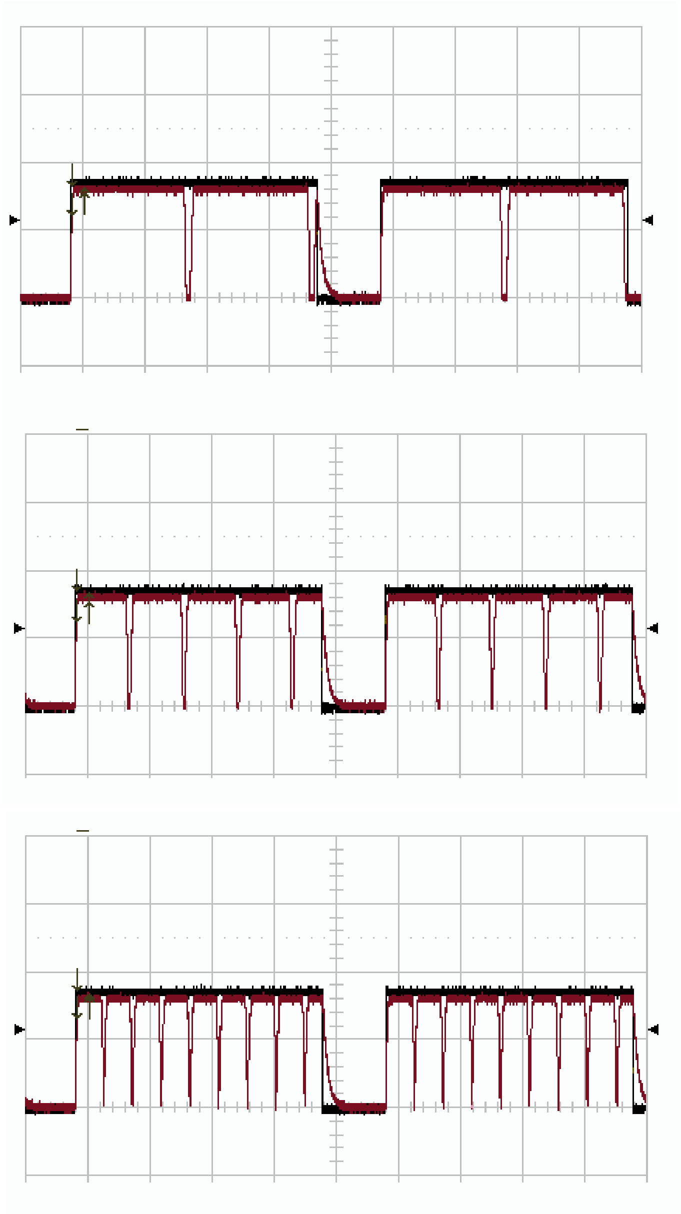

Figure 6. Oscillogram of circuit operation at 0.85V and different control voltages to change the operation frequency. The red curve corresponds to the output of the sense amplifier, and the black curve to the activation signal. Scales: 0.5V/div, 2ms/div