

A 60-GHz Differential Power Amplifier in a 90nm CMOS Technology

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Abstract— This paper describes a 60-GHz differential power amplifier (PA) designed in a 120-GHz f_T 90nm CMOS technology. It consists of three identical differential cascode stages with inter-stage matching implemented by wide-gap coplanar waveguide (CPW) structures and M6-M5 plate capacitors. A double-stub network realized by CPWs provides more design freedom for the input matching. Load-pull simulation generates an optimal differential load of $26.6 + j69.3\Omega$, and the output matching network transforms a differential 100Ω to this optimum impedance. High-Q M6/M5 capacitors in parallel with 5pF MOS capacitors decouple the supply and gate bias of cascode transistors for robust design. The simulated peak small-signal gain is 32.8dB and drops to 22dB at the maximum output power of 12dBm. At 62GHz, the peak PAE is 10.8%, and the -1dB compression point and IIP3 is around -22.8dBm and -15.8dBm, respectively. The die size is $1.18 \times 1.78\text{mm}^2$, and the amplifier consumes 100mA from a 1.5 V supply. Compared to several mm-wave PAs from recent literature, this PA provides superior linear and saturated power gain though operating at the lowest supply voltage.

Keywords— millimeter wave, differential power amplifier, CMOS power amplifier, coplanar waveguide, load pull

I. INTRODUCTION

There are a multitude of multimedia applications requiring broadband wireless transmission over short distances, such as high-speed point-to-point data links and next-generation wireless personal area networking (WPAN). The desired data rate for these applications may be hundreds of Mb/s or even multi-Gb/s. The unlicensed 60-GHz bands (e.g., 59–62 GHz in Europe, USA and Japan) are of special interest for short-range communications within a range of 10m, because the high propagation attenuation in both the oxygen and walls (e.g., 10-15 dB/km in oxygen [1]) helps to isolate communication cells in a local-area networking environment, enabling multiple channel frequency reuse thanks to the low co-channel interference. In addition, millimeter-wave (mm-wave) fre-

quencies lead to smaller-size antennas with highly directional beams, consequently enhancing antenna gain and making on-chip antenna and beam-steering possible [2, 3].

Two standardization organizations, i.e., IEEE 802.15.3.c task group [4] and WirelessHD group [5], have been driving 60-GHz radios. According to some preliminary debates, with an antenna gain of up to 30dBi, a 10-dBm transmit power into antenna satisfies the global requirement of the electromagnetic field emission [6, 7]. In [3, 8–11], several III-V and SiGe solutions were proposed. However, driven by cost reduction and full integration, 60-GHz CMOS radios have become active research in recent years [12–18].

This paper describes a CMOS differential power amplifier (PA) operating from a 1.5V-supply, realized in a baseline 90nm CMOS technology (i.e., CMOS090_LP), based on [17]. The simulated peak small-signal gain is 32.8dB and drops to 22dB at the saturated output power of 12dBm. The outline of the paper is as follows: Section II presents the mm-wave passive components with measurement results on the proposed transmission lines and M6-M5 plate capacitors; Section III addresses the differential PA design issues, covering multi-stage robust design; Section IV shows both small- and large-signal simulation results; Finally, Section V concludes the paper with a performance summary of several recently reported mm-wave PAs (including this work).

II. MM-WAVE PASSIVE COMPONENTS

A. Transmission Lines

Fig. 1 illustrates the cross section of the proposed wide-gap coplanar waveguide (CPW), as implemented in [15, 17]. At 60GHz, the measured insertion loss was 1.1dB/mm, and the quality factor (Q) was in the range of 10-12. As expected, the measured inductance was proportional to the transmission line (TL) length

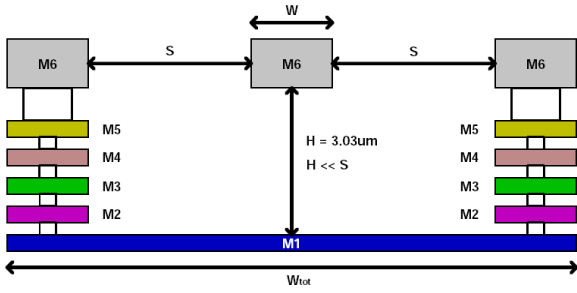


Fig. 1. Wide-gap CPW cross section

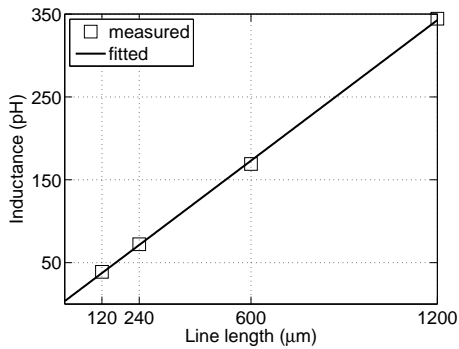


Fig. 2. Measured inductance of the transmission lines

(see Fig. 2). Thanks to this property, inductor design using short-circuit TLs can be simplified.

B. Metal Plate Capacitors

High-Q capacitors, for decoupling, matching and resonators, are realized using inter-plate capacitance between metal 6 (M6) and metal 5 (M5). For a robust design, the parasitic M6-M1 and M5-M1 capacitances have to be considered (M1 is the ground plane). Fig. 3(a) illustrates the top view of the proposed M6-M5 capacitor unit cell, and Fig. 3(b) shows an example of four unit cells in parallel. As shown in Fig. 4, for the number of unit cells below four, the measured M6-M5 capacitance (after deembedding) scaled linearly with the number in parallel; while the number was further increased, the fringe capacitance seems to play a more significant role and the scalability with the number was lost. Anyhow, the capacitance density was around $0.1\text{fF}/\mu\text{m}^2$. Also, the parasitic M5-M1 and M6-M1 capacitances were approximately 30% and 10% of the M6-M5 capacitance, respectively. Therefore, the overall equivalent capacitance differs while flipping M6 and M5 terminals, which actually pro-

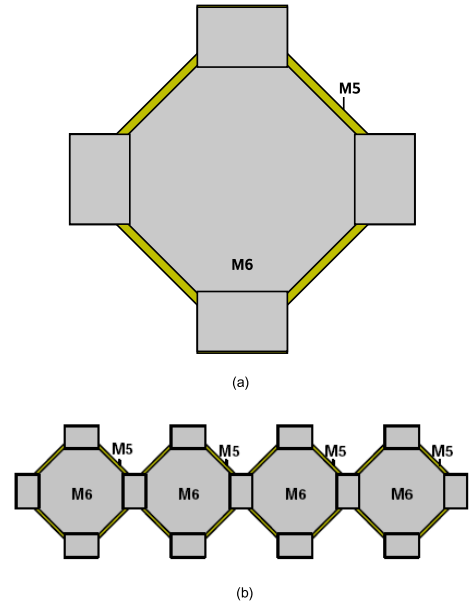


Fig. 3. M6-M5 capacitor top view: (a) $10\mu\text{m}\times 10\mu\text{m}$ unit cell (b) $4\times$ unit cells

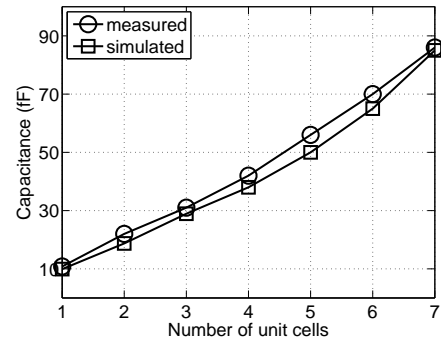


Fig. 4. Measured and simulated M6-M5 capacitances

vides another design freedom for matching network optimization.

III. MM-WAVE DIFFERENTIAL POWER AMPLIFIER DESIGN

In [17], a singled-ended class-A PA with three identical cascode stages was fabricated, and the measured output power reached 8dBm at 60-GHz bands. In principle, by placing two identical single-ended PAs into the differential configuration, 3dB more output power can be achieved ideally. Fig. 5 shows the schematic of the proposed 3-stage differential PA with resonant loads. The parasitics associated with the M6-M5 capacitors were included in the circuit simulation. To obtain a good common-mode rejection, symmetrical layout of the two differential branches is a must. In addition, three 60-pH spiral induc-

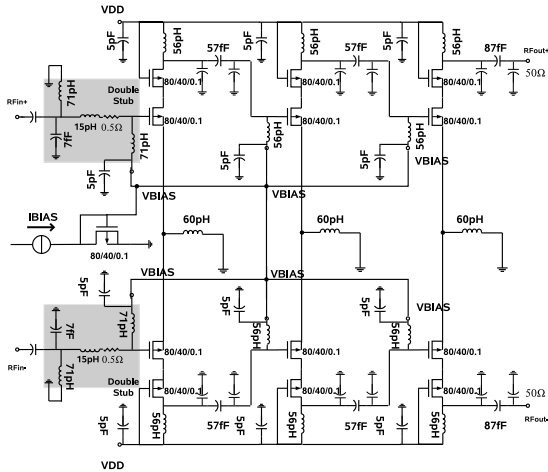


Fig. 5. Schematic of the proposed differential PA

tors were placed at virtual ground nodes to reduce common-mode power gain without minimal effects on the differential output. Here the model inaccuracy and inherited parasitics associated with these source-degenerated inductors are not a problem.

As in [17], for the input matching, a double-stub network implemented by CPWs proposed in Section II was adopted to provide more design freedom over a single-stub design. As a consequence, the transmission line length was minimized and thus the chip area was reduced. Load-pull simulation generated a differential load of $26.6 + j69.3\Omega$ for optimum power match, and the output matching network transformed a differential 100Ω to this optimum impedance. To ensure a robust design and avoid oscillations, high-Q M6-M5 capacitors (i.e., in the order of 100fF) were put in parallel with 5-pF MOS capacitors to decouple the supply and gate bias of cascode transistors.

IV. SIMULATION RESULTS

Fig. 6 shows the simulated small-signal gain (i.e., S21) of the differential PA was in the range of 25–32dB at the unlicensed bands of 59–62GHz. With resonant loads, the gain flatness was sacrificed as expected. Large-signal simulation results are shown in Fig.7. At 60, 61 and 62GHz, the linear gain was approximately 26, 29 and 31dB, respectively, which was in good agreement with the S-parameter simulation results. At 62GHz, the peak power-added efficiency (PAE) of 10.8% is obtained at -3.7-dBm input RF power, and for the input power range of -18 to -10dBm, 10–12-dBm output power and 6.6–10.2% PAE can be achieved. Also at 62GHz, the -1dB compression point and the third-order input intercept point (IIP3) were around -22.8dBm and -15.8dBm, respec-

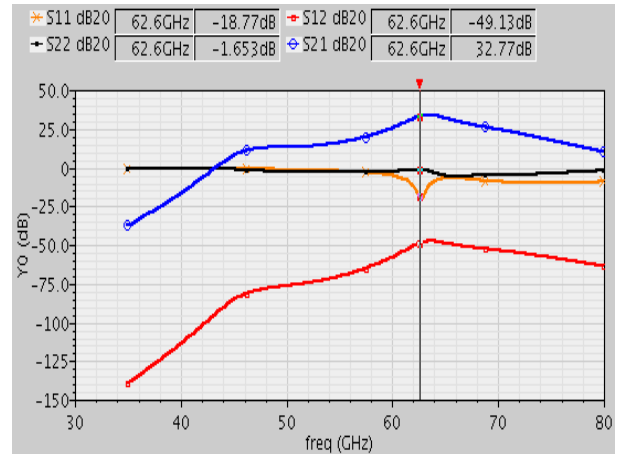


Fig. 6. Simulated small-signal S-parameters for the differential PA

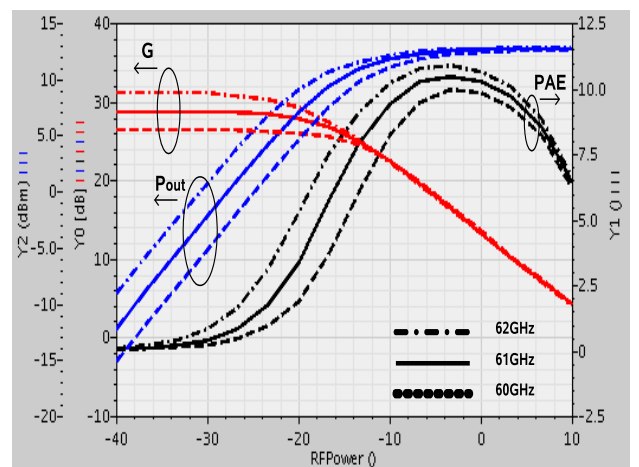


Fig. 7. Simulated power gain, output power and PAE for the differential PA

tively. Fig. 8 shows the simulated temperature dependencies of the power gain, output power and PAE for the differential PA. When the temperature varied from 20°C to 150°C, the output power dropped by 3–5dB, and the PAEs decreased by 4–6%. At 60°C (for an input power of -15dBm), an output power of 10.2dBm and a PAE of 7% can be still achieved. Fig. 9 shows the die photomicrograph of the differential PA. Including all pads, the die occupies $1.18 \times 1.78\text{mm}^2$.

V. CONCLUSION

A 60-GHz 3-stage differential PA was implemented in a 120-GHz f_T 90nm CMOS technology, consisting of three identical differential cascode stages with inter-stage matching implemented by wide-gap CPWs and M6-M5 plate capacitors. The amplifier delivered a saturated output power of 12dBm, with a peak PAE

TABLE I
MM-WAVE PA COMPARISON FROM RECENT LITERATURE

Parameters	This	[16]	[9]	[3]	[10]
Freq.(GHz)	62	60	60	60	60
P_{sat} (dBm)	12	9.3	20	12.8	–
GT_{sat} (dB)	22	–	4.5	–	–
CP_{-1dB} (dBm)	7	6.4	13.1	11.2	+17
GT_{max} (dB)	32	5.2	18	12	13.4
PAE_{peak} (%)	10.8	7.4	12.7	7.9	5.5
VDD(V)	1.5	1.5	4	1.8	3
Technology	90nm	90nm	0.13 μ m	0.18 μ m	0.15 μ m
-	CMOS	CMOS	SiGe-BiCMOS	SiGe-BiCMOS	pHEMT

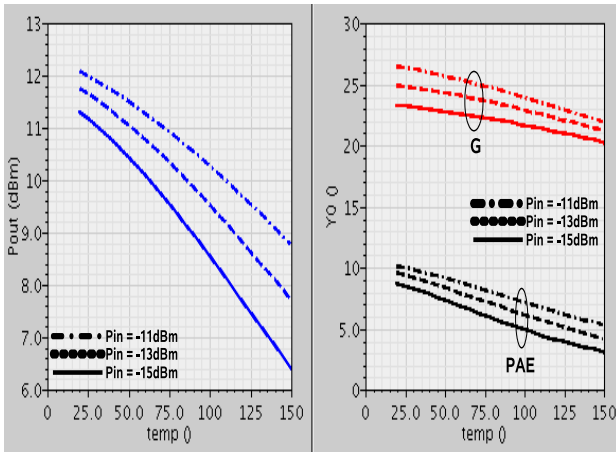


Fig. 8. Simulated temperature dependencies of the power gain, output power and PAE for the differential PA

of 10.8%, and a maximum power gain of +32dB. The total power consumption was 100mA from a 1.5-V supply. Compared to several mm-wave PAs in recent literature, as shown in Table I, this PA provides superior linear and saturated power gain (i.e., GT_{max} and GT_{sat}) though operating at the lowest supply voltage.

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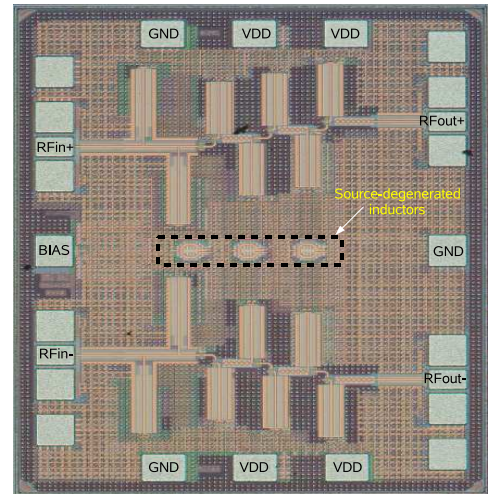


Fig. 9. Die photomicrograph of the differential PA

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