

Towards Digitally Enhanced ADC's

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Abstract—Analog-to-Digital converters operating at gigasamples per second are often required in nowadays communication systems. One effective way to achieve high sampling rates at low power consumption is time-interleaving. However, time-interleaved converters suffer from well known problems like offset, gain and sample time mismatch which degrade the performance of the ADC system as a whole. The designer can make use of available digital functionality to cope with these problems. This article discusses ways to improve the performance of time-interleaved analog-to-digital converters by making use of the possibilities (and tradeoffs) of added digital resources.

Index Terms—A/D conversion, calibration, time-interleaved, track/hold circuit, channel mismatch.

I. INTRODUCTION

IN recent years, due to the continuous development of Applications in communications, measurement, etc., there is an increasing demand for high speed analog-to-digital converters. A practical and effective way to achieve high operating speeds is to apply time-interleaving [12]-[14]. Also with the years fabrication technology offers advantages like more functionality per silicon area, faster transistors and additional digital resources. These extra functionalities can be used to improve system performance in the challenging field of analog circuit design.

In fact this is not a new idea: [3], [5] and other references in literature propose the use of these available resources to create on-chip intelligence which can be used to improve the performance of analog circuits. In the particular case of analog-to-digital converters performance is described in terms of power, speed and resolution. For example in [3] this approach is employed to digitally correct the linearity of a pipelined ADC, built with non accurate components. Ref. [5] proposes a description at block diagram level of how a “Smart AD/DA” should look like and points out some examples. In this work focus points will be on high speed operation and low-power consumption, combined with high resolution, obtained by the use of “smart” calibration.

A promising architecture to achieve power efficiency and

This work has been supported in part by the Dutch Technology Foundation STW.

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higher speed than that dictated by technology limitations for a single converter is to use simple and efficient analog-to-digital converters in a time-interleaved array. This has been shown already in [12]-[13] where pipelined and SAR topologies have been connected in a time-interleaved way achieving sample rates of 600MSPS and 20 GSPS respectively. Ideally each of the interleaved ADC's characteristics should be identical and clock skew should be zero. However, time-interleaved converters suffer from offset mismatch, gain mismatch and sampling time errors among the channels. These errors and their implications have been widely documented in literature [4].

Inspired by the necessity to improve the performance of high speed analog-to-digital converters and to make use of what is available on chip; this paper discusses the possibilities to take advantage from the time-interleaved architecture together with calibration techniques. This combination can additionally track changes in the system and correct them to achieve the desired specifications. Section II reviews the time-interleaved concept and discusses practical choices on track and hold, ADC and interleaving large amount of channels. Section III gives a compilation of techniques used to remove offset mismatches. Section IV describes ways to remove gain errors. Section V presents correction of timing errors. Section VI extends the discussion with the possibilities of combining time-interleaving with calibration.

II. TIME-INTERLEAVED CONVERTERS

A time-interleaved architecture consists of M converters connected in parallel. Each of the converters is called a “channel” [1]. Each channel operates at the same sampling rate f_s divided by M , the overall converter operates at a sampling rate f_s . This is illustrated in Fig. 1.

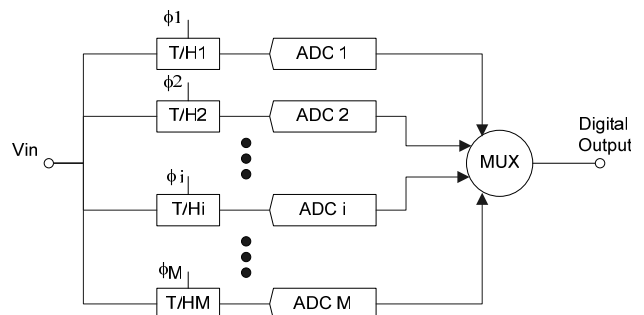


Fig. 1. Time-interleaved ADC architecture.

The analog input is multiplexed by the track and hold array, the final output code is realized by digitally multiplexing each of the codes from the channels.

A. Track and Hold

The design decision of implementing the track-and-hold function with an array will have the following effects: on one hand this relaxes the speed requirements compared to the case when only one track-and-hold would have been used; on the other hand it complicates things because the different track-and-hold units will suffer from offset, gain and timing mismatches.

The track and hold unit also helps to drive each ADC channel input capacitance from the sampling capacitance. This capacitance is determined by the required resolution together with kT/C noise. The drive function is carried out with a buffer included in the track and hold [2]. Currently we focus our efforts in two possible buffers: a differential source follower and a differential pair. If the devices were sized according to offset requirements the sizes would end up being huge, and this would limit the track and hold speed. This tradeoff evidence the need for some calibration algorithm for offset reduction to achieve the higher speed: Some offset will be accepted in the design which will be later corrected as described in Section III. Thus priority is given to increase the speed as much as possible.

Once transistors are sized, the current required to bias the transistors is determined by the settling behavior. If the transistors would exhibit a quadratic current-overdrive voltage relation, one would expect that doubling the current would make the circuit twice as fast. However, this is not the case for deep submicron technologies. Fig. 2 shows this situation where f_s is the sample rate achievable with current I_b based on technological limitations. At a certain point it is more attractive from the power point of view (reflected as a current on the x axis) to interleave in time two converters to get twice the speed (trend is reflected in the linear function) than simply making one converter which consumes two times the current (trend reflected in the curved function).

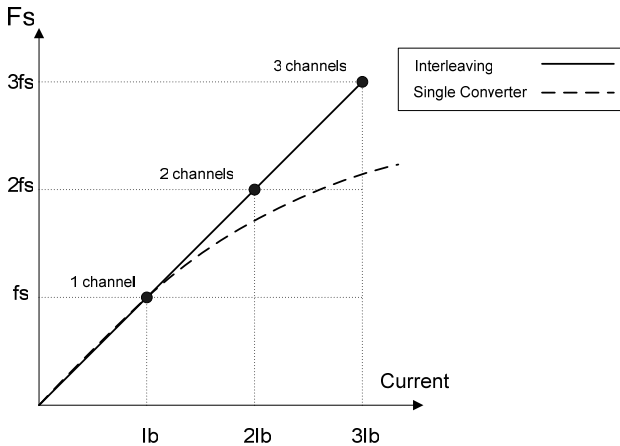


Fig. 2. Interleaving achieving higher sampling rate than single converter for the same current.

B. ADC Channel

Each ADC topology is chosen according to performance requirements. For high speed and medium resolution pipeline has been the preferred topology [6], [12]. However, the successive approximation topology [13] also seems to be a good candidate despite of being considered the best choice regarding power efficiency, especially for low sampling rate applications for many years. The main advantage stems from its simplicity, this topology needs no precision components like a multiply by 2 amplifier and has only one comparator. When comparing the achieved speeds and power efficiency reported in literature with both topologies it appears that pipelined time-interleaving reaches higher sample rates but is less power efficient than successive approximation time-interleaving.

C. Limitations on Large Amount of Channels

The amount of channels to be interleaved is very dependent on the implementation; each implementation will require different currents and will have different capacitances. Also the amount of channels to interleave can not be very high, because there will be practical limitations regarding parasitics and clock distribution networks.

III. OFFSET MISMATCH

A. Causes

As the overall ADC will be made of slower independent channels, each track and hold and ADC will add up a different offset to each channel due to mismatch [6], there are two ways to decrease the offset.

1. Use larger devices in the track and hold path; larger devices will show better matching. Unfortunately this will lead to slow circuits.
2. Accept the offset present, and try to correct for it. This can be in the digital, the analog domain, or a mixture of both.

B. Time Domain Effects

Offset mismatches are reflected in the time domain as an additive signal independent of the input signal, this is commonly referred to in literature as fixed pattern noise.

C. Frequency Domain Effects

This mismatch fixed pattern noise has frequency f_s/M , in the frequency domain it causes noise peaks at

$$f_{noise} = k \times f_s / M, \quad k = 1, 2, 3, \dots$$

The degradation of the S/N due to offset is independent of the signal input frequency and amplitude [4].

D. Calibration Methods

Several ways have been proposed to cope with this problem; one way has been to store the offsets of each channel and then subtract them digitally from the output, other

alternatives are translating the offset spur to low frequencies by chopping and the translated spur by filtering, or adjusting some calibration reference [14] [15].

IV. GAIN MISMATCH

A. Causes

Gain differences between the channels will appear due to mismatches present on each channel. Generally certain amount of gain mismatch is tolerated and corrected by means of calibration or adding redundancy.

B. Time Domain Effects

As the gain is a multiplication factor of the input signal, it is common to call the gain error “multiplicative” in the time domain; this means that for low signal levels the effects of gain error will be smaller compared to signals which are close to full amplitude. That proportionality to the signal amplitude is commonly referred to as amplitude modulation AM; in fact the input signal is being modulated by the channel gain sequence.

C. Frequency Domain Effects

Because of the amplitude modulation effect, amplitude and gain mismatch dependent spurs will appear at the frequencies

$$f_{noise} = \pm f_{in} + \frac{k}{M} f_s, \quad k = 1, 2, 3, \dots$$

It is important to underline that unlike with offset mismatch; gain mismatch SNR degradation is dependent on the signal amplitude [4].

D. Calibration Methods

All the techniques trying to correct for gain mismatch are focused to establish a channel reference. Once this reference is established, the gain of the remaining channels is adjusted. This gain can usually be controlled by a reference voltage or current.

In [7] an analog calibration mode is proposed. There the gain is measured from an ADC taken out of the time-interleaved structure. Then a slow but accurate ADC is taken as calibration reference. The gain value is adjusted to that of the reference using a LMS algorithm; the gain can be adjusted by fixing the reference voltage of the respective channel ADC.

Another approach is presented in [8], here the gain required is estimated by an LMS loop which includes adding an analog pseudorandom noise signal to the input and later subtracting it digitally from the main signal. An advantage is that this calibration is background; a disadvantage is that the dynamic range of the ADC is reduced because voltage room is required to add a signal.

To overcome that problem in [9], gain is estimated by using chopping techniques together with a correlation based algorithm based on the fact that the spurs contain information related to the gain mismatch. To correct gain errors some references are adjusted reducing substantially the spurs due to gain mismatch. This approach is intensive in digital signal

processing which in the end benefits from CMOS scaling.

V. TIMING ERRORS

A. Causes

Timing error has two origins: deterministic and random (jitter). Aperture error or clock skew is the deterministic difference between the ideal and real sampling instant arising from the use of a several clocks in a distributed track and hold circuit, in some implementations the timing error problem has been overcome by placing a single track and hold [8]. A distributed track and hold offers the advantage of avoiding building an accurate circuit operating at the full speed of the time-interleaved ADC, but as each track and hold unit requires a clock, each clock path should have a careful layout to avoid errors in the timing. In some cases a meticulous layout is not enough to guarantee the right timing because clock drivers are prone to mismatch. Furthermore timing errors can arise from disturbances in the power supply as well.

B. Time Domain Effects

Suppose that clocks $\phi_1, \phi_2, \dots, \phi_M$ have skews dt_1, dt_2, \dots, dt_M , suppose also that the input is a sine wave, in this case the error due to clock skew will be larger at the point where the sine wave has maximum slope, i.e. at the zero crossings resembling a phase modulation. The error signal is then 90 degrees shifted with respect to the input signal.

C. Frequency Domain Effects

Because of the phase modulation effect, deterministic timing error spurs will appear at the same frequencies as for the gain mismatch case

$$f_{noise} = \pm f_{in} + \frac{k}{M} f_s, \quad k = 1, 2, 3, \dots$$

In this case the SNR degradation is proportional to the input signal frequency, affecting the dynamic performance of the time-interleaved ADC.

D. Calibration Methods

The required timing error allowed to get distortion power from timing skew less than the quantization noise in a Nyquist converter with maximum input frequency ω_0 is given by [15]:

$$|dt| < \sqrt{\left(\frac{M}{M-1}\right)\left(\frac{2}{3\omega_0^2}\right)\left(\frac{1}{2^{2n}}\right)}$$

This means that for an input signal of 800MHz and 16 interleaved channels, the timing skew should be less than 164fs for 10 bit accuracy. At such low timing error levels is then the question whether building a complex variable delay circuit will not ruin the desired functioning by adding jitter.

In [10] a digital interpolation method correcting for timing errors is shown. This method is based on the fact that it is possible to reconstruct the original signal with the samples

obtained at the actual sampling moments if the timing information is known. The timing error is measured with a ramp signal at the input and the clock skew is extracted as the difference between two codes divided by the ramp slope, random jitter effects on the measurement are cancelled by averaging a large number of measurements. The main disadvantages of this method are: the requirement of an accurate ramp signal and that the calibration method is made background by adding the ramp signal the input signal reducing the input dynamic range.

Ref. [11] proposes blind adaptation, meaning that the only information required to estimate the mismatches and correct for them is that the signal is band limited to the Nyquist frequency of the complete ADC system. The correction is fully digital and offers good perspectives regarding low area and low power consumption with the newer CMOS technologies. However the algorithm is very complex computationally speaking.

In [9] extensive digital signal processing is used to correct for sample time error. Sample time error is detected with the frequency domain spur containing information related to the timing error. This information is read out as a DC value by multiplying the input signal with the same signal passed by a chopper and a Hilbert transformer. This Hilbert transformer shifts the phase 90 degrees, allowing to distinguish between gain error mismatch and time error mismatch. The obtained error is proportional to both the input signal frequency and the timing error; this is convenient for detection because it makes the correction sensitivity higher for higher frequencies and for higher clock skews values. For correction the ideal fractional-delay-time filter is calculated. It turns out that several of the filters required are non causal, and some approximations are made for circuit implementation. This correction method has the advantage that is fully digital, but the disadvantage that the detection method can indicate that a correction is needed when the input signal has frequencies close to $f_s/4$.

VI. DISCUSSION

This paper presents possibilities to implement a time-interleaved ADC high speed low power analog-to-digital converter, profiting from the advantages offered by calibration. It is finally a challenge for the circuit designer to make the choices regarding tradeoffs and calibration to achieve the desired performance. One crucial issue is power consumption; it is a fact that digital calibration is very appealing. To give an example in CMOS90 technology a 2 input NAND requires 2.5fJ per operation, a state of the art 10 bit ADC consumes 0.25nJ per conversion which is equivalent to 100000 NAND gates [3]. However the extra power used to do calibration should be reflected in performance improvement or the ability to track changes like proposed in the "Smart approach". The several references mentioned show that the combination time-interleaved, calibration is a viable approach. It is then very likely to see more in this direction in the following years.

VII. CONCLUSION

In this paper ways to improve performance of time-interleaved analog-to-digital converters have been presented. The trend is to implement in silicon techniques that combine analog circuits helped by digital circuits to realize this improvement. The need for smartness is evidenced by initial calculations of a time-interleaved track and hold showing the need to include calibration for offset. Other aspects to take into account would be timing and gain error correction. Timing error correction will be of particular importance for high speed data converters; remarkably there are not so many published implementations in silicon addressing this problem for a large amount of channels.

ACKNOWLEDGMENT

The author would like to thank Ed van Tuijl for his support and discussions.

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