Design of a process-parameter independent test-structure for reliability tests

Kristian Hafkemeyer, Andreas Domdey, Wolfgang Krautschneider

***Abstract*— A test-structure for statistical measurements of MOSFET failures caused by the time dependent dielectric breakdown with an external microcontroller is presented. The concept is technology independent and can be used to adjust and verify existing breakdown models.**

***Index Terms*— Reliability statistics, test structure, MOSFET, breakdown**

I. Introduction

Tests in CMOS-circuits with gate-voltage and temperature stress are important to get insights into the degradation of modern CMOS-devices with ultra-thin gate-dielectric thinknesses. The gate-dielectric-failure is one of the dominant yield and reliability issues of integrated circuits. A lot of important results regarding the time dependent dielectric breakdown have been gained from measurements by [1], [2], [3] and [4]. For the measurements most often single devices were used. To get a large statistic about the gate-dielectric breakdown in MOSFET devices depending on time a parallelized test structure with external failure-analysis was developed. The test-structure consists of a high density discrete DUT (devices under test) matrix (approx. $2^{16} = 65536$) and different decoders to control the matrix, which are able to localize failures in the matrix of the devices under test, see Figure 1.

Failures are caused for instance by the time-dependent dielectric breakdown, which increases the gate current through a conducting path inside the gate dielectric. The increase of the total current compared to the tunnelling current of the matrix is detected by the voltage drop over an external shunt resistor and a subtracting amplifier which distinguishes between a high and a low current, i.e. a working and a non working device. The evaluation and processing of this signal as well as the control of the complete test structure is done by an external microcontroller. Finally, DUTs with gate oxide breakdowns are shut off by an additional MOSFET which is connected in series to the gate of the DUTs and is controlled by the row and column decoder and the logic part of the DUTs.

The paper is structured in four sections: Section II explains the concept of the test structure; Section III discusses the proposed implementation of the test-circuit; conclusions are given in Section IV.

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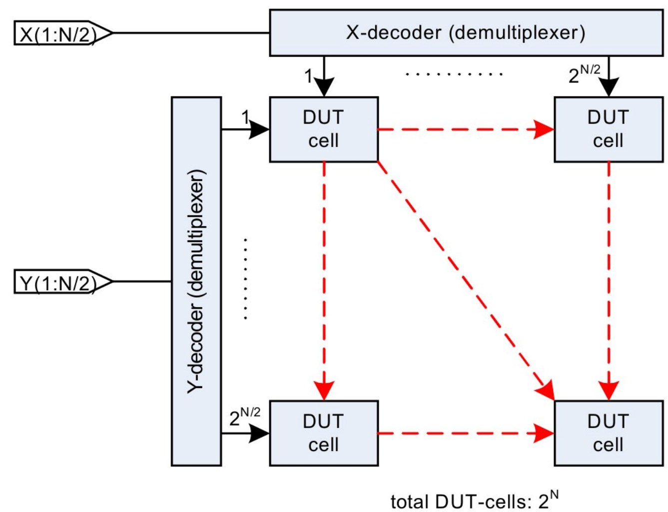

Fig. 1: Outline of the complete test-structure.

II. Concept

The major problem of this discrete integrated matrix is that the control-circuit, the decoders and logic part of the DUT-cell, and the devices under test (DUT) are on the same chip. In this case the DUT, and the digital part are stressed with the same temperature and degrade nearly with the same probability in time. To circumvent this problem, it is possible, to use different gate-dielectric thicknesses for particular MOS-transistors in mixed mode CMOS processes. Therefore the demultiplexer, the decoder and the switch-off transistors are integrated with so called I/O transistors and the DUTs themselves with design kit specific lowest dimensions regarding the gate-dielectric thickness.

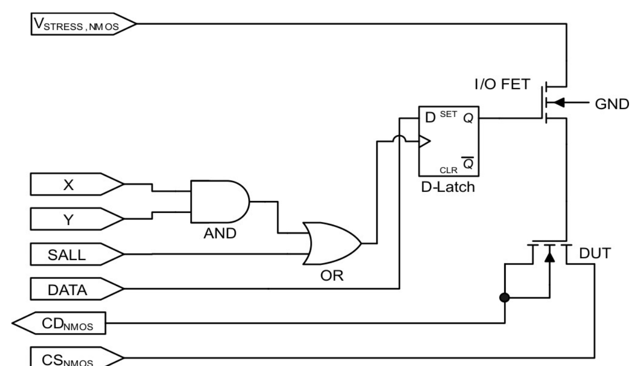

Fig. 2: Circuit of an NMOS-DUT-cell.

This means for a 130 nm process the I/O transistors are dimensioned for a 3.3 V supply voltage and the DUTs are integrated with standard performance 1.2 V voltage range transistors. The gate-dielectric thickness of the I/O transistors is about twice as thick as the standard performance transistor in this particular CMOS process.

The control logic is large compared to the DUTs, because there have to be row- and column-decoders as well as latches for every device under test integrated. The schematic of one single DUT-cell is illustrated in Figure 2.

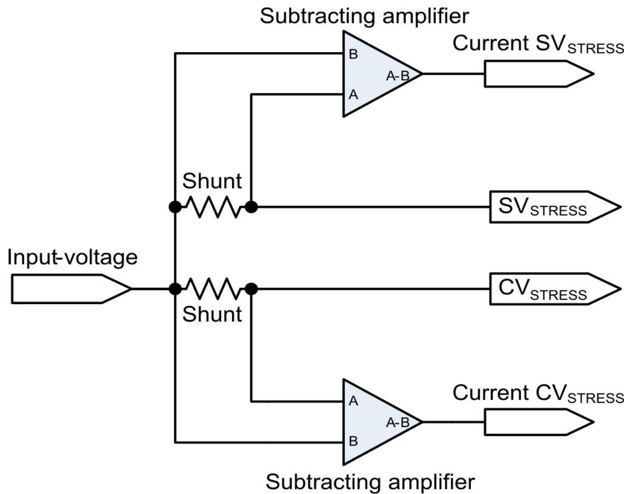

Fig. 3: Current sense circuit for failure analysis.

To keep the system size and the complexity as small as possible, the total current through the MOSFET matrix is measured by the voltage drop over two external separated shunt resistors if an NMOS-DUT-matrix is integrated, see Figure 3. The currents SCV_{STRESS} (single current V_{STRESS}) and CCV_{STRESS} (common current V_{STRESS}) are used to identify the damaged device. The voltage drop over the shunt resistors is measured by means of a subtracting amplifier and is proportional to the current through the resistor. Implementing the subtracting amplifier on chip will cause reliability issues by the applied stress. Therefore, it is setup by discrete components externally from the chip.

If a gate-dielectric breakdown occurs inside the matrix, the common current CCV_{STRESS} through the resistor is going to increase and is detected by the continuously sampling microcontroller. In this case the microcontroller switches the stress voltage to a second current monitoring circuit row by row. If the current SCV_{STRESS} through the second shunt resistor is very small or insignificant then there is no breakdown within the row under investigation and the microcontroller steps to the next row until the current SCV_{STRESS} is high. Once a high current is detected in a single row, every DUT is switched off and on until the corrupt device is located. The control logic of every cell helps to switch DUTs permanently off. The timestamp when the gate-dielectric breakdown occurs is saved to the flash-memory on the microcontroller as well as the addresses of devices which are switched off permanently, in order to reconstruct the matrix in case of problems or reset.

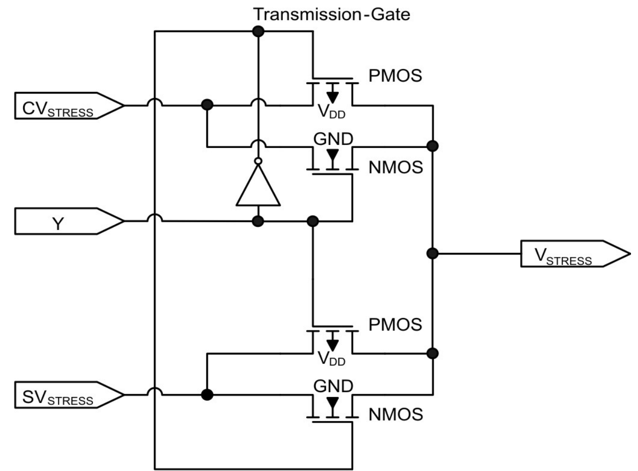

Fig. 4: CMOS Transmission-Gate.

There is the need of two shunt resistors to switch the row under investigation to a different current measuring circuit with a CMOS transmission-gate to keep the MOSFET devices stressed as long as possible, see Figure 4.

III. Circuit Design

Every single row consists of two transmission-gates which work as an analogue-switch and transfer the common or single stress-voltage to its output, see Figure 4. The analogue-switch is integrated with PMOS and NMOS transistors as well as a CMOS inverter.

The stress voltage is transferred to an additional I/O FET which can switch on and off the DUT by toggling the D-latch in the control-logic. The D-latch is controlled by a row- and column-decoder (AND gate) and an option to select all devices (OR gate) in order to reset the whole matrix at the beginning of the test series or at uprising problems. The AND and OR circuit can be simplified to a NOR and NAND gate with inverted inputs to reduce the amount of transistors per cell.

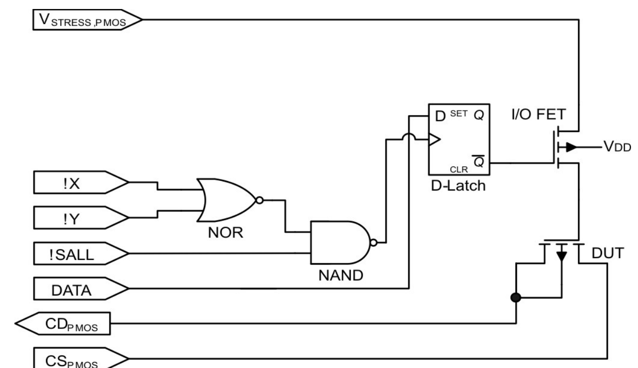

Fig. 5: Circuit of PMOS-DUT-cell with NOR and NAND gates.

The MOSFET device under test can either be an NMOS or a PMOS device. In order to test PMOS devices, everything of the logic part up to the output of the D-latch can be kept as in a NMOS-DUT-cell. The common drain and source is connected to V_{DD} and the stress-voltage is grounded.

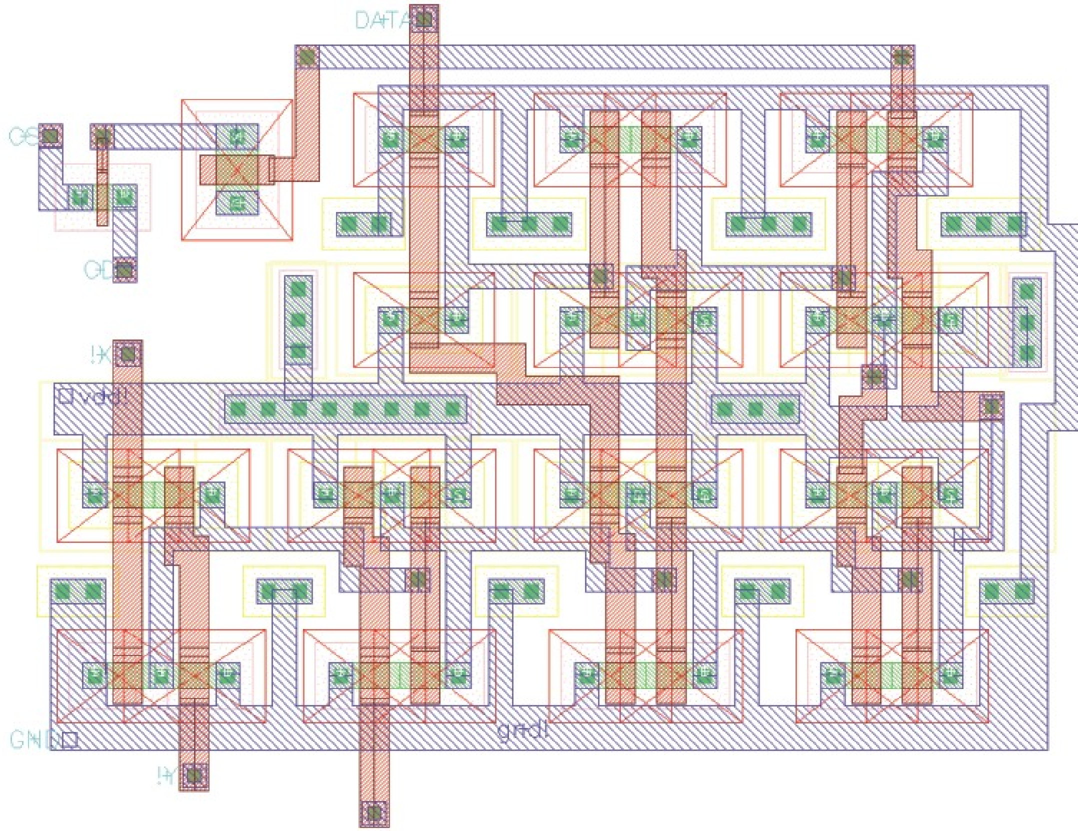

Fig. 6: Layout of a single NMOS-DUT-cell.

The circuitry for a PMOS-DUT is shown in Figure 5. The whole chip is fabricated in a 130 nm process. In this case, the process supports MOSFETs with different thicknesses of the gate-dielectric which is very important for the choice. The AND and OR gate as well as the NOR and NAND are generated with I/O FETs, because the gates have to sustain temperature and other stress gradients. The layout of the complete NMOS DUT cell with the logic and DUT derived from the schematic (Figure 2) is exposed in Figure 6. On the chip are NMOS as well as PMOS-DUT cells with different W/L sizes of the DUT integrated.

The Cadence based design-flow of the customized DUT-cell is basically as follows:

- schematic entry in Virtuoso
- verification of the digital-blocks within the DUT-cell
- Layout with Virtuoso Layout XL
- Generation of the abstract view with the Cadence Abstract Generator. It is used to create a Library Exchange Format (*lef*) file containing the physical properties of the cell.

The *lef*-file is used to perform an automatic placing and routing of the complete DUT-matrix.

The row and column selection is done by an N-bit to 2^N demultiplexer. The X- and Y demultiplexer are integrated with I/O FETs. The decoders are synthesized from a Verilog code with NOR and NAND gates whereas the inverter, NOR and NAND gates had to pass through nearly the same design-flow like the DUT-cell and has been constructed as well.

TABLE I: Input- and output-pins of the test-chip.

Input-pin	Description
X(1:N/2)	Column-selection
Y(1:N/2)	Row-selection
SALL	Select all devices
DATA	Data for the latch
$4xV_{DD}$	Powersupply
4xGND	Ground
$CV_{STRESS,\ NMOS}$	Common Stress-voltage NMOS
$SV_{STRESS,\ NMOS}$	Single Stress-voltage NMOS
CD_{NMOS}	Common drain NMOS
CS_{NMOS}	Common source NMOS
$CV_{STRESS,\ PMOS}$	Common Stress-voltage PMOS
$SV_{STRESS,\ PMOS}$	Single Stress-voltage PMOS
CD_{PMOS}	Common drain PMOS
CS_{PMOS}	Common source PMOS

IV. Conclusion

This test setup consisting of the test structure in state of the art CMOS technology and the microcontroller for the analysis is going to be used for different stress temperatures and stress voltages in parallel. The cell size of one DUT is about approx. 15x10 um^2, the complete matrix with the decoder is about 4x4

mm^2. The stress tests are going to run for up to two years in parallel with different temperatures and stress-voltages. The results of the stress tests are taken in order to calibrate and verify commonly used models for the time-dependent dielectric breakdown of MOS gate dielectrics. The devices under test themselves have different sizes in order to review whether the gate dielectric breakdown is dependent on the gate-area or on the perimeter of the gate-dielectric. This makes it easier to make a projection from a small number of devices to several billion devices. At the end of the measurement, there will be the bathtub curve whereof the parameters of existing and self postulated models can be verified.

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