Flexibility studies on ultra-thin silicon substrates

L. Wang, M. Bartek, A. Polyakov, K.M.B. Jansen, L.J. Ernst

***Abstract*—In this paper, some results of our work on flexibility studies on ultra-thin poly- and single crystalline silicon layers on thin polyimide substrates under mechanical deformation are presented. By embedding ultra-thin silicon layers into a thin flexible polyimide substrate and patterning the silicon into square or hexagonal segmentations, an increased mechanical flexibility and resistance against cracks is reached. The occurrence of cracks in the silicon and the dielectric layers under controlled bending (on cylinders with diameters of 2 - 10 mm) and tensile loads is studied, using bending and tensile tools being specially designed for this purpose. Specimen observation was performed, using an optical microscope combined with digital recording. Crack occurrence evaluation was performed using pattern recognition software. The results show that cracks appear first in the dielectric layers in-between the silicon layer segments and only at higher loads they propagate or are initiated within the silicon itself. The development of first cracks depends significantly on the segmentation size of the silicon layer. This affects both the crack density and the crack width. The crack density increases sharply with the strain at early stage and then increases slightly. The crack width increases steadily. The highest flexibility result reached here shows no crack occurrence for bending tests on a cylinder with 2 mm diameter. A maximum strain failure criterion was established for the ultra-thin thermal silicon dioxide layer by specific bending and tensile tests.**

***Index Terms*— Flexible substrate, Substrate transfer, Ultra-thin substrate.**

I. INTRODUCTION

THE demand to miniaturize products especially for mobile applications is continuing to drive the evolution of electronic products and manufacturing methods. One key to miniaturization developed in the past was the use of unpackaged, bare die [1]. Conventional IC packages form a rigid shell around silicon IC dies. Their purpose is to provide environmental protection, electrical interconnect and heat dissipation. Despite the fact that majority of current silicon ICs are realized in a very thin top layer of the silicon substrate (<10 µm), the typical thickness of packaged IC dies exceeds 150µm. The main reason for this is twofold: a) front-end processing relies on single-crystalline silicon substrates having sufficient thickness for reliable wafer handling, even at very high temperatures; b) substrate thinning below 100 µm is not a trivial operation, which moreover complicates handling and will therefore be applied only when justified by the intended application.

During recent years, studies of wearable computer systems, smart clothing, sensitive skin and Radio-Frequency Identification have been executed. Applications of sticking the RFID and smart clothing on non-planar (even high curvature) surfaces of objects issue the challenges to flexible and stretchable substrates. Ultra thin chips (i.e. silicon dies thinned down to ~50 µm total thickness) lend themselves to reach the flexibility to a certain extent [2, 3]. However, sufficient stretchability is not attainable through only thinning the silicon substrates.

Previously [4, 5], substrate transfer technology for SOI and non-SOI single-crystalline silicon wafers was demonstrated allowing for high-performance low-power RF applications. One of its very interesting variations is transfer onto flexible ultra-thin (<10 µm) polyimide substrates. Initial studies have demonstrated that active circuitry maintains its functionality even for high bending curvatures, opening new possibilities for embedding electronics in MEMS applications and realization of disposable smart adhesive labels. If next to the vertical thinning also a lateral partitioning of the silicon substrate on sub-millimeter scale is applied, then 3D deformable electronics could be realized. By varying the partition dimensions and the geometry of connecting bridges, the level of acceptable deformations can be controlled. In practical realization such patterned silicon structures have to be embedded into a polymer film to provide local stress relieve and protection. In many applications it will be useful to embed IC's into flexible or even stretchable substrates. The targeted applications of this technology are wireless ID tags and sensor networks.

In this contribution, results of our work on mechanical reliability issues of poly- and single crystalline silicon on ultra-thin polyimide substrates are presented. To improve

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reliability, square and hexagonal segmentation was applied to the silicon layer before it was transferred onto an ultra-thin polyimide substrate (<10 µm) using a wafer-to-wafer substrate transfer technique based on a temporary glass carrier. Generation of cracks within the silicon and dielectric layers was then studied under controlled bending (on cylinders with diameters of 2 - 10 mm) and tensile loads.

Test samples were prepared on a 4 inch silicon wafer and consisted of a 0.5 µm thick silicon layer, sandwiched between 300 nm thermal and 500 nm PECVD silicon dioxide layers. The silicon layer was segmented into hexagonal or square partitions varying in size from 150 to 2000 µm. The segmented silicon layer was then transferred onto a thin polyimide carrier substrate (5-10 µm Durimide 115A) using a substrate transfer technology. During this substrate transfer procedure, the polyimide was first deposited by spinning a required layer thickness, then cured and covered by a PECVD silicon dioxide layer. This structure was subsequently adhesively bonded to a temporary glass carrier, using acrylic glue such that the adhesion promoter was applied at the wafer edge only. After the removal of bulk silicon by wet etching, the segmented ultra-thin silicon on a PI substrate sample can be pealed off from the temporary glass carrier and is ready for characterization.

The formation of cracks was studied experimentally using bending and tensile tools, specially designed for this purpose. Specimen observation was done using an optical microscope with possibility of digital recording and evaluation by pattern recognition software. The results show that the cracks appear first in the dielectric layers in-between the silicon layer segments and propagate at higher loads only, or are generated within the silicon itself. The development of first cracks depends significantly on the silicon layer segmentation size, which affects both the crack density and the crack width. The crack density increases sharply with strain at the early stage and then increases slightly. The crack width increases steadily. By optimizing the segment structure, segment size and gap between segments, a high flexibility result can be reached, while no cracks are detected under the bending tests till 2 mm diameter.

The mechanical properties of poly-silicon and oxide thin film differ much from those of the bulk material according to the research results [6, 7]. Fragmentation tests in the uniaxial mode were performed on poly (ethylene terephthalate) film coated with a silicon oxide layer of thickness ranging from 30 to 156 nm to investigate the strength. The cracks appear first at strains of 1.2% to 2.0% for the oxide coated thickness ranging from 30 to 156 nm respectively [6]. The fracture strain ranges from 12% to 22% (This depends sharply on the sample size and temperature in bending tests on nano-scale silicon oxide wire at intermediate temperatures using a AFM-based technique [7]). In this study, the maximum strain failure criterion of the ultra-thin thermal silicon dioxide layer could be reached by specific bending and tensile tests. The results of the tensile and the bending tests match very well.

II. Sample Design

In order to investigate the effect of segment sizes and the gaps between segments on the flexibility and reliability of the structure, the samples were designed with square and hexagonal partitions (Fig. 1) varying in side length from 150 µm to 2000 µm and in gap size from 20 µm and 250 µm. The following table (table 1) shows the details.

Table 1
The segment side length and segment gap used for different samples.

sample	segment side length (µm)	segment gap (µm)
1	150	20
2	300	40
3	450	60
4	450	120
5	600	80
6	2000	250

The poly-silicon layer of the test samples is sandwiched between 300 nm thermal and 500 nm PECVD silicon dioxide layers. The vertical structure schematics of the samples are shown in the following figure (Fig. 2).

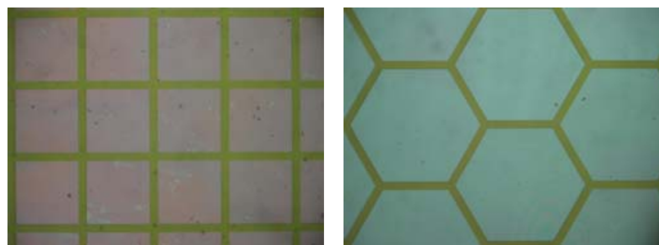

Fig. 1: Square and hexagonal segmentation schematics.

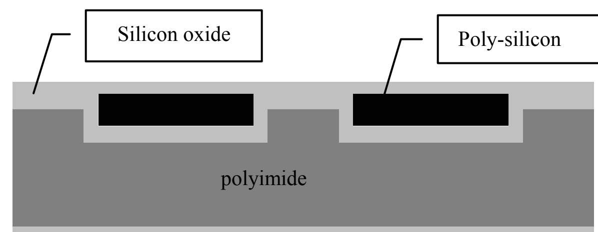

Fig. 2: Cross section of the test structures.

III. Sample preparation

The sample preparation starts with deposition of a 300 nm thermal oxide layer on 4" p-type silicon wafers (Fig. 3a). Then, a 500 nm polysilicon layer is deposited and patterned with the test structures layout (i.e. square and hexagonal

segmentation) (Fig. 3b), followed by a 500 nm-thick PECVD oxide layer (Fig. 3c).

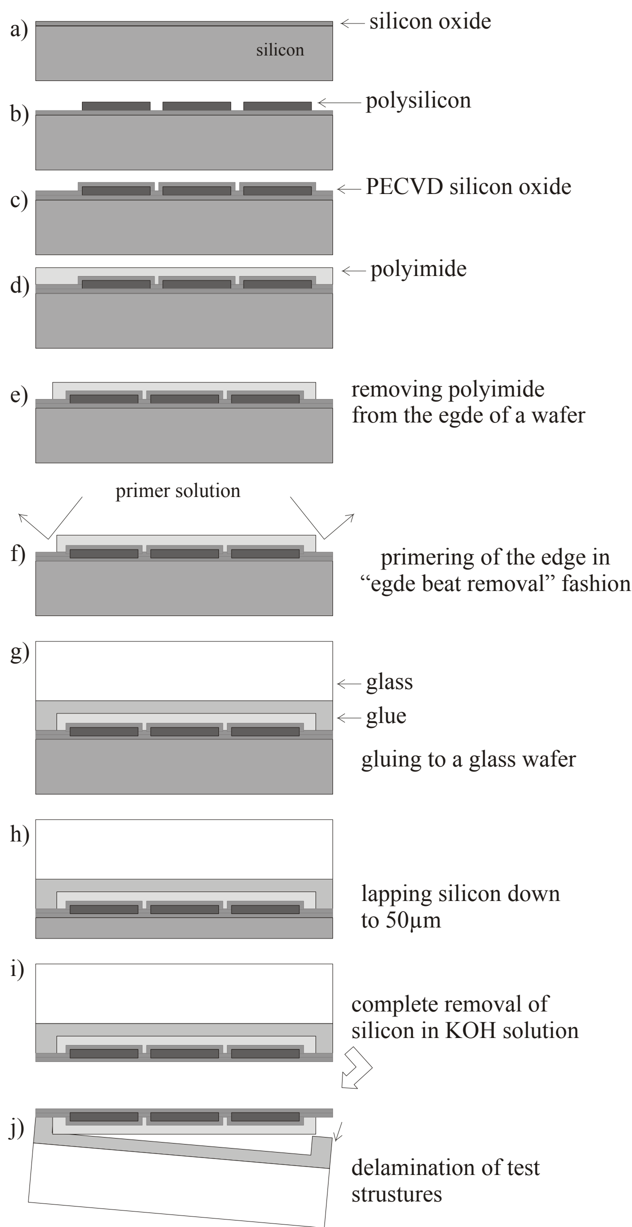

Fig. 3: Schematic process flow for ultra-thin silicon substrates fabrication on a thin polyimide substrate.

The 8-9 µm-thick layer of photosensitive Durimide™ polyimide from Arch Chemicals is spin coated at 1000 RPM (Fig. 3d). The polyimide is then soft backed at 120 °C for 6 minutes. A photoresist layer of ~2 µm is coated and approximately 1 cm of the wafer edges is exposed. A TMAH based positive photoresist developer is used to develop the photoresist and to remove the polyimide from the edge of the wafer (Fig. 3e). Afterwards the photoresist layer is removed in acetone; the final polymerization of polyimide takes place at ~300°C for 1 hour in nitrogen environment.

The wafer bonding is accomplished using UV-sensitive acrylic glue. The glass substrates (AF45 type from Schott used in the experiment) and edge of the wafer are coated with primer (Fig. 3f). The gluing procedure is similar to the SOA process [4] (Fig. 3g).

After the bonding, the silicon is lapped down to ~ 50 µm thickness (Fig. 3h), and the remaining silicon is removed in 33% KOH solution at 80°C (Fig. 3i). The thermal oxide layer is used as an etch top. Finally, samples are peeled off the glass substrate (fig.3j).

IV. Test Setup

Special tensile and bending test setups were designed and fabricated. On these, the specimen observation can be done by optical microscope during tensile and bending tests. The cracks could be detected and recorded by means of an optical microscope with digital recording, the magnification ranging from 25 up to 3000 times and a maximum image resolution of 4800 x 3600 pixels is obtained.

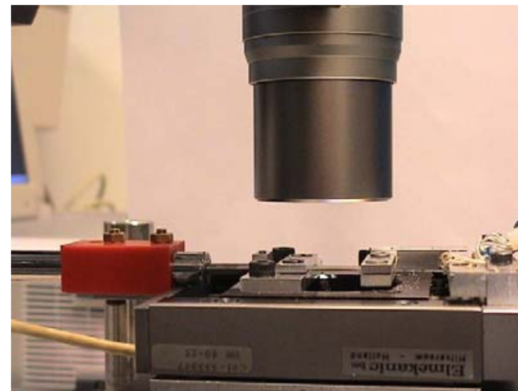

Fig. 4: Photograph of the tensile test setup.

The tensile tool (Fig.4) includes the clamper, a manually controlled micro-screw loading part, and force and displacement sensors. The data is recorded by computer after collecting, amplifying, and transforming the force and displacement signals into electric signals.

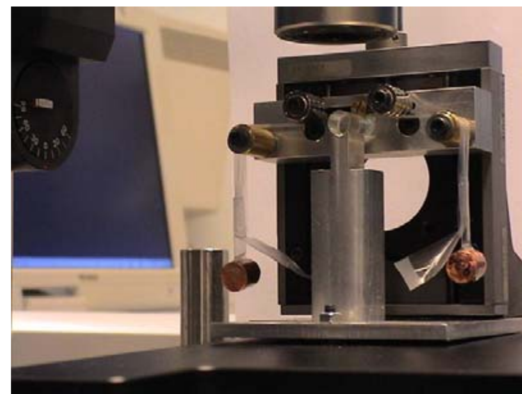

Fig. 5: Photograph of the bending test setup.

A dedicated bending test tool (Fig.5) allows the sample to be curved around glass cylinders with different diameters. Due to the ultra-thin sample and residual stress, it is necessary

to hold the sample by controlled small force. The lens can be rotated to observe the cracks around the glass cylinder surfaces.

V. Bending Test

The samples with square and hexagonal segments varying in size and gap are wrapped around the glass cylinders having different diameters (Fig. 6). The bending procedure is made up from the following steps:

Fig. 6: The schematic bending direction.

First, bend the samples around the glass cylinder with diameter 10 mm, then scan the Region Of Interest (ROI) with the microscope to detect the cracks; if there are some cracks, record the cracks. Subsequently, bend the sample around the glass cylinder with diameter 8, 6, 4, 2 mm.

Table 2
The results of bending tests for samples with square segmentation.

	Segment side length	Segment gap (µm)	Diameter for onset crack
1	150	20	4
2	300	40	2
3	450	60	2
4	450	120	----
5	600	80	8
6	2000	250	no test

Table 3
The results of bending tests for samples with hexagonal segmentation.

	Segment side length	Segment gap (µm)	Diameter for onset
1	150	20	no test
2	300	40	----
3	450	60	2
4	450	120	2
5	600	80	6
6	2000	250	10

The crack appears first on the top or second oxide layer (assuming the top layer the first layer, see Fig. 6) between the segments. The cracks are parallel with the axis of the bending cylinder (Fig.7). The formation of the first crack depends significantly on the segment size and the gaps between the segments for samples with square or hexagonal segments. According to the results in Table 2 and 3, the diameters for the onset of cracking increase with increasing segment size. They decrease with increasing gaps between the segments of constant segment size. For the sample with the square pattern of 450 µm side length and 120 µm gaps and the sample with the hexagonal segment of 300 µm and 40 µm gap, there is no crack, even not for bending around a cylinder with 2 mm diameter. However, for the samples with the 150 µm side length segment we do not observe this trend, the reason probably is the stress concentration due to the little gaps between the segments.

Fig. 7: The cracks under the bending test.

VI. Tensile Test

Only one sample with a segment size of 300 µm side length and 40 µm gap was used in the tensile test because of the lack of samples. The cracks take place in-between the segments in the first and second layer of oxide (from the top side), the direction of cracks is perpendicular to the loading direction (Fig. 9). The first crack appears when the strain reaches a value of 1.1% (as shown in Fig. 8).

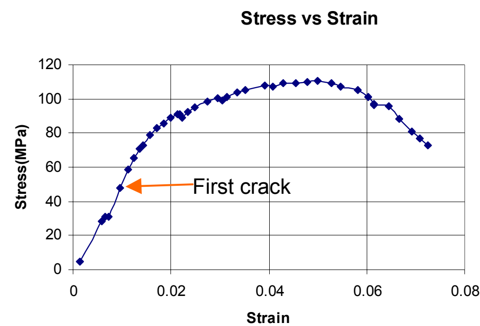

Fig. 8: Stress vs. strain for the sample with 300 µm side length segment in tensile test.

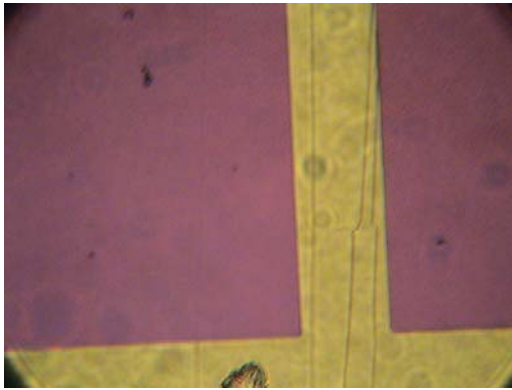

Fig. 9: cracks under the tensile loading

VII. FAILURE CRITERION OF ULTRA-THIN OXIDE FILM

The sample is made up by two 500 nm silicon oxide layers sandwiching the polyimide layer with 8 µm thickness. Fig. 10 shows the structure and bending direction schematics. The images were digitally recorded and processed to analyze the crack number and crack width.

Fig. 10: Structure and bending direction.

The first crack was detected when the sample was bended around the cylinder with diameter of 2 mm. The cracks are parallel with the axis of the bending cylinder. According to the relation between the curvature and the strain, the failure strain for the first crack is approximately 0.8%.

In tensile testing, the Region Of Interest of the microscope is fixed on the 600 x 450 µm window with an image resolution of 1600 x 1200 pixels under magnification of 500 times. The images were recorded and processed.

Fig. 11: the cracks on the silicon oxide under the tensile loading.

Fig. 11 shows the cracks on the silicon oxide layer under tensile loading. All the cracks are pependicular to the loading direction.

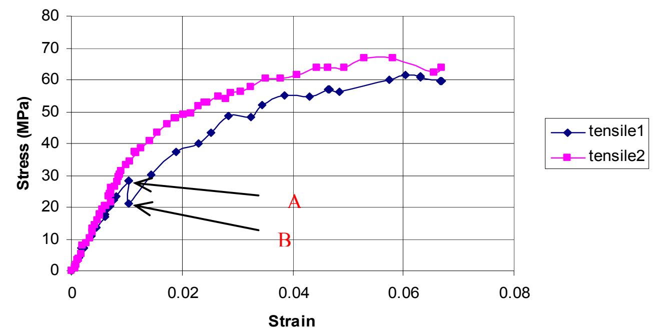

Fig. 12: The relation between stress and strain for tensile tests

From Fig. 12, we can see that the two tensile test curves match well within a strain range less than 1%. The crack appears first at a strain of 0.77% and 0.9% for sample 'tensile 1' and 'tensile 2,' respectively. This is consistent with the result of the bending tests. The 'tensile 1' case was being hold for 15 hours with a of 1.04%. This strain ia kept constant while the stress decreases significantly because of the polyimide viscoelastic properties (transition from A to B in Fig. 12). The images have been analyzed to investigate the crack density and width during the loading.

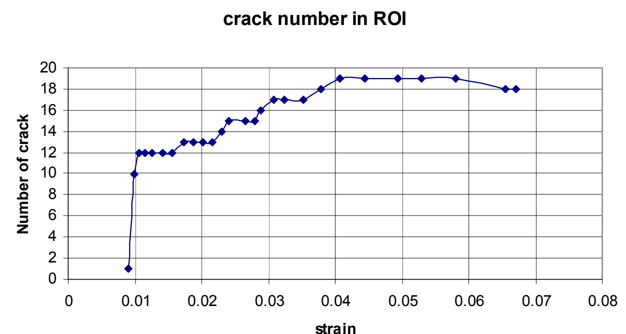

Fig. 13: The number of cracks in the region of interest (600 x 450 µm).

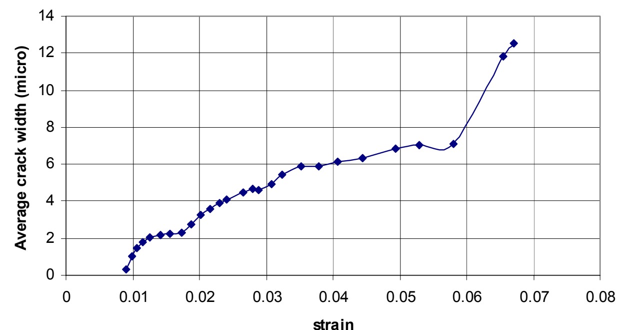

Fig. 14: The crack width in the region of interest (600 x 450 µm).

The crack direction is perpendicular to the loading direction in tensile tests. From Figs. 13 and 14, we can see that the crack density increases sharply with the strain at early stage

and subsequently increases slightly. However, the crack width steadily increases until the sample breaks.

VIII. CONCLUSIONS

A promising flexible substrate concept based on vertical thinning and lateral partitioning is proposed. In order to investigate the effect of the segmentation and gap sizes on the mechanical reliability, test samples were designed and prepared on a 4 inch silicon wafer and transferred to a thin polyimide substrate. They consist of a 0.5 μm thick silicon layer sandwiched between 300 nm thermal and 500 nm PECVD silicon dioxide layers with hexagonal or square partitions varying in size from 150 to 2000 μm. Specific tensile and bending tools were fabricated to observe the cracks by optical microscope during the loading with possibility of recording the images and analyzing the crack density and width.

The results show that the cracks appear first in the dielectric layers in-between the silicon layer segments. Only at higher loads these cracks propagate and also additional cracks are generated within the silicon itself. The development of the first cracks depends significantly on the silicon layer segmentation size, which affects both the crack density and the crack width. The crack density increases sharply with the strain at early stage and subsequently increases slightly. The crack width increases steadily. There is no crack detected under bending load on glass rods with 2 mm diameter (with magnification 500 times) for samples with square segments with 450 μm side length and 120 μm gap and hexagon segments with 300 μm side length and 40 μm gap. The results show that the flexible ultra thin substrate can be applied on non-planar or even high curvature surfaces.

The failure strain of oxide layers with 500 nm thickness under tensile load is consistent with that in bending. The first crack was detected when the strain is up to 0.8%. The crack density increases rapidly for the early stage with strain and then increases slightly. However, the width of crack increases steadily during loading.

IX. FUTURE WORKS

Bending and tensile simulation will be done to optimize the segment size, segment gap and structure parameters by Finite Element Analysis in order to eliminate the stress concentration and improve the flexibility and reliability of the ultra-thin substrate. Integrated circuits will be fabricated on the ultra-thin silicon islands and the functions on the segments can be interconnected by embedding leads into the flexible polyimide substrate.

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