

# Depletion-Free Poly Gate Electrode Architecture for Sub 100 Nanometer CMOS Devices with High-K Gate Dielectrics

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**Abstract**— In high-k and ultra thin gate dielectric systems, parasitic gate charge is a major concern. Due to the parasitic charge in the poly gate electrode, the charge carriers in the channel are affected by remote coulomb scattering, and the device performance degrades. The decrement in the drain current can be assigned to mobility degradation. However, when the gate is inversely doped, i.e., using a n-type poly gate in a PMOS-FET instead of a p-type poly gate and vice versa for a NMOS-FET, the gate depletion can be totally eliminated since the gate poly silicon is driven into accumulation when the device turns on. This inversely doped gate architectures results in a substantial performance improvement in conventional CMOS devices without using a metal gate.

*Index Terms*— advanced CMOS devices; gate engineering; remote coulomb scattering; performance improvement; gate depletion

## I. INTRODUCTION

In conventional CMOS devices, the gate depletion is a major concern as it degrades the device performance [1] and is a main hurdle for the downscaling the CMOS devices into sub 50nm regime. The poly silicon gate depletion often occurs and introduces a poly gate depletion capacitance ( $C_{pd}$ ) in series with the oxide capacitance ( $C_{ox}$ )[1]. When EOT is approaching 2nm and below,  $C_{pd}$  cannot be neglected when compared to  $C_{ox}$ . Thus the total gate capacitance ( $C_g$ ) reduces in the presence of gate depletion (fig. 1) when the devices are turned on, resulting in a reduced drain current. In order to reduce the poly

gate depletion effects, the poly silicon gate should be doped very high, about  $10^{20}$  atoms/cm<sup>3</sup>. Even at these high doping concentrations, however, the gate depletion is not fully eliminated, and more parasitic charge centers are added at the poly silicon-gate oxide interface, which further degrades the mobility by remote coulomb scattering (RCS) [2]. In order to decrease RCS, the gate should have less parasitic charges, which means that gate doping has to be decreased, as a result poly depletion increases. Thus it is obvious that both effects, poly gate depletion and RCS are unavoidable in conventional CMOS devices. According to the ITRS roadmap, the gate oxides should be scaled below 1 nm in near future [3]. When crystalline high-k gate dielectrics like  $Pr_2O_3$  are used, which are compatible with poly gate processing and which don't need a  $SiO_2$  buffer layer, the EOT can be scaled down to fractions of a nanometer [4]. The above-mentioned effects i.e. gate depletion and remote coulomb scattering of charge carriers in the channel will become more severe. As a result of these effects, performance of CMOS devices degrades. Metal gates are suggested in order to eliminate the gate depletion. But processing of metal gates is difficult.

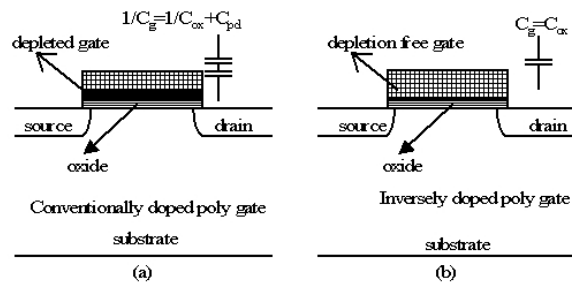


Fig. 1 Schematic diagram of poly gate-oxide interfaces of (a) conventionally doped poly gate structures and (b) inversely doped poly gate structures illustrating the total gate capacitance ( $C_g$ ).

To eliminate the poly gate depletion and RCS, in this work, we suggest alternative gate architecture, without using metal gates, which eliminates the poly gate depletion and RCS thus improving the device performance substantially.

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## II. THE GATE DOPING SCHEME

In order to eliminate PGD and RCS in poly silicon gate electrodes, we propose an alternative gate doping scheme in which the poly gates are inversely doped, i.e. the  $n^+$  poly gate in the NMOS-FET (n-channel MOSFET) is replaced by a p-type poly gate and the  $p^+$  poly gate in the PMOS-FET with a n-type poly gate. For inversely doped gates, PGD and RCS are completely eliminated since the gate is driven into **accumulation** when the device turns on as shown in fig.1. In this work, the impact of gate dopant type and gate dopant concentration on the electrical characteristics of devices having different channel lengths from 150nm down to 40nm are investigated. Simulation studies of inversely doped gates showed the expected performance improvement. This novel concept was verified experimentally with hardware.

## III. DEVICE SIMULATIONS AND FABRICATION

### A. Process and Device Simulations

PMOS-FETs and NMOS-FETs with various gate doping profiles of  $10^{15}$ - $10^{20}$  atoms/cm<sup>3</sup> and channel lengths ranging from 150nm down to 40nm with an EOT of 2nm were process simulated using TSUPREM4 [6]. The main aim of these process simulations is to obtain devices with an identical threshold voltage ( $V_t$ ). The simulated structures were then imported into the device simulator MEDICI [7] to obtain device I-V characteristics.

### B. Fabrication of Alternatively Doped Gate Devices

In order to prove the concept of the alternative gate-doping scheme, PMOS-FETs were fabricated with highly doped  $n^+$ -poly gates having a phosphorus concentration of  $10^{20}$  atoms/cm<sup>3</sup> and low-doped n-poly gates with a doping concentration  $10^{18}$  atoms/cm<sup>3</sup> respectively.

## IV. RESULTS AND DISCUSSION

### A. Current Voltage Characteristics

For better understanding of the improved I-V characteristics, lets first look at simulated C-V characteristics of a NMOS capacitor (PMOS-FET) with different poly gate doping concentrations. The C-V characteristics of the above-simulated structures are shown in fig. 2. When the PMOS-FET is turned on, due to the gate depletion the gate capacitance decreases. Even though the gate doping is increased, it is almost impossible to attain maximum possible gate capacitance  $C_{ox}$ .

When the gate of the PMOS-FET is inversely doped, i.e., a n-gate instead of a  $p^+$  gate, the gate

only depletes when the device is turned-off, retaining the maximum gate capacitance when the device turns on.

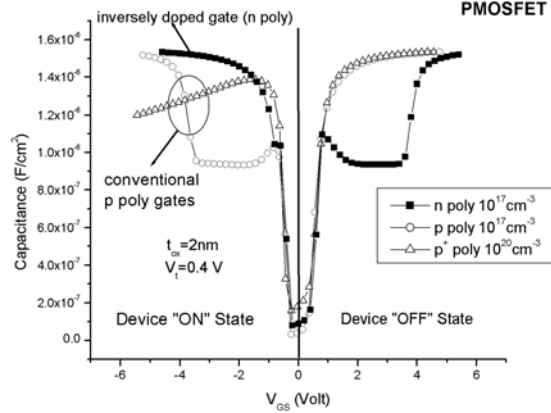


Fig. 2 C-V characteristics of a PMOS-FET (p-channel MOSFET or NMOS capacitor) with conventional poly gates and inversely doped gates.

The elimination of gate depletion in inversely doped gates was experimentally verified using PMOS-FETs with a channel length of 1.2 $\mu$ m. Although the gate doping is reduced by two orders of magnitude, from  $10^{20}$  atoms/cm<sup>3</sup> down to  $10^{18}$  atoms/cm<sup>3</sup>, the drain current increases substantially as shown in fig. 3. In the absence of gate depletion one can take full advantage of the reduced gate work function of the low-doped gate to increase the gate overdrive ( $V_{GS} - V_t$ ). Although the experimental devices are buried channel devices rather than surface channel devices, the principle still holds. Furthermore, our simulation studies show that, if one downscales the lateral device dimensions (channel length) of the device to sub 200nm, a surface channel device can be achieved with inversely doped gates [7].

The simulated device I-V characteristics are shown in fig. 4 and fig. 5 are obtained for devices with a channel length of 150nm. For inversely doped gate devices, one can observe a substantial performance improvement in terms of drain current. The improvement in the drain current in CMOS devices can be attributed to: (1) the elimination of gate depletion, as a result the total gate capacitance is maximum, (2) the mobility is enhanced since RCS is removed in the absence of parasitic gate charges. In addition, due to the reduction of  $V_t$  adjust implant dose, the doping concentration in the channel is reduced [7], thus resulting in an additional mobility improvement due to reduced impurity scattering.

The devices are further scaled down in order to study the dependency of the inversely doped gate

doping concentration on channel length of the device, while for the conventional CMOS devices,

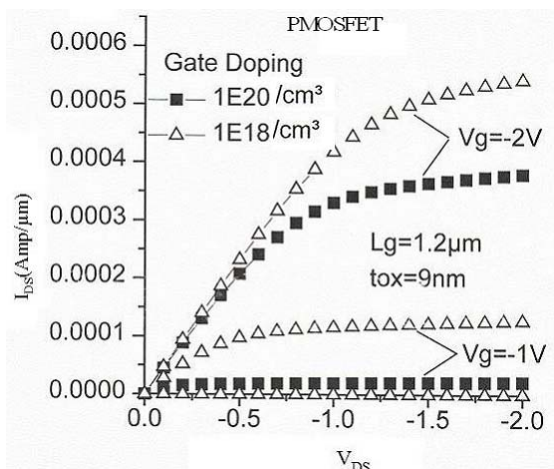


Fig. 3 Measured I-V characteristics of PMOS-FETs with inversely doped gates proving the concept.

the gate doping is fixed constantly at  $10^{20}$  atoms/cm<sup>3</sup>. For this, PMOS-FETs and NMOS-FETs with different channel lengths were process

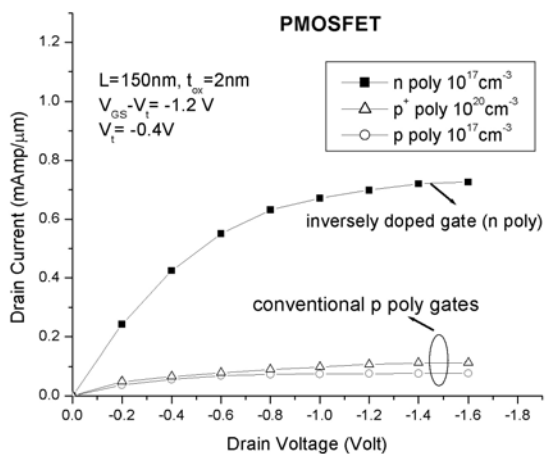


Fig. 4 Simulated I-V characteristics of a PMOS-FET with inversely doped n-poly gate ( $10^{17}$  atoms/cm<sup>3</sup>) and conventionally doped p-poly gates ( $10^{17}$  and  $10^{20}$  atoms/cm<sup>3</sup>) clearly showing the improvement in drain current.

and device simulated. In case of inversely doped gate CMOS devices, the gate doping concentration for different channel lengths are tabulated in table 1 and plotted in fig. 6. Drain characteristics of both conventional NMOS-FETs and inversely doped gate NMOS-FETs at a gate over drive of 1.2 V are shown in fig. 7. The saturation drain current ( $I_{Dsat}$ ) at a fixed gate voltage and drain voltage with a varying channel length are shown in fig. 8. Similar results for a PMOS-FET are obtained. When the

devices are scaled down, due to the short channel effects,  $V_t$  rolls off. In conventional CMOS devices, the roll-off is compensated with additional channel implants. As a result, the carrier mobility in the channel further decreases. In case of inversely doped gate devices, the  $V_t$  roll-off can be compensated by either channel implants or by adjusting the poly gate work function. Thus the alternative gate-doping scheme provides an additional degree of freedom for  $V_t$  optimization. As there is no extra  $V_t$  adjust implantation needed, the mobility can be retained to its maximum possible value, thus improving the device performance.

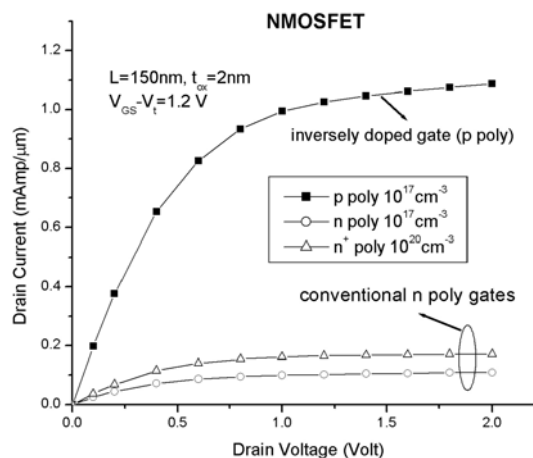


Fig. 5 Simulated I-V characteristics of a NMOS-FET with inversely doped p-poly gate ( $10^{17}$  atoms/cm<sup>3</sup>) and conventionally doped n-poly gates ( $10^{17}$  and  $10^{20}$  atoms/cm<sup>3</sup>) clearly showing the improvement in drain current.

Channel Length (L)	n-poly doping in PMOS-FET (cm <sup>-3</sup> )	p-poly doping in NMOS-FET (cm <sup>-3</sup> )
150 nm	$1 \times 10^{17}$	$1 \times 10^{17}$
100 nm	$2.36 \times 10^{17}$	$2 \times 10^{17}$
90 nm	$2.88 \times 10^{17}$	$2.47 \times 10^{17}$
60 nm	$2.3 \times 10^{18}$	$1.9 \times 10^{18}$
40 nm	$4.7 \times 10^{18}$	$4.1 \times 10^{18}$

Table 1: Gate doping dependency on channel lengths for alternatively doped gate CMOS devices to adjust the  $V_t$  roll off when no  $V_t$  adjust implants are used.

While fabricating the inversely doped gate CMOS devices, the fabrication process doesn't need an extra mask level. In advanced sub micron devices due to the drain and source junction depth limitations, drain and source should be shallow

junctions, which need low energy implants. While on the other hand, the gate needs a higher energy

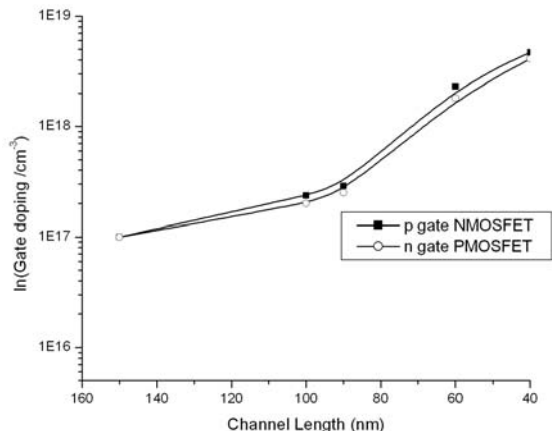


Fig. 6 Dependency of gate doping of an inversely doped gate on channel length when no  $V_t$  adjust implants are done.

implant when compared to drain and source implants. Thus, it is necessary to have two different implantation steps, one for the source/drain and the other for the poly gate. As a result, there is only one process step modification, a n-type gate doping is needed instead of a p-type doping in case of a PMOS-FET and vice versa in case of a NMOS-FET to achieve the inversely doped gate architectures.

### B. A.C Characteristics

Further preliminary work on inversely doped gate architectures showed us a significant performance

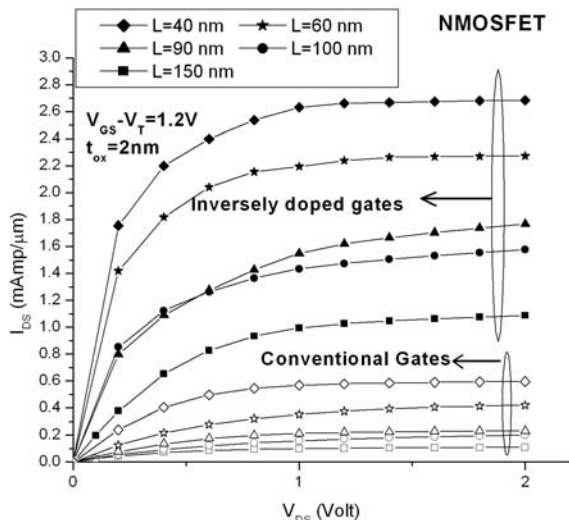


Fig. 7 A comparison of simulated drain current characteristics of a NMOS-FET with conventional and inversely doped gates at different channel lengths clearly showing the improvement in drain current.

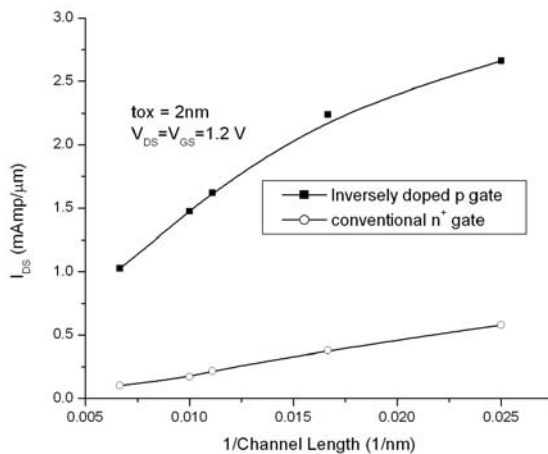


Fig. 8. Variation of saturation drain current ( $I_{Dsat}$ ) for NMOS-FETs with conventional and inversely doped gate counterparts at different channel lengths.

improvement in transconductance and cutoff frequency of the device. Fig. 9 shows the transconductance of NMOS-FET devices. The improvement in trans-conductance of the devices is due to the improved capacitance and mobility apart from the improved over drive due to eliminated poly gate depletion and RCS. Similar results were obtained for the PMOS-FETs.

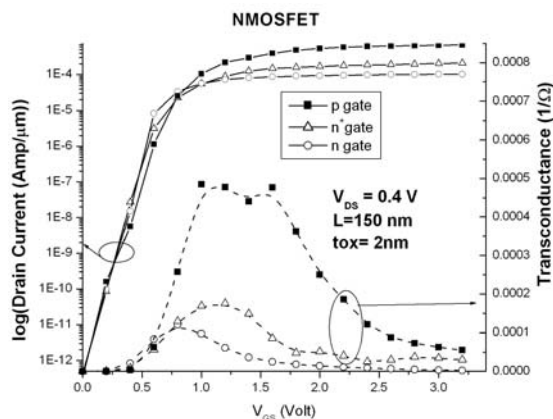


Fig. 9: Simulated sub threshold characteristics and corresponding transconductance ( $g_m$ ) of NMOS-FETs.

## V. CONCLUSION

In this work, we showed with usage of inversely doped gate architectures, the poly gate depletion and remote coulomb scattering effects can be eliminated without the need of introducing any metal gates. These inversely doped gate architectures result in a substantial performance improvement. The use of alternative doping scheme is very economical as it can be used with the

existing process lines without introducing any major process step variations.

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#### REFERENCES

- [1] R. Rios and N. D. Arora, 1994 IEDM Technical Digest, p. 613.
- [2] F. Gámiz, et al., Semicond. Sci. Technol., 18 (2003), p 927.
- [3] <http://public.itrs.net/>
- [4] U. Schwalke, et al., ESSDERC, Sept. 2002, p. 407.
- [5] TSUPREM-4, Two Dimensional Process Simulation Program User's manual, SYNOPSYS Corporation, USA, 2002.
- [6] MEDICI, Two Dimensional Device Simulation Program User's manual, SYNOPSYS Corporation, USA, 2002.
- [7] R. Komaragiri, F. Zaunert and U. Schwalke "Proceedings of Semiconductor Advances for Future Electronics 2004, Nov. 25 – 26, 2004 – Veldhoven, The Netherlands.