

Oxide to oxide wafer bonding for three dimensional (3D) IC integration technologies

M.Cannavo', H.W.van Zeijl, G. Pandraud, J. V. Driel, T. Alan, P.M.Sarro

Abstract — In this paper a temporary bonding process that can be performed before device fabrication is investigated. Silicon oxide is selected as temporary bonding layer. A 500 nm thick silicon oxide layer is thermally grown on both wafers and the oxide on one wafer is patterned using a conventional photolithographic process. The presence of a pattern allows penetration of an (IC compatible) oxide etchant between the wafers for the final separation of the process wafer from the handle wafer. In particular the influence of the type of pattern and the available bonding area on the bonding strength is investigated. Three configurations with a different pattern distribution are studied. After bonding the wafers are annealed for one hour in a vacuum furnace at temperatures between 100°C and 400°C with a 200 mbar pressure. The bond strength is evaluated using the tensile strength test. An average value of 1350 MPa is measured, with higher values obtained for the configuration with the reduced bonding area.

Index Terms— Bond strength, Oxide-to-oxide waferbonding, Temporary waferbonding, Tensile strength test

I. INTRODUCTION

IN three-dimensional (3D) integration technologies, thin device wafers are often required. Thinning of the wafers is generally applied at the end of the process, with a risk of breaking fully processed, and thus high value, wafers. Moreover thin wafers are difficult to handle. Therefore, a temporary bonding of the wafer to be thinned to a support or handle wafer is used during wafer thinning and further processing. However, bonding and wafer thinning remain critical process steps and in some cases it would be preferable to perform these steps before device fabrication. In order to do this the wafer needs to be temporary bonded to a handle wafer using a method that is compatible with the thermal budget of the subsequent device fabrication process. In addition, the removal of the handle wafer must be compatible with the 3D integration process and when possible, the handle wafer should be reclaimed.

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Several bonding methods and techniques of bare silicon wafers and wafers with an intermediate layers have been studied extensively [1,2].

In particular, the silicon oxide-to-oxide wafer bonding is studied as it is being used for silicon on insulator (SOI) structures that are of interest for advanced integrated circuits, for 3D integration and for MEMS devices encapsulation [2-6]. Furthermore, oxide-oxide bonding can be performed at room temperature, while being compatible with the high temperature required for device fabrication.

For these reasons we have investigated an oxide-to-oxide wafer bonding process to be used as temporary bonding. The 500 nm silicon oxide layer is thermally grown on both wafers. On one wafer the oxide is patterned using a conventional photolithographic process and wet chemical etching. The presence of a pattern in the temporary bonding layer allows penetration of an (IC compatible) oxide etchant between the wafers for the final separation of the process wafer from the support or handle wafer. In order to evaluate the influence of the type of pattern and the available bonding area on the bonding and release of the wafers three configurations are investigated: A) the whole die is covered by bumps with different layouts; B) in each die four squares (1x1 mm² each) with a distance among them of 2.3mm are placed in the center of the die; C) same as B, but now each square contains bumps as for configuration A.

The effect of the bonding conditions, especially the anneal temperature, and the bonding pattern on the bond strength is evaluated using visual inspection and the tensile strength test.

II. PROCESS DESCRIPTION

For the experiments standard silicon wafers, p-type, 2-5 Ωcm resistivity, 100 mm diameter with a thickness of 525 μm have been used. The oxide layer was thermally grown, using a dry oxidation process in a furnace. The thickness was fixed at 500 nm. On one wafer the oxide film is patterned by photolithography. Three layouts have been designed for the 1x1 cm² die as indicated in Fig.1. In the first one (layout A) the whole die is covered by bumps with different diameters and spacing (see Table I and Fig.2). For layout B only four squares, 1x1 mm² each and with a distance among them of 2.3 mm are designed. Finally, layout C is similar to B, but each square has now bumps as for layout A. The bumps in layout A and C are configured either in a “chessboard” manner or they

are positioned with equidistant spacing in both the vertical and horizontal direction, as schematically indicated in Fig.2.

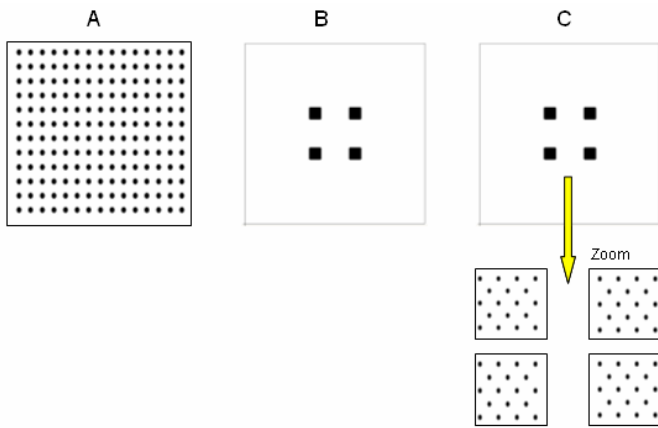


Figure 1. General view of the three die layouts used. A close-up of configuration C is also shown.

TABLE I. Size (diameter D) and spacing (P) of the patterned bumps used in the A and C layouts.

Layout	Layout A	Layout C
Chessboard with a diameter (D) of $5\mu\text{m}$ and a pitch (P) of $11\mu\text{m}$	A I	C I
Bumps vertically and horizontally equidistant with $D = 5\mu\text{m}$, $P = 12\mu\text{m}$	A II	C II
Bumps vertically and horizontally equidistant with $D = 4\mu\text{m}$, $P = 10\mu\text{m}$	A III	C III
Chessboard with a diameter $D = 4\mu\text{m}$, $P = 10\mu\text{m}$,	A IV	C IV

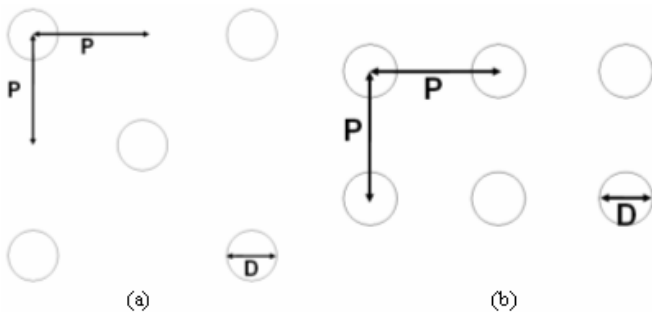


Figure 2. A schematic view of the positioning and size of the bumps related to the basic unit of the “chessboard” (a) and “vertically and horizontally equidistant” (b) configurations.

Wet etching in BHF is used to pattern the oxide. The associated under-etching will reduce the effective area of the bump involved in the bonding. For example, in Fig. 3 we can

see a structure of the type “A II” bump (nominal diameter of $5\mu\text{m}$) that is undercut of about 390nm . This means that the final diameter is in this case about $4\mu\text{m}$. In Fig. 4 there is a drawing of the same bump, illustrating the loss of bonding area due to the isotropic nature of the wet etching solution used to pattern the bump. Based on SEM (Scanning Electron Microscope) measurements we observed that all the bumps of the different layouts have a diameter of about $1\mu\text{m}$ less than the nominal values. The effective bond area is then corrected for this underetch effect.

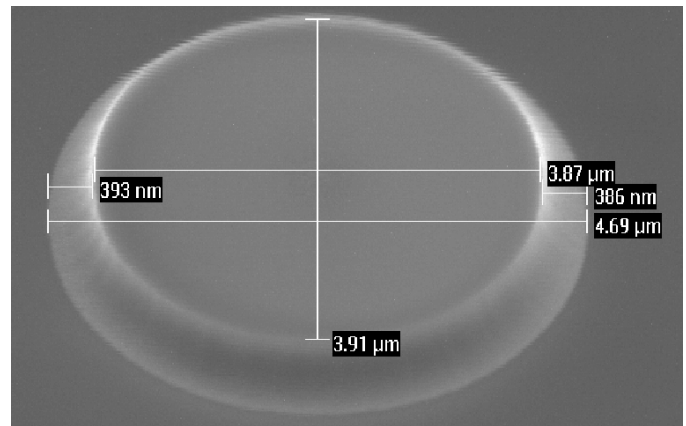


Figure 3. SEM image of a patterned bump (A II layout) clearly showing the underetch.

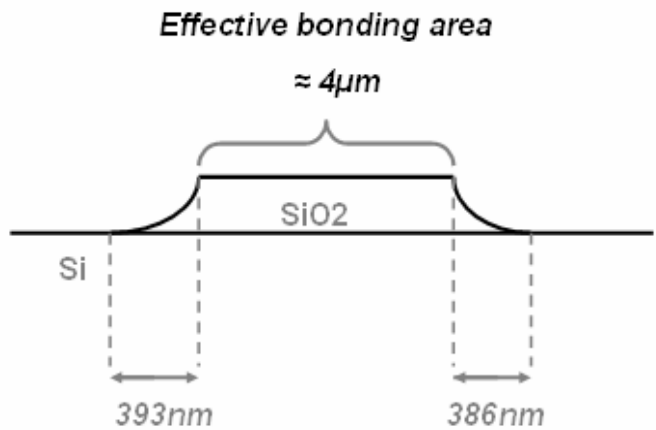


Figure 4. Cross section of the etched bump, illustrating the reduction in effective bonding area due to underetching.

Before bonding the patterned wafer to the non patterned one, we used a standard cleaning procedure with 100% HNO_3 and 65% HNO_3 followed by a Marangoni cleaning. This is a special cleaning procedure that provides ultra clean surfaces [7,8].

The wafers are then bonded at room temperature by applying a slight pressure over the entire wafer. The bonding achieved at room temperature is usually relatively weak. Therefore, the wafer stack needs to undergo an additional heat treatment to strengthen the bonds across the interface [4,9].

An annealing was thus performed for one hour in a vacuum furnace at three temperatures (100, 200 or 400°C) and with a 20 kPa pressure.

By patterning the oxide before bonding, a free path is created for an oxide etching solution that can thus penetrate in these cavities between the two wafers and remove the oxide temporary bonding. By selecting IC compatible chemicals, the separation can be performed without damaging the devices present in the wafer and the handle wafer can be reclaimed.

After bonding the wafers are cut in 1x1 cm² dies. For the tensile strength test, each die is glued between two steel blocks (see Fig. 5) and mounted in a draw-bench break-strength test set up. The specimen under test is pulled normal to the bonding interface until fracture occurs. The maximum force (F_m) at fracture is measured and the tensile strength σ_m can be calculated using the following expression:

$$\sigma_m = \frac{F_m}{A_b} \quad (1)$$

where A_b is the effective area of the bonded surface.

The alignment of the steel blocks is of critical importance. Small deviations from the normal of the bonding interface already induce a bending moment, which causes premature failure of the specimen tested (the sample should be placed into the center of the steel blocks to assure that the pull axis is perpendicular to the sample surface).

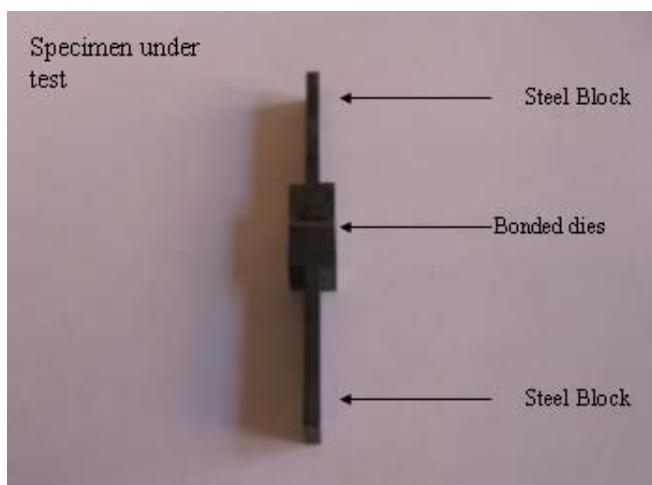


Figure 5. Optical photograph of a specimen under test

III. RESULTS AND DISCUSSION

The values of the bond strength as function of the inverse bonded area are plotted in Fig.6. From these preliminary measurements it appears that there is a larger spread in values for some configurations and surprisingly that the stress increases with the reduction of the bonded area.

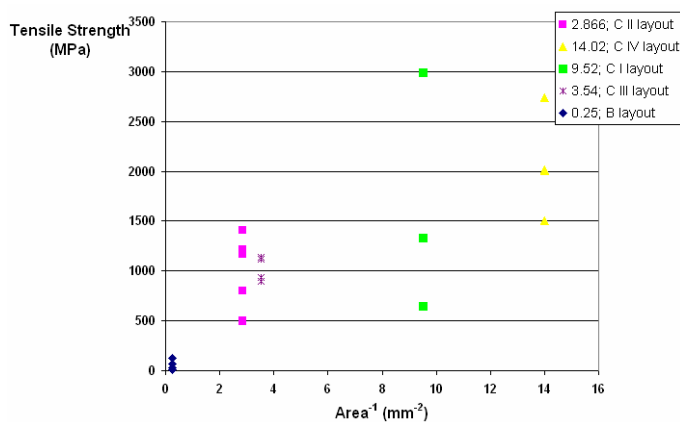


Figure 6. Tensile strength as a function of bonded area (C and B designs)

In fact the largest values are obtained for samples of the C design which have less bonding area (from 0.07 mm² to 0.35 mm²). For the layout A, with a bonding area from 1.78 mm² to 8.72 mm² not enough significant data could be collected for a proper comparison. In fact, the poor bonding observed in this case could be caused by process induced wafer curvature due to the patterning process, as this layout contains a very large number of bumps compared to the other designs. The compressive stress of the patterned oxide can cause wafer bending.

The better results given by the C design as compared to the B design could also be an indication of the fact that when the bonding area is “pixilated” the chance that a particle on the oxide will affect the bonding is also reduced.

A more detailed analysis of the results obtained with configuration C is summarized in Figs 7 and 8.

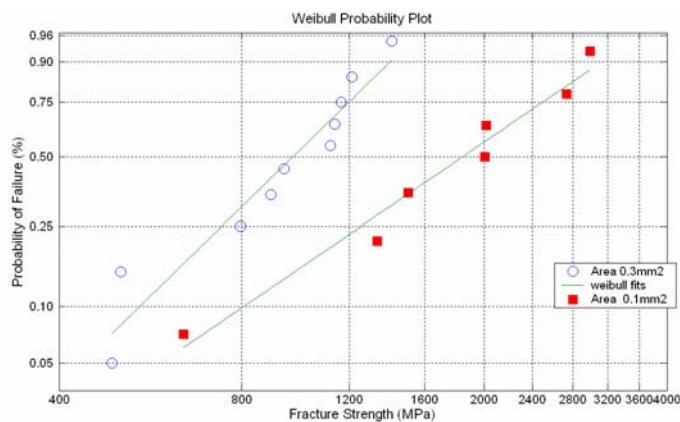


Figure 7: Weibull Probability Plot for samples with the C layout

A remarkable difference between the different die-layouts can be seen. Once again the configurations with less bonding area give better results. In Fig. 7 a Weibull distribution plot, based on the Weibull probability distribution is depicted. The Weibull distribution is one of the most widely used lifetime distribution plots in reliability engineering. In Fig. 8 a plot of

the Poisson distribution is shown that is used to model the number of events occurring within a given time interval.

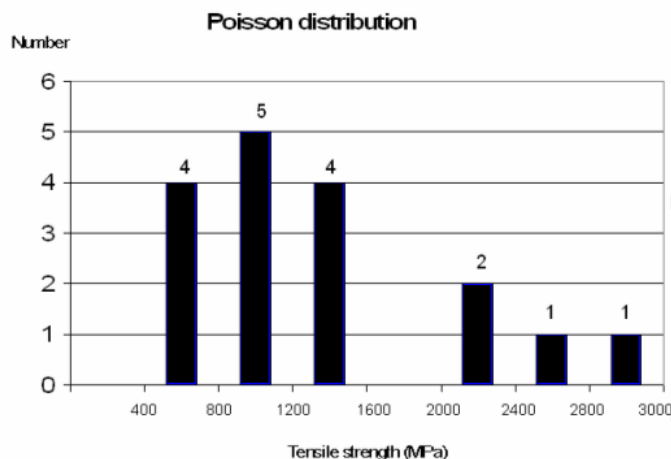


Figure 8: Poisson distribution of the bond strength for the C layout

An average value of 1350 MPa for the bonding strength with a standard deviation of 721 has been measured. This value is really high, because the maximum tensile strength reported in the literature is approximately 300 MPa [4, 10].

There are several factors that can explain this result. One of them is that during bonding, due to the small patterned area in a die, the applied pressure pushes the silicon of the patterned wafer (in between bumps and bump area) into contact with the silicon oxide of the non patterned wafer, enlarging the effective bonded area (Fig. 9). In fact, in some dies, debonded after the tensile test, a microscope analysis showed signs that indicate a silicon-oxide bonding.

To avoid this, a new design that increases the bonding area to avoid the silicon-oxide bonding is being prepared.

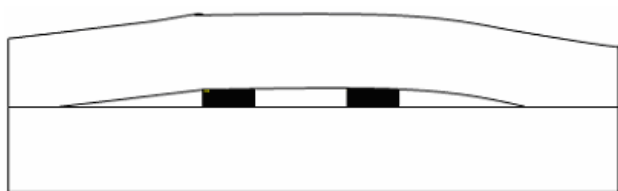


Figure 9. Silicon-to-oxide bonding in addition to oxide-to oxide bonding due to die bending during initial bonding

IV. CONCLUSION

We have developed an oxide-to-oxide wafer bonding process for temporary bonding, using a patterned oxide on one wafer which results in successful bonding. The process uses temperatures lower than 400°C and is fully IC compatible. Three different die layouts have been designed to study the influence of the patterned area (size and distribution) on the bond strength. The bond strength is determined using the tensile strength test. Successful bonding is observed even for

samples with relatively small bonding areas. However, in some cases, dies, debonded after the tensile test, showed signs of undesirable silicon-oxide bonding.

A modified design which considers larger and denser bonding areas is being considered. The modified layout should avoid undesirable silicon-oxide bonding while achieving a strong, but temporary, i.e. removable, oxide-to-oxide bonding, as required for 3D IC integration technologies.

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REFERENCES

- [1] S. H. Christiansen, R. Singh, U. Gösele, "Wafer direct bonding: from advanced substrate engineering to future applications in micro/nanoelectronics", *Proceedings of IEEE* Vol. 94, No. 12, (2006)
- [2] Tommi Suni, "Direct wafer bonding for MEMS and microelectronics", VTT publications 609.
- [3] A. Plohl, G. Krauter, "Silicon-on-insulator: materials aspects and applications", *Solid-State Electronics* 44 (2000) 775-782.
- [4] F. Sugimoto, Y. Arimoto, "Bond strength of bonded SOI wafers" (1992)
- [5] T. Abe, T. Takei, A. Uchiyama, Y. Nazakato, "Silicon wafer bonding mechanism for silicon-on-insulator structures" (1990).
- [6] K. P. Larsen., J. T. Ravnkilde, O. Hansen, "SOI silicon on glass foe optical MEMS" (2003).
- [7] J. Marra, J. A. M. Huethorst, "Physical principles of Marangoni drying" (1991).
- [8] O. Zikanov, W. Boos, K. Wolke, A. Thess, "A model for thermal Marangoni drying" (2000).
- [9] M. Wiegand, M. Reiche, U. Gösele, K. Gutjahr, D. Stolze, R. Longwitz, E. Hiller, "Wafer bonding of silicon wafers covered with various surface layers", *Sensors and Actuators* 86 (2000) 91-95.
- [10] A. Berthold, B. Jakoby, M. J. Vellekoop, "Wafet-to-wafer fusion bonding of oxidized silicon to silicon at low temperatures", *Sensors and Actuators A* 68 (1998) 410-413