

A Configurable Multi-Mode Dual Slope ADC in 130nm CMOS for Biomedical Signal Acquisition

Harish Balasubramaniam, Wjatscheslaw Galjan and Wolfgang H. Krautschneider

Abstract—A configurable multi mode dual slope ADC for acquisition of biomedical signals has been implemented in a 1.2V/130nm CMOS technology. Configurability of the ADC in terms of speed, resolution and accuracy make this ADC adaptable for multiple applications. The ADC has eight configurations with a highest resolution of 13 bits at 38.3kS/s and highest performance of 72.56kS/s at 11 bit resolution. The reconfigurability is achieved by use of an integrated resistor array which is set externally. Proper matching techniques and low noise design allow the ADC to have accurate detection of input signal voltages as small as 25 μ V without any noise and offset reduction techniques. At a supply voltage of 1.2V the ADC can detect signals between 200mV and 1V and frequencies of up to 35 kHz nyquist rate.

Index Terms—Biomedical Signal Acquisition, Configurable ADC, Dual Slope ADC

I. INTRODUCTION

Efficient acquisition of biomedical signals requires proper integration of several low noise, high accuracy analog and digital components. Bio-signals being of the order of few millivolts are severely influenced by noise. With the low voltage headroom provided by current CMOS technologies it has become increasingly difficult to achieve a high signal to noise ratio. Use of techniques such as chopper modulation or correlated double sampling allows low noise operation but at the added expense of additional circuitry and increased offsets. Dual slope ADCs are well known for their excellent noise rejection, high accuracies and lower circuit complexities. With higher clock frequencies available from current CMOS generations, the advantages of this ADC are made available to a large range of input signal bandwidths.

In this work, a dual slope ADC which can handle all important biomedical signals, such as EEG and ECG is implemented and verified using post layout simulation. All components are integrated on chip with the exception of reference voltages which are generated externally. By variation of this voltage the ADC can be switched between high and low precisions. In addition, an externally configurable resistor

array realized on chip can switch the ADC between high and low speeds (80, 160, 320 MHz) as well as between high and low resolutions (13 to 10 bits).

II. ARCHITECTURE AND CONFIGURABILITY

The architecture of the ADC [1] is depicted in Figure 1. The ADC consists of the sample & hold circuit, a switching network followed by a configurable resistor array [2]. An integrator utilizing a low noise operational amplifier for integration of signals followed by a comparator forms the rest of the analog subsystem of the ADC. The digital part consists of a control logic based on a finite state machine, a signed counter and a serial transmission system. Integration of the resistor and capacitor on chip reduces the parasitics and hence aids in reduction of noise.

The dual slope ADC is highly configurable in terms of speed, resolution and accuracy. It has eight different modes of operation as shown in Table I which can be selected by applying control signals to the three pins *Clk_Res_Sel_0*, *Clk_Res_Sel_1* and *Clk_Res_Sel_2*. Depending on these control signals the switches in the configurable resistor array are turned on or off thereby routing the signal either through the switch or the resistor connected in parallel.

Variation of the effective resistance across the array terminals changes the integration time constant ($\tau = R_{\text{eff}}C$) and thus the maximum resolution and speed achievable by the ADC. The value of integration capacitor C is chosen as 80 pF and unit integration resistor R in the resistor array is set to 200 k Ω . In addition, the ADC allows the possibility to improve the accuracy of each bit (volts per bit) in all the modes by external variation of the reference voltages between 100 mV and 400 mV around analog ground of 600 mV resulting in accuracies ranging from 25 μ V to 100 μ V for 13 bit resolution.

III. WORKING PRINCIPLE

The ADC operation is controlled by the digital block which is made up of a finite state machine. After release of the Reset signal the ADC cycles through five states successively. These states are:

1. **IDLE** - Idle mode.
2. **AUTOZERO** - Auto zeroing of the integration capacitor to analog ground level.

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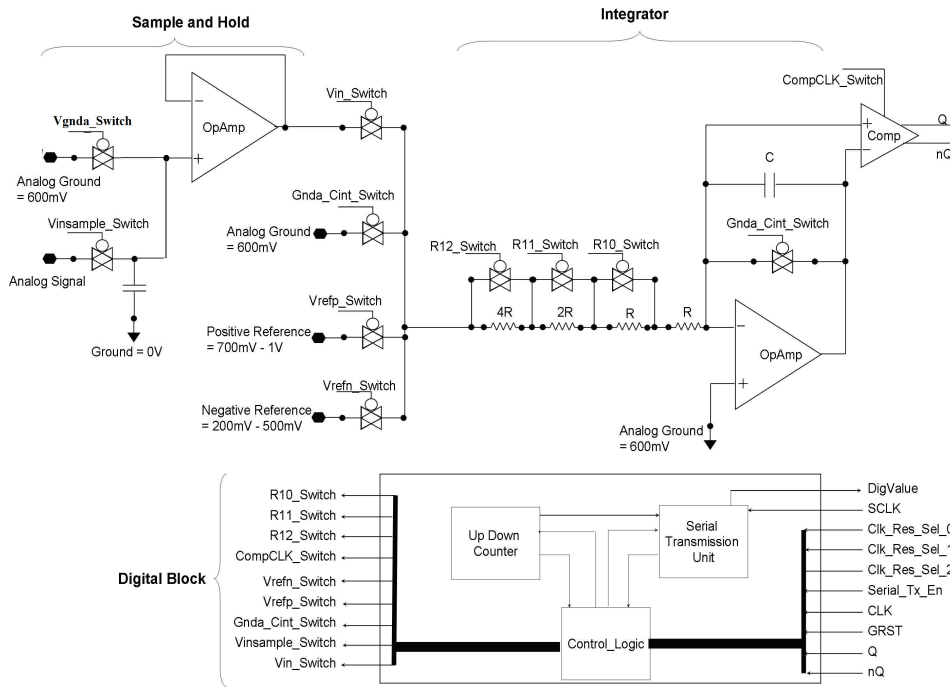


Fig. 1. ADC architecture

3. **VinINT** - Input signal integration for fixed time.
4. **VrefINT** - Reference signal Integration for variable time.
5. **EndCONV** - End of conversion and digital output transmission.

When the ADC is ready for a new conversion the state **IDLE** changes to the **AUTOZERO** mode. The conversion then proceeds with the sampling of the signal by the sample and hold circuitry and simultaneously discharging the integration capacitor terminals to 600 mV analog ground during the 128 steps of the counter. By shorting the integrator capacitor the charge, which is leftover from the previous conversion is removed. The state then switches to **VinINT** phase during which the sampled input signal is integrated for a fixed time.

The integration time is determined by the selected mode of operation and is controlled by the up down/counter in the digital logic during this phase. Therefore, the integration time depends on the adjusted resolution and the applied clock frequency and is equal to $\tau_{int} = 2^{N-1}/f_{clk}$, where N is the number of bits and f_{clk} is the clock frequency. For example, using Mode 1 with resolution of $N = 13$ bits and $f_{clk} = 80$ MHz results in a time constant of $\tau_{int} = 51.2$ μ sec.

During this phase, based on the comparator output, the polarity of the sampled signal with respect to 600 mV analog ground is also determined. At the end of the integration time τ_{int} the integration capacitor is charged with the input voltage and the state changes to **VrefINT**. Based on the input signal polarity determined during **VinINT** state, the reference voltage with opposite polarity is integrated. This means, if the input signal is greater than 600 mV analog ground than a reference of 200 mV is applied and if input signal is less than 600 mV

TABLE I
CONFIGURABLE MODES OF THE ADC.

Modes	No. of Bits N	Clock (MHz)	kS/sec
Mode1	13	80	9.57
Mode2	13	160	19.16
Mode3	13	320	38.3
Mode4	12	80	18.8
Mode5	12	160	37.6
Mode6	11	80	36.28
Mode7	11	160	72.56
Mode8	10	80	67.79

TABLE II
OPERATIONAL AMPLIFIER FEATURES

AC Gain (dB)	75.7
Phase Margin (deg)	64.5
1/f noise @1 Hz (nV/ \sqrt Hz)	287
Noise Corner Freq. (Hz)	15
CMRR (dB)	68
Slew Rate (V/ μ s) positive	12.0
negative	11.1
Input referred Offset (μ V)	70
Area (μ m x μ m)	148 x 95
Power (mW)	1.9

analog ground than a reference of 1V is applied. The counter steps accordingly in up direction for input signals greater than analog ground and down direction for input signals less than analog ground producing N-1 bit resolution for each direction and N bits for entire range. When the output of the integrator crosses the 600 mV analog ground voltage the counter stops. At this instant the counter output which is represented in a signed binary value is latched and the state switches to the **EndCONV** phase. During this state the generated data is transmitted to external circuitry by a synchronous serial interface.

After the ADC is initially switched on the digital offset calibration routine in the digital block connects the analog ground node to the ADC input and calculates the offset voltage caused by the opamp and comparator. This offset is then subtracted from the measured digital result during successive conversions.

IV. CIRCUIT DESCRIPTION

The following section explains the various components of the ADC in detail. These components have been designed to achieve high accuracy, high conversion speed and low noise behavior and are:

1. Operational Amplifier.
2. Comparator.
3. CMOS Switch.
4. Control Logic.

A. Operational Amplifier

The schematic based on [3] is depicted in Figure 2 and gives a good performance and low noise behavior along with low offset required for biomedical applications. The design consists of an n-channel differential input pair connected to

p-channel current source loads. This configuration gives the maximum possible input common mode range without using parallel n- and p-channel input stages. The differential outputs from the first stage are folded through a second stage p-channel transistor to produce single ended output. This single ended signal is connected to a class A amplifier with miller compensation which forms the output stage of the opamp. The main features such as AC gain, phase margin, noise level, CMRR, slew rate and offset voltage [4] of the opamp are given in Table II. Low noise and low offsets are achieved by using high gain and high effort on proper matching for input stage transistors [5].

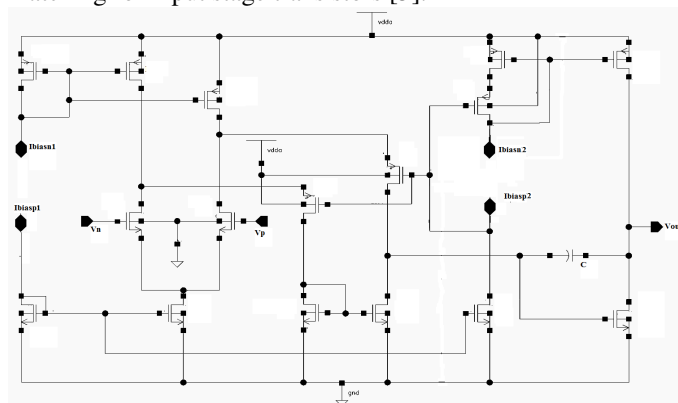


Fig. 2. Opamp schematic.

B. Clocked Comparator

The comparator [1] is a regenerative latched comparator with operation speeds of up to 400 MHz. The architecture of the comparator is given in Figure 3. The input stage amplifies the input signal difference and tilts either the transistor terminals to high or low. The cross coupled p- and n-channel CMOS transistors amplify the voltage difference and act as a bistable stage on the positive clock edge. The output of this stage is then latched by a SR latch to provide a stable output. The SR latch consists of two NOR gates whose outputs are cross connected to each others inputs. The comparator has a nominal power dissipation of less than 300 μ W with very fast settling times of the order of 300 ps. The digital logic prevents the outputs of the comparator from fluctuating by disabling the clock when not in use.

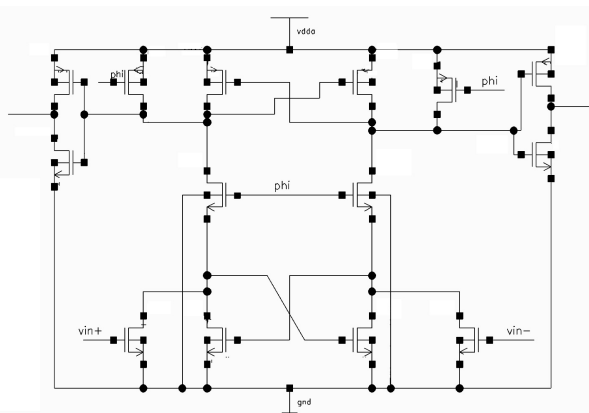


Fig. 3. Comparator schematic.

C. CMOS Switch

The architecture of the switch given in Figure 4 consists of CMOS n-channel and p-channel pair with a resistance R_{on} and R_{off} of 200 Ω and 83 M Ω . To minimize the effects of voltage dependent charge injection which increases at higher voltages, dummy transistors are connected at the CMOS switch output [1]. An inverter with faster transition time is used to provide the complementary signals to the CMOS switch.

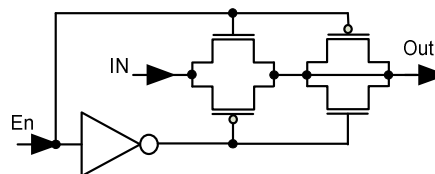


Fig. 4. CMOS switch schematic.

D. Digital Logic

The digital part is the main unit of the ADC [6] and is made of two different modules. The control logic module forms the core of the digital logic. It is made up of a finite state machine which switches through the five different states. The second module consists of an up/down counter and a serial transmitter. The control logic module is responsible for controlling all the switches used in the ADC as well as the finite state machine in conjunction with the up/down counter. The counter produces 2's complement steps to represent both positive and negative voltages with respect to the analog ground. The serial transmitter transmits the digital data serially to external source using a serial clock on the pin *SCLK* which is synchronized with the external circuit. Every transmission of converted value begins by lowering the output pin level *DigValue* to zero and waiting for reception of enable signal on the pin *Serial_Tx_En*. Then, the data is transmitted starting with the start bit followed by a 2's complement number as shown in Figure 5.

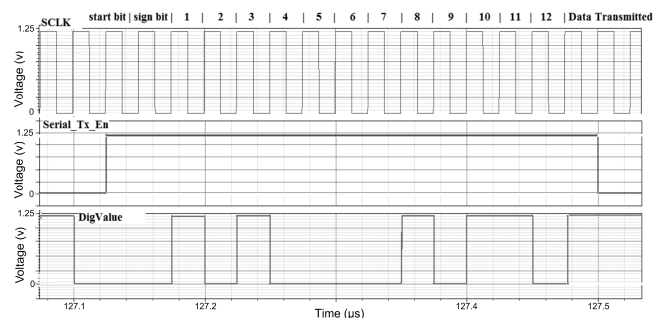


Fig. 5. Serial data transmission.

V. SIMULATION RESULTS

Static testing was carried out by applying a slowly varying ramp voltage at the input of the ADC. The calculated values show that the ADC performs better for voltages from 300 mV to 900 mV input range and gives Integral NonLinearity (INL) and Differential NonLinearity (DNL) values of less than -1.45 LSB and -0.07 LSB for all modes of the ADC, respectively.

For an input voltage range between 200 mV and 1 V, the performance degrades due to the increased charge injection from the CMOS switches, resulting in a higher INL value of -2.5 LSB.

Figure 6 shows the ADC conversion taking place for both voltages above and below analog ground of 600 mV and the Figure 7 shows the zoomed-in transfer characteristic, plotting the digital output corresponding to the analog input voltage for the configuration Mode 1. To measure the Signal to Noise and Distortion Ratio (SINAD), Signal to Noise Ratio (SNR) and Effective Number of Bits (ENOB), transient noise simulation was done and outputs recorded were used for calculating the results using equations 1 to 3, where N is the number of digitized bits, measured error is the averaged noise, AFS is the converter's full-scale input range as determined by the reference voltages, ASIGNAL[rms] is the rms value of input signal and ATOTAL_NOISE[rms] is the rms value of the total noise.

$$ENOB(N) = \log_2\left(\frac{A_{FS}}{(MeasuredError) \times \sqrt{12}}\right) \quad (1)$$

$$SINAD = (6.02 \times ENOB) + 1.76. \quad (2)$$

$$SNR = 20 \times \log_{10} \frac{ASIGNAL[rms]}{ATOTAL_NOISE[rms]} \quad (3)$$

Veriloga noise models for random Gaussian noise were added into the schematic at the integrator input for simulating noise interference from internal and external sources. Calculations reveal that for input voltages in the range between 300 mV and 900 mV, the ADC performs better. The ideal and non ideal simulated values for SNR and SINAD differ by around 7dB. The entire results of the ADC for 4 different modes with input signal ranges of 300 mV - 900 mV and 200 mV - 1 V are summarized in Table III. The layout of the ADC is shown in Figure 8.

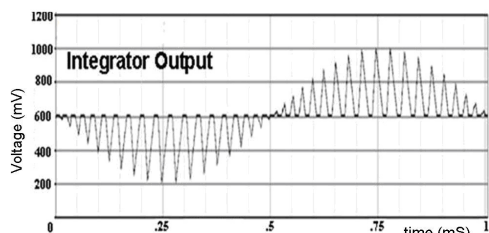


Fig. 6. ADC integrator output waveform.

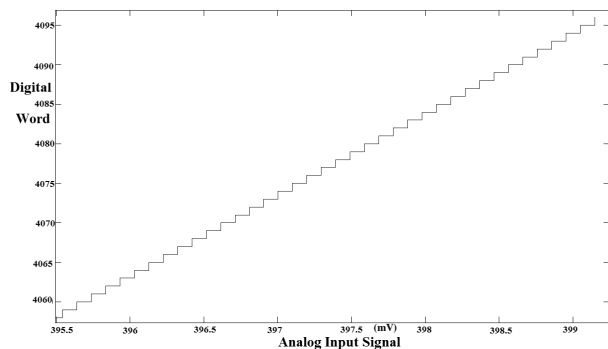


Fig. 7. Transfer characteristic.

VI. CONCLUSION

In this paper, a low power, low voltage ADC designed using 130 nm technology for biomedical signal acquisition is presented. The ADC operates well without the use of any offset reduction or noise reduction features normally employed in commercial ADC's like chopper or coherent sampling. With very high degree of configurability, the ADC is well suited for applications existing in the audio frequency region.

TABLE III
ADC SIMULATION RESULTS.

Modes 80MHz Clock	Mode1 13bits	Mode4 12bits	Mode6 11bits	Mode8 10bits
Integral Non Linearity (LSB) @200mV≤Vin≤1V	-2.51	-1.08	-0.99	-1.3
Differential Non Linearity (LSB) @200mV≤Vin≤1V	-0.089	-0.07	-0.076	-0.062
Effective No. of Bits @1kHz and 200mV≤Vin≤1V	10.64	10.22	9.28	7.98
SINAD @1kHz and 200mV≤Vin≤1V	66.1	62.04	55.78	48.1
SNR @1kHz and 200mV≤Vin≤1V	66.39	63.30	57.62	49.8
Integral Non Linearity (LSB) @300mV≤Vin≤900mV	-1.45	-0.98	-0.95	-1.25
Differential Non Linearity (LSB) @300mV≤Vin≤900mV	-0.069	-0.05	-0.055	-0.042
Effective No. of Bits @1kHz and 300mV≤Vin≤900mV	11.73	10.89	9.92	8.88
SINAD @1kHz and 300mV≤Vin≤900mV	72.84	67.75	61.8	55.5
SNR @1kHz and 300mV≤Vin≤900mV	73.45	68.30	62.13	55.93
Area (μm x μm)	300x349			
Power (mW) @80MHz Clock	4.83			

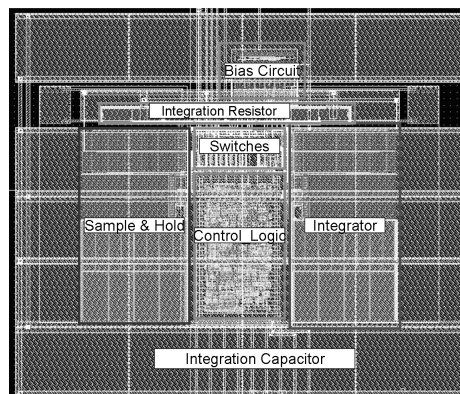


Fig. 8. ADC layout.

REFERENCES

- [1] R. J. Baker, "CMOS Circuit Design, Layout, and Simulation", John Wiley and Sons, 2005.
- [2] W. C. Goeke, "An 8-1/2 digit integrating analog to digital converter with 16 bit, 100kS/s performance", Hewlett Packard Journal, vol. 40, no. 2, pp. 8-14, Apr 1989.
- [3] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design", Oxford Press, 2002.
- [4] C.-T. Chiang, L.-L. Kao, and Y.-C. Huang, "A low-cost cmos integrated dual-mode dual-slope adc with synchronous rectification circuit for ac/dc signal measuring", Proc. IMTC 2008, May 2008.
- [5] P. R. Gray, "Analysis and Design of Analog Integrated Circuits", John Wiley and Sons, 2001.
- [6] http://www.maxim-ic.com/appnotes.cfm/appnote_number/2094/