

A Fifth-order Continuous-Time Sigma-Delta Modulator with 65-dB Dynamic Range and 2MHz Bandwidth

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Abstract—This paper presents a single-bit fifth-order continuous-time sigma-delta modulator for UMTS application. To relax the linearity requirement of the first integrator, a low-pass filter is inserted in the negative feedback loop after the summing node. To reduce power consumption, the loop-filter is implemented using a feed-forward topology. Measurement results show that it achieves 62dB SNDR with an over-sampling ratio of 32 over a 2MHz bandwidth. The power consumption is 8mW at a supply voltage of 2.5V in a 1-poly 5-metal 0.24 μ m CMOS technology.

Index Terms—Analog-to-digital converter, sigma-delta converter, continuous-time ADC, clock jitter, feed-forward topology.

I. INTRODUCTION

High-speed data communication requires analog-to-digital converters (ADCs) with increasing bandwidth and resolution in order to support higher data rates. For universal mobile telecommunication system (UMTS) applications, a 2MHz bandwidth is required^[1]. Fig.1 shows a UMTS low-IF receiver without analog channel filtering. Channel selection is performed in the digital domain to avoid the use of expensive discrete-component channel selection filters.

Typically, $\Sigma\Delta$ modulators with MHz bandwidths can be implemented using switched-capacitor circuit techniques^[2]. However, switched-capacitor sigma-delta modulators have a sampler at the input and therefore require anti-aliasing filters. They also tend to consume more power because of settling time requirements.

A continuous-time (CT) $\Sigma\Delta$ modulator has the advantages of intrinsic anti-alias filtering. This can relax the trade-off between the provision of prefiltering/AGC and the ADC dynamic range. Furthermore, it has the potential for lower power consumption and the capability to operate at higher sampling frequencies. Consequently, continuous-time $\Sigma\Delta$ modulators have become popular as ADCs for base

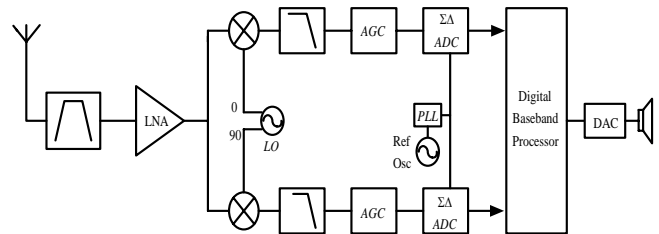


Figure.1 Block diagram of a UMTS receiver

band in a wireless transceiver. Several continuous-time $\Sigma\Delta$ modulators have been successfully implemented in AM/FM radio^[4], UMTS^[1] and GSM-EDGE/CDMA2000/UMTS applications.

In this work, a low-pass filter is added after the summing node in order to mitigate the linearity requirements imposed on the first integrator. A zero is introduced in the feedback path to compensate the resulting pole so that the transfer function remains unchanged. Non-return-to-zero (NRZ) feedback coding is employed because it is less sensitive to clock jitter than return-zero (RZ) coding. A measured dynamic range (DR) of 65dB was achieved in a 2-MHz bandwidth with a sampling clock frequency of 128MHz.

Section II of this paper describes the architectural level considerations for the $\Sigma\Delta$ modulator. Simulation result and physical layout considerations are presented in Section III, and Section IV concludes with the measurement results of the presented modulator.

II. ARCHITECTURE LEVEL CONSIDERATION

A. Modulator Architecture

The in-band quantization noise for the modulator is chosen lower than the circuit's thermal noise. To efficiently suppress the quantization noise at the edge of the signal band and thereby improve the signal-to-noise ratio (SNR), a fifth-order loop-filter is implemented with two complex poles (Fig.2). This introduces notches in the noise transfer function (NTF) of the modulator. Pole and zero positions are then optimized in order to minimum the quantization noise.

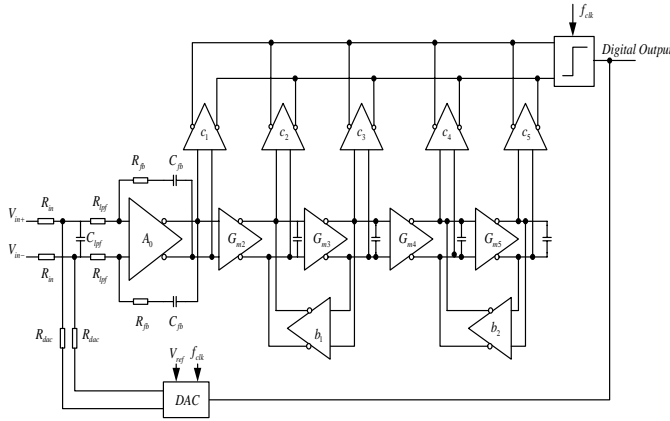


Figure.2 Fifth-order continuous-time $\Sigma\Delta$ modulator

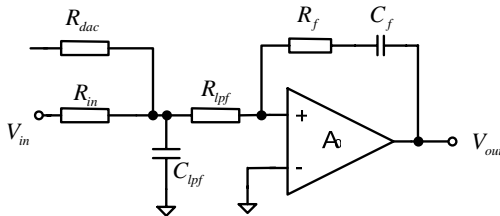


Figure.3 The first integrator with low-pass filter

The circuit noise is mainly contributed by thermal noise from the input resistor, the feedback DAC resistor and circuit noise from the first integrator. Other integrators, which have less critical design constrains, are implemented by Gm-C stages, and the filter coefficients are realized via transconductors.

For the first integrator, high gain at high frequency is beneficial for linearity at the cost of power consumption. However large DC power must be consumed to achieve high linearity. In order to mitigate the linearity requirements on the first integrator, a low-pass filter is added after the summing point, as shown in Fig.3 for a single-ended integrator.

Adding R_f introduces a zero to the feedback path of the first integrator to compensate for the extra pole. The output voltage is expressed as:

$$V_{out} = -\frac{1}{R_{lpf}} \frac{1}{R_{in} + R_1} \frac{R_1}{1 + sC_{lpf} \frac{R_1 R_{in}}{R_{in} + R_1}} \frac{sC_f R_f + 1}{sC_f} V_{in} \quad (1)$$

So by choosing R_f properly, the extra pole can be cancelled.

The loop-filter's coefficients are scaled to make the voltage and current of each gm stages realizable. For the $\Sigma\Delta$

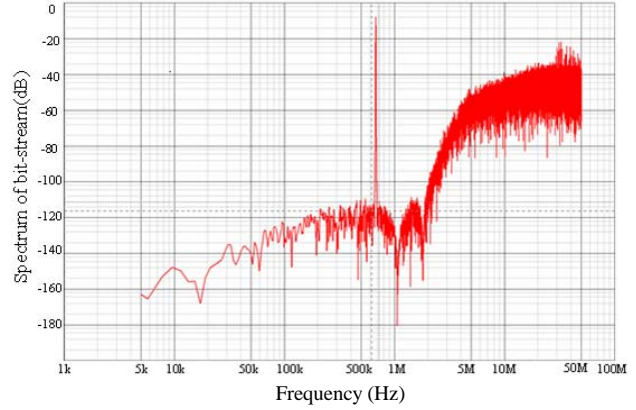


Figure.4 Spectrum of the output bit-stream with ideal blocks

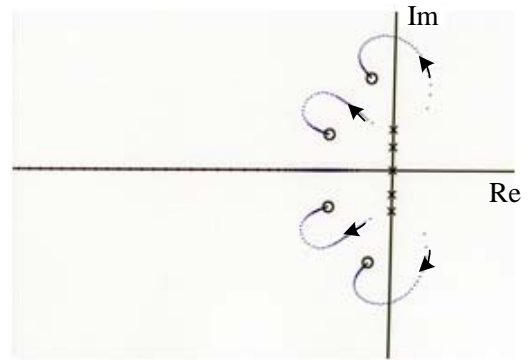


Figure.5 Root-locus of the closed loop system

modulator with ideal building blocks, a FFT spectrum of the output bitstream is shown in Fig. 4. Notches at 1MHz and 1.8MHz are clearly visible.

From the root-locus of the closed-loop system (see Fig.5), one can see that one pair of poles move into the right half plane at low loop gain, which causes instability. As the loop gain increases, the pole pairs all reside in the left half plane. Loop gain decreases when the output signal of the loop filter becomes too large causing the quantizer to overload with a consequent drop in gain.

The first integrator dominates the linearity of the system, because distortion from the following stages is decreased by the preceding integrator's gain. The first active-RC integrator, shown in Fig.2, has the best linearity and largest signal swings due to the feedback structure.

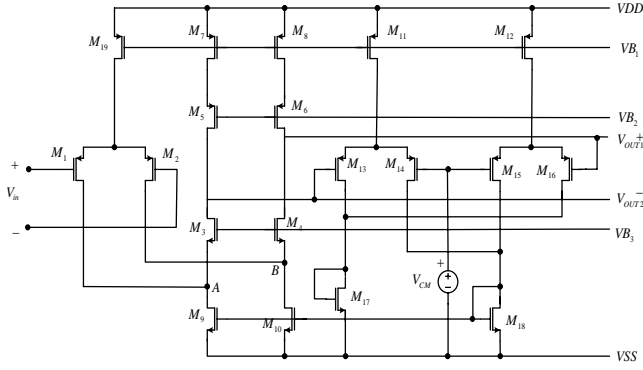


Figure. 6 First opamp schematic

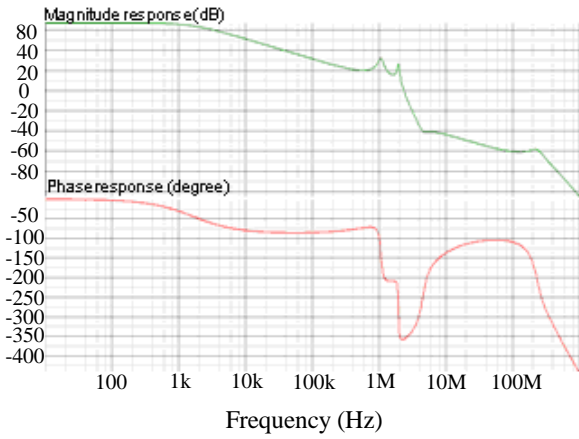


Figure. 7 Frequency response of the loop-filter

III. CIRCUIT DESIGN

In this section, circuit design, simulation results and layout consideration will be described.

A. Circuit implementation and Simulation results

The first integrator is an active-RC stage implemented with the opamp illustrated in Fig.6. The following stages are constructed using degenerated differential pairs. The loop-filter's frequency response is plotted in Fig.7. The resonators' finite quality factor and passive components spread cause the deviation in the notches positions. In order to counteract the effects of processing variation, the resonator frequency is placed $\sim 7\%$ higher than the optimum frequency.

The 1-bit quantizer is implemented with a continuous-time feedback DAC. A dynamic quantizer employing a cross-coupled latch structure saves power and achieves high speed.

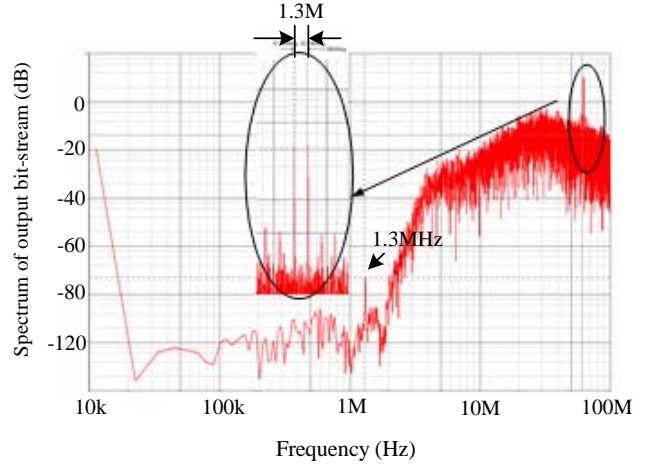


Figure. 8 Simulated FFT spectrum with DC input of 5mV

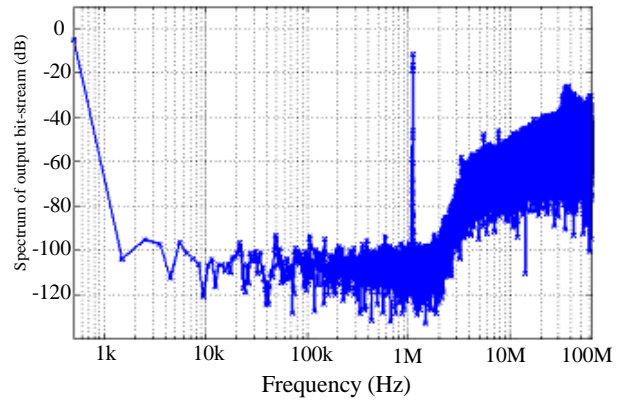


Figure. 9 FFT plot of the output bit-stream spectrum

B. Physical Layout

a) During the layout phase, attention was paid to noise at multiples of the sampling clock frequency to ensure that it does not interfere with input signals or the feedback DAC signals. The clock generator is placed as close to the DAC as possible in order to reduce parasitic coupling and modulation by harmonics at one-half of the sampling frequency.

b) In order to reduce excess-loop-delay, which is critical for the stability of the system, important nodes in the quantizer are connected using higher metal layers to reduce parasitic capacitance.

c) The fully differential signal paths are kept as symmetric as possible, especially for the first integrator. Offsets from the other integrators are reduced by the first integrator's gain. Offset and asymmetry introduces tones in

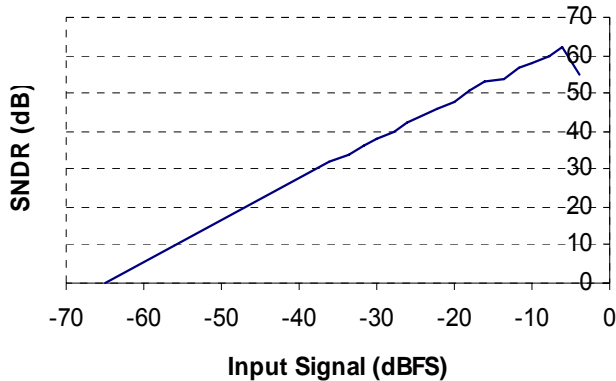


Figure.10 Measured SNDR as a function of input signal

the signal band for a DC input. For a DC input of 5mV, the tone is at 1.3MHz, and it is caused by the second-order harmonic of strong tones at one-half of the sampling frequency of 64MHz, as shown in Fig. 8. The following figure of merit (FOM) is used to benchmark the performance of the ADC.

$$\text{Figure of Merit} = \frac{\text{Power}}{2f_{BW} \cdot 2^{ENOB}} \quad (2)$$

In Equation (2), the linearity is expressed as the effective number of bits ($ENOB$). f_{BW} is the bandwidth of the ADC. A comparison with start-of-the-art continuous-time $\Sigma\Delta$ modulators is shown in Table.1. We can see that this work achieves comparable performance with start-of-the-art.

IV. EXPERIMENTAL RESULT

The 1.25 mm² prototype chip was fabricated in a 1-poly 5-metal 0.24 μ m CMOS Technology. Fig.9 shows the measured SNDR of the output bit-stream spectrum. In Fig.10, the modulator's SNDR is plotted as a function of the input signal, peak SNDR is 62dB. The full scale (FS) input is 0.62V_{rms} and it achieves a DR of 65dB over 2MHz bandwidth.

V. CONCLUSION

A fifth-order continuous-time $\Sigma\Delta$ modulator is presented in this paper. The loop-filter employs feed-forward topology and a low-pass filter is added after the summing point to relax the linearity requirements for the first integrator. It achieves a DR of 65dB over a 2MHz bandwidth.

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Table.1 Figure of merit comparison with state-of-the-art

Reference	Bre ^[7]	Zw ^[4]	Pa ^[6]	This work
Sampling (Hz)	13M	10.7M	300M	128M
Bandwidth (Hz)	100k	300k	15M	2M
OSR	65	15	10	32
SNR/SNDR	82dB	79dB	63.7dB	62dB
Loopfilter	4 th - order single loop	5 th - order single loop	4 th - order single loop	5 th - order single loop
Quantizer	1 bit	1 bit	4 bit	1 bit
DAC	1bit RZ	1bit RZ	4bitRZ	1 bit NRZ
Power	1.8mW	8mW	70mW	8mW
Technology (um)	0.35 CMOS	0.25 CMOS	0.13 CMOS	0.24 CMOS
<i>FOM</i>	1.098p	1.62p	2.28p	1.38p

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