

A 0.8-2.5GHz Wideband CMOS LNA with ESD Protection for Multimode Receivers

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Abstract—A fully integrated 0.8-2.5GHz low-power ESD-protected low noise amplifier (LNA), designed in 90-nm CMOS technology is presented. This 5.7mW LNA features a 18dB voltage gain across the band with a noise figure smaller than 1.7dB. The input return loss is below -10dB from 600MHz to 2.5GHz. A resistive feedback current reuse common source input stage together with the ESD-protection circuit and the bondwire parasitics achieves wideband input impedance matching without employing large on-chip or off-chip inductors. The ESD-protection circuit is co-designed as part of the LNA input matching network to achieve 3kV HBM at the RF input pin without sacrificing the LNA RF performance. The input nMOS and pMOS transistor are sized to achieve 1.7dB NF within 4mA bias current from 1V supply voltage. The output stage realizes the single-to-differential conversion and provides 250 Ω single-ended output impedance required by the following mixer stage. The simulated maximum gain mismatch and phase mismatch between the differential outputs across the band are 0.5dB and 3 $^\circ$, respectively.

Index Terms— multi-mode, multi-band, fully integration, low-power, low noise amplifier, ESD, radio frequency.

I. INTRODUCTION

Recent developments in wireless communication have resulted in many widely adopted wireless standards, with each catering to different needs depending on their data rates, operating range, bandwidth requirement and carrier frequency. Therefore, the trend of the future wireless transceiver design is an integrated circuit that can work across multiple standards, be configurable and reuse maximum number of building blocks within the minimum power consumption and chip area.

One of the key building blocks for multi-band transceiver is the low noise amplifier (LNA). There are three ways to implement a multi-band LNA. The simplest way is to use a separate narrow band LNA for each standard, resulting in larger die area, higher cost and power [1]. The second alternative is to design a switching band LNA, e.g., adopting a switched inductor [2] either at input stage or at load, which are more compact and use less power, but still occupy a larger chip area due to the additional inductors and forbid the concurrent operation of various standards. It is desirable to provide true multi-band transceiver where various wireless standards can operate simultaneously to extend its functionalities [3]. The third way to implement the multi-band LNA can solve this problem, i.e., a wideband LNA, which can operate across

multi-band with sufficient performance for each standard.

In this way, the LNA is more compact and flexible, shared by multi-band. Notch filter can be further added in the LNA to reject the out of band blockers. In this paper, the idea of wideband LNA is adopted. The list of standards for the multi-band LNA in this work is shown in Table I.

Table 1 Frequency Bands

Wireless Standard	Frequency Spectrum (MHz)
GSM	935 – 960, 1805-1880
UMTS	850/900/1700/1900/2100
DCS-1800	1805 -1880
DECT	1880 -1900
PCS-1900	1930 - 1990
WCDMA	2110 - 2170
WLAN (802.11b/g)	2400 - 2483
Bluetooth (802.11FH)	2400 - 2483

With the decrease of the gate oxide thickness, CMOS circuits become more sensitive to stress from electrostatic discharge (ESD). The LNA is one of the most critical building blocks in RF front-end and is usually connected to the outside world through antenna or an off-chip antenna filter and therefore can be exposed to ESD events. Incorporating sufficient level of on-chip ESD protection on a given circuit requires that the added ESD protection does not degrade the performance parameters of the circuit. Consequently, simultaneously achieving the RF performance and ESD robustness in state-of-the-art CMOS technologies is highly challenging. RF-ESD co-design method, which includes the ESD-protection circuit into the LNA design space, is employed in this work. The parasitics of the ESD-protection circuits are absorbed as a part of the LNA input matching networks. In this way, the NF and the gain of the LNA are seldom altered by the ESD-protection circuit. Meanwhile, the required on-chip inductor value for input impedance matching is reduced to only 1nH, facilitating the fully integration.

The paper is structured as follows. A brief review of wideband LNA design consideration and the state-of-the-art wideband LNA topologies are analyzed in Section II. Then the proposed wideband LNA architecture, circuit design aspects, and ESD-protection are discussed in Section II. Section III describes the LNA simulation results with ESD-protection. The

conclusion is given in Section IV.

II. STATE-OF-THE-ART WIDEBAND LNA TOPOLOGY

The wideband input impedance matching and the low NF across the band are two design challenges for wideband LNA input stage. Besides, the flat in-band gain is also very important in some applications. In this work, for multi-band operation, the flat gain is not critical, and therefore, only the input topology of the wideband LNA is addressed here.

The conventional cascode LNA with inductive source degeneration is one of the most popular LNA topologies used in narrow band LNA design in each of the band listed in Table 1 due to its merits of low NF, high gain, and high reverse isolation. By sizing the input common-source (CS) transistor and biasing current, the simultaneous noise matching and input impedance matching can be achieved theoretically. However, in order to cover multi-band across 800MHz-2.5GHz, the required quality factors (Q) of the degeneration inductor and the base inductor are too small to maintain the high gain and low noise performance of the narrow band LNA. Moreover, the inductor required for impedance matching at this frequency band is up to tens of nH [4] to resonate the capacitive part of the LNA input stage around 1GHz. Off-chip inductor is usually unavoidable to achieve impedance matching at 1GHz in modern CMOS technology.

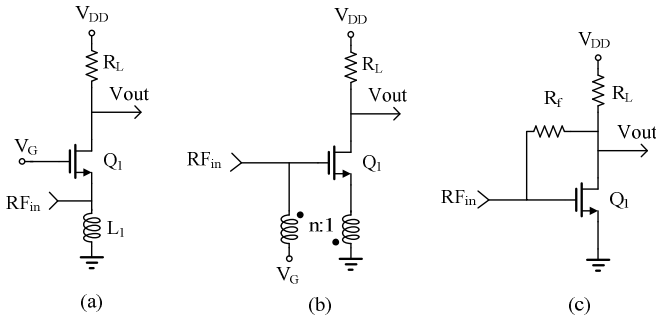


Fig.1 Wideband LNA topologies

As an alternative, common-gate LNA [5], resistive feedback [6], and reactive feedback [7] topologies are reported to provide wideband operation. The simplified schematics of them are shown in Fig.1.

The common-gate (CG) LNA facilitate the wideband input impedance matching determined by $1/g_m$. However, the gain and the NF performance of the CG stage are both worse than its common-source (CS) counterpart, especially its NF is constrained to about 3dB in modern CMOS technology [5]. Although some capacitive feedback CG topology is reported to improve the NF, the minimum reported NF of the CG topology is still around 3dB, which is too large to satisfy the GSM specification [8].

The reactive feedback LNA in Fig.1 (b) achieves the lowest reported NF (2dB) in 3.1-10.6GHz band [7]. However, to implement the required transformer in this topology on-chip is still impossible in the 0.8-2.5GHz band in modern CMOS technology, which limits this topology to the circuit operating above 3GHz.

The resistive shunt feedback, shown in Fig.1(c) can achieve wideband input impedance on the first order approximation, which roughly equals to the feedback resistance divided by the voltage gain of the input stage without feedback. However, the feedback resistor will add additional thermal noise to the LNA and easily raise the NF to above 3dB [9]. To reduce its contribution to NF, the value of the resistor should be as large as possible. Consequently, the gain of the CS stage should increase to maintain the equivalent input impedance around 50Ω , leading to high power consumption. An improved version of the resistive shunt feedback wideband LNA is proposed in the next section which adopts the current reuse technique to increase the voltage gain, lower the NF to 1.6dB, while consuming only 4mA biasing current at the input stage.

III. LNA CIRCUIT DESIGN

The schematic of the proposed wideband LNA is shown in Fig.2. The input stage is an nMOS-pMOS co-current CS configuration. pMOS devices are not favored in the RF circuit design due to its lower characteristic frequency (f_T) and larger parasitics compared to nMOS device of the same dimension. However, in the proposed wideband LNA operating at 0.8-2.5GHz, the speed of the pMOS transistor in the 90-nm CMOS technology is sufficient. The large parasitic capacitance of the pMOS is desired here since it can be absorbed into the input matching network and reduces the required on-chip source degenerative inductance to only 1nH and the base inductor to 3nH, which can be realized by bondwire. Moreover, the pMOS CS stage is sized to provide the same transconductance as the single nMOS CS stage and results in a doubled transconductance at the output of the input stage without increasing any bias current. Therefore, the open loop gain of the LNA is doubled and the resistor in the feedback path (R_f) can be doubled ($1k\Omega$ in this case) to reduce its contribution to the LNA NF. The design detail of the input stage, ESD co-design, and the output stage single-to-differential conversion are described as follows.

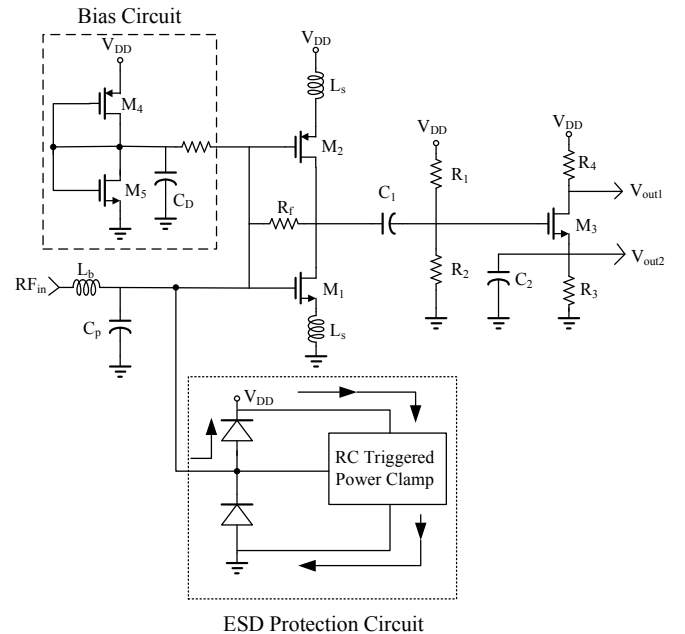


Fig.2 ESD protected wideband LNA

A. Input stage with ESD co-design

Since the LNA input pin connects to the gate of the amplifying nMOS and pMOS transistors, it is extremely sensitive to ESD. The input of the LNA is facing two types of signals. The RF signal should be maximally absorbed by the amplifying device, whereas the hazardous ESD-signal which should be kept away from the amplifying device. A separation of these two signals needs to be performed.

In this work, a dual diode network on input pin and RC-triggered silicided power clamp consist of the protection network (dotted box in Fig.2) to provide the proper discharge paths for all the potential discharge modes – where the current will enter and leave the circuit with both possible polarities of the discharge. The P+/NW is designed as 300 μ m perimeter and the N+/SX diodes 200 μ m perimeter to carry the current as high as 2A (i.e., 2kV HBM) [10]. The 100fF parasitic capacitance originated from the diodes network can be absorbed in the input impedance matching network. The on-resistance of the two diodes is only several ohms to provide fast discharge path.

To achieve the 1.6dB NF at 1GHz, the length of the input transistor is chosen as 0.25 μ m instead of the minimum length 0.1 μ m in 90-nm CMOS technology in order to reduce the contribution of the 1/f noise. The input nMOS and pMOS are sized as 125 μ m/0.25 μ m and 250 μ m/0.25 μ m with a 4mA bias current respectively as a result of the tradeoff between the power consumption, gain, NF, and on-chip inductance needed for impedance matching. The 1k Ω feedback resistor is added to achieve the wideband impedance matching across the band. The relation of the R_f and the S_{11} is shown in smith chart in Fig.3. The inductor L_b (about 3nH) is added to resonate the capacitive part of the input impedance and can be implemented by the bondwire. The 100fF parasitic capacitance coming from the bondpad is also included in the simulation. Transistor M4 and M5 provides the proper bias voltage for the input transistors. The shunt resistive negative feedback topology is also good for linearity and the stability of the LNA.

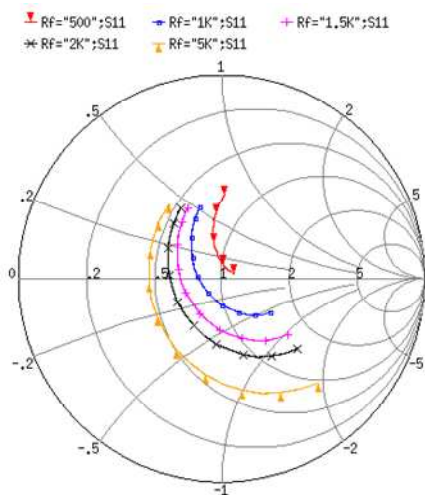


Fig.3 LNA S_{11} vs. R_f

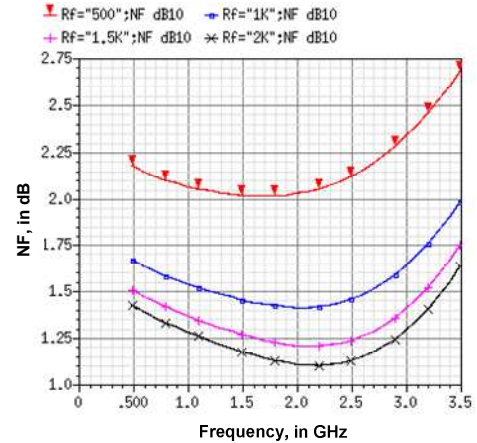


Fig.4 LNA NF vs. R_f

B. Output stage design

The input RF voltage is amplified by the input stage with a transconductance gain equals to the sum of the transconductance of the two input MOS transistors. The amplified RF current signal establishes a RF voltage on the gate of M3 (in Fig.2) through resistor R1 and R2 which are used as the load of the input stage and meanwhile provide the proper bias voltage for M3. The single ended input voltage is converted to the differential output voltage and send to the following mixer stage from the drain and source of M3 respectively. The capacitor C2 (110fF) is added to reduce the maximum phase error between the two differential outputs within 3 $^\circ$ across the whole band. The load resistors R3 and R4 are 250 Ω , providing about 16dB single ended voltage gain and the proper output impedance for the mixer stage. The bias current of the second stage is 1.5 mA as a tradeoff between the LNA gain and the linearity.

IV. SIMULATION RESULTS

The proposed LNA circuit is designed in IBM 90-nm CMOS technology and the key simulation results are illustrated here. The relation of the feedback resistor R_f with the LNA NF and input matching is shown in Fig.3 and Fig.4. It can be seen that good input matching in the concerned frequency band prefer a small R_f , whereas the low NF requires a big R_f . The 1k Ω is finally used as a tradeoff.

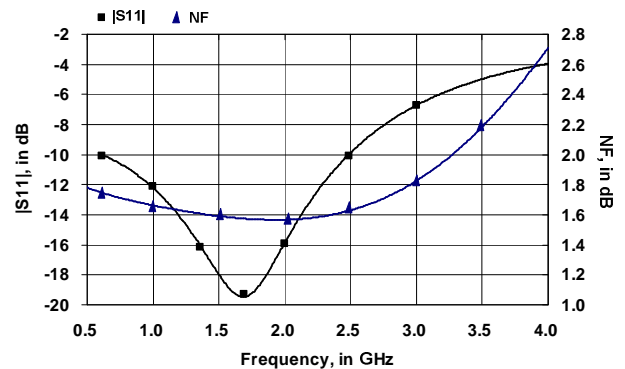


Fig.5 LNA $|S_{11}|$ and NF

The resulted LNA S11 is below -10dB from 0.6MHz-2.5GHz, shown in Fig.5 and the NF is below 1.7dB across the band with a minimum value of 1.55dB at 2GHz (see Fig.5).

The voltage gain at the differential outputs are show in Fig.6, in which the maximum gain difference is 0.5dB. The phase difference between the differential outputs is shown in Fig.7, with 3° maximum phase error.

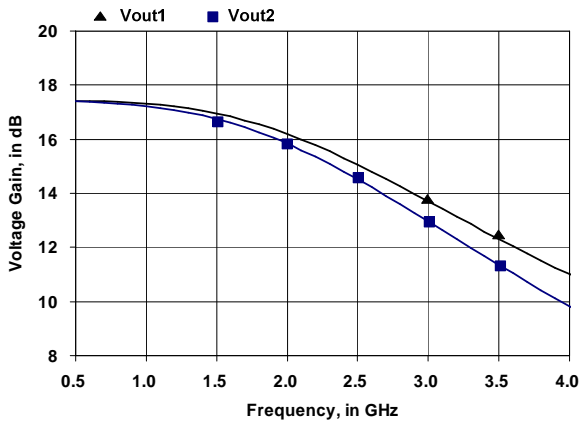


Fig.6 Voltage gain of the differential outputs

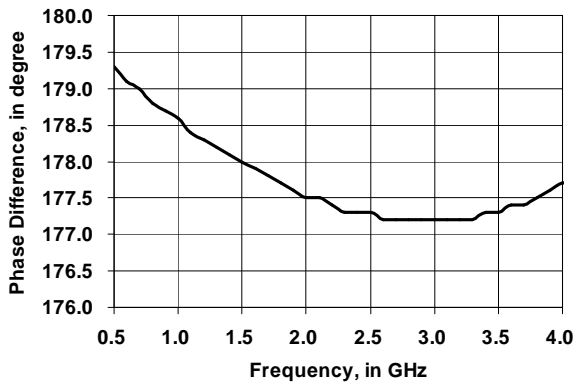


Fig.7 Phase difference between the differential outputs

The IIP3 curve is plot in Fig.8 and the input referred IP3 is about -10dBm at 1GHz. The LNA is unconditional stable in the whole frequency band and the reverse isolation is below -40dB across the band.

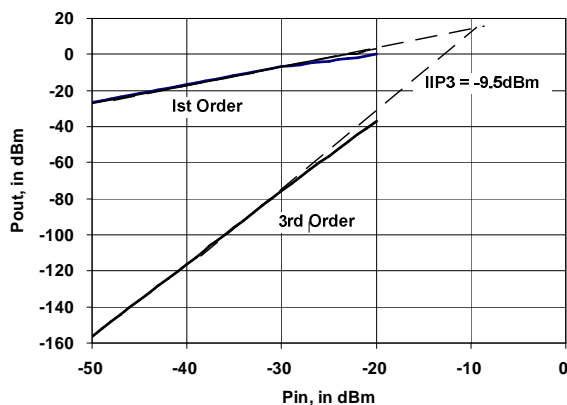


Fig.8 LNA IIP3 curve @1GHz and 1.02GHz two-tone inputs

V. CONCLUSION

A fully integrated 5.7mW wideband LNA in 90-nm CMOS technology is proposed. The nMOS-pMOS current reuse topology together with the resistive shunt feedback reduces the number and the size of the on-chip inductor needed for wideband impedance matching. The ESD protection circuit is co-designed with the LNA and its parasitic is used as part of the impedance matching network. The parasitics of the bondwire and the bondpad are absorbed in the input impedance matching to make the whole design compact and robust. The simulated NF is below 1.7dB across the band and the voltage gain of each differential output is about 16dB. The output stage achieves single-to-differential conversion and provides the interface for the following mixer stage. The whole LNA only draws 5.7mA from a 1V power supply.

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