

2D Simulation of Hot-Carrier-Induced Degradation and Reliability Analysis for Single Grain Si TFTs

J. Tan, A. Baiano, R. Ishihara and K. Beenakker

Abstract—The reliability performance of Single-Grain (SG) Silicon (Si) Thin Film Transistor (TFT) is reported based on the device simulation. We present a model validation through a certain fit methodology with trap profiles in the band gap under a linear region bias stress condition ($V_{DS} < V_{GS} - V_T$). An accurate physical degradation model is implemented to reflect the trap formation and hot-carrier degradation mechanism under the bias stress condition. The device degradation model parameters can be extracted through measurements and the inverse modeling approach. In the inverse modeling approach, the data that describe the device performance (such as transfer characteristics) are used as the input of the 2D device simulator (Sentaurus TCAD) and model parameters used in the simulation are extracted and regarded as the output. When the device simulation results show a good fit with the measurement result before and after stress, the device degradation model is accurately determined and can be used to predict the device reliability performance.

Index Terms—SG Si TFTs, reliability performance, degradation model, hot carriers

I. INTRODUCTION

SINGLE grain Si TFTs are fabricated making use of a two-dimension (2D) location-controlled single grain to cover the active region of TFT device, which gives fewer in-grain and grain boundary defects compared with Polycrystalline-Si TFTs and Amorphous-Si TFTs[1][2][3][4]. Hence, SG Si TFTs have a high carrier mobility of about $600 \text{ cm}^2/\text{VS}$, a low drain leakage current of $9\text{e-}14\text{A}$ and a low subthreshold swing (S) of about 0.2 V/decade . However, the reliability performance of SG Si TFTs is becoming a great challenge for the device stability when applied to digital and analog circuits. Hot-carrier effect is an important issue for SG Si TFTs reliability, inducing interface trap generation, oxide layer charge injection, etc. As a result, the device characteristics

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show the mobility reduction, threshold voltage shift, subthreshold swing variation and increasing leakage current[5][6][7]. An accurate physical degradation model is needed to present the device degradation mechanism under the bias stress condition and hot-carrier effect, which can be used to predict the device time-dependence reliability performance as well. In this paper, a certain trap profile in the band gap is used to implement a good fit between measurement results and simulations of device characteristics. Based on that trap profile, parameters of a time-dependence degradation model are extracted in the simulator and the device reliability prediction is also presented.

II. RESULTS AND DISCUSSION

A 2D physical model of SG Si TFTs is established in the simulator to analyze the time-dependence hot-carrier degradation under a high field stress based on the interface trap physics and hot-carrier degradation mechanism described in [8]. The device reliability performance is presented through the transient simulation with accurate degradation model parameters.

A. Device Structure Implementation

The simulator of Sentaurus TCAD is used to perform the 2D device simulation.

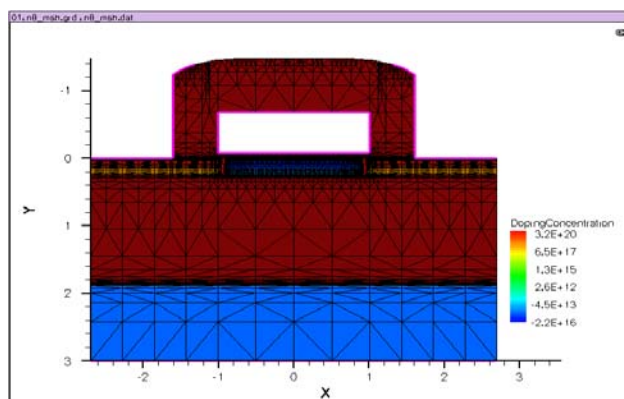


Fig.1. SG Si TFT device created by Sentaurus Structure Editor with doping concentration and its mesh profile generated by Sentaurus Mesh

Process steps of SG Si TFTs can be translated into the syntaxes and can be programmed in Sentaurus Process. After that, the device structure is meshed by Sentaurus Mesh

simulator. The quality of mesh is closely related to the numerical analysis in the following Sentaurus Device because the physics model and equations are solved based on a mesh unit[9]. Fig.1 shows the schematic view of a SG Si TFT device structure. The geometrical parameters of SG Si TFTs used in our study are as follows, the channel length $2\mu\text{m}$, the channel width $2\mu\text{m}$ and gate oxide thickness 80nm . The device characteristic simulation is performed on the device structure through the modification of physics specifications, which will be discussed below.

B. Trap Effect on Device Characteristics

Under high bias stress voltage, hot-carriers are generated from the strong impact ionization near the drain junction and the active region in SG Si TFTs, which corresponds to the high electric field as well. The trap generation and hot-carrier injections are originated from the hot-carrier effect. Acceptor-like traps are neutral when unoccupied and negative when one electron occupies, which are mainly located in the upper half of the band gap. Donor-like traps are positive when unoccupied and neutral when occupied, which are mostly located in the lower half of the band gap[8]. Due to the different function of acceptor-like traps and donor-like traps, they have different effect on the device characteristic degradation[10].

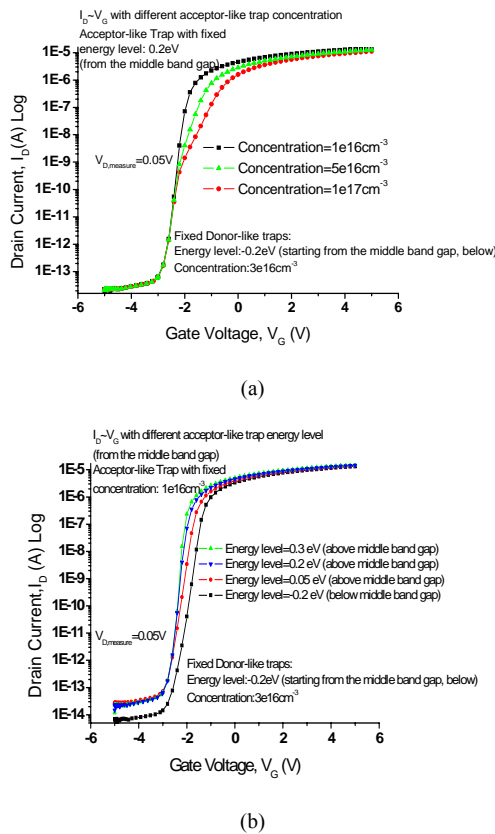


Fig.2. I_D - V_G characteristics changing with different acceptor-like trap concentration (a) and trap energy level (b), the donor-like trap has a fixed concentration and energy level

From Fig. 2(a), it can be indicated that with the growth of trap concentration at a certain energy level in the band gap, the on-current is reduced gradually and the threshold voltage

shifts due to the obvious on-current reduction. However, the drain leakage current has no variation with the concentration increase. It can be concluded that with the increase of acceptor-like trap generation in the upper half of the band gap at a certain energy level, the on-current will be reduced due to the electron capturing in the n-channel device[6][11]. While from Fig. 2(b), it can be seen that when the trap energy level goes down and comes towards the middle of the band gap or even below, the on-current shows a relatively small reduction while the subthreshold swing shifts obviously. The threshold voltage variation at different energy levels is the result of the subthreshold swing shift. The leakage current still keeps the same until the energy level goes below the mid-band gap and then it decreases. From the above analysis, the acceptor-like trap generation near the middle of the band gap will give an effect on the subthreshold swing shift and small on-current reduction. When the energy level is below the middle of the band gap, the acceptor-like trap makes the whole characteristic go down.

The similar simulation is also performed to evaluate the effect of donor-like traps on the device characteristic for n-channel device.

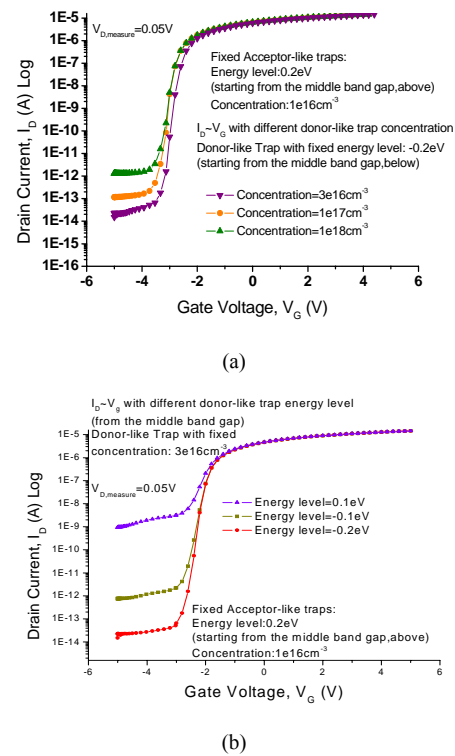


Fig.3. I_D - V_G characteristics changing with different donor-like trap concentration (a) and trap energy level (b), the acceptor-like trap has a fixed concentration and energy level

Fig. 3(a) shows that the leakage current goes up with the increase of trap concentration and in this case the donor-like trap energy level is fixed at -0.2eV (below the middle of the band gap). It is because more donor-like traps in the lower half of the band gap give higher generation possibilities so that the leakage current rises. However, the subthreshold swing does not alter with the increase. It presents in Fig. 3(b) that the leakage current also increases when the donor-like

trap energy level moves towards and above the middle of the band gap, which rises from -0.2eV to 0.1eV (above the mid-band gap). When the donor-like trap energy level moves towards the middle of the band gap, it has a stronger trend to be a recombination-generation center so that it helps electrons jump to the conduction band and increases the leakage current. However, in Fig. 3(a) and Fig. 3(b), there is no clear variation for on-current and threshold voltage, which are mainly determined by acceptor-like traps in the upper half of the band gap. Therefore, donor-like traps in the lower half of the band gap do not give much influence on the variation of on-current [8].

C. Device Model Validation and Fit Methodology

According to the previous trap effect analysis, the on-current, leakage current and subthreshold swing in $I_D \sim V_G$ characteristic can be modified through the variation of trap concentration and energy level of acceptor-like and donor-like traps. Hence, device performance degradation due to hot-carrier effect under a high bias stress can be simulated by putting some addition trap profiles in the band gap in the simulator.

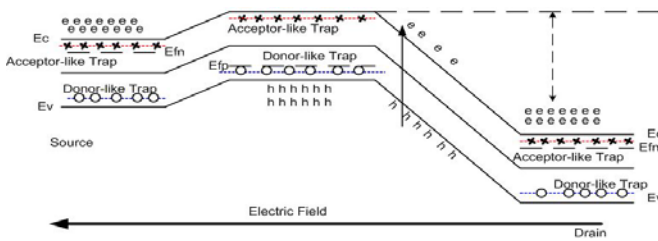


Fig. 4. Cross section of acceptor-like and donor-like traps in the band diagram

Fig. 4 shows the cross section of a band diagram with acceptor-like and donor-like traps. At on-state, the transfer characteristic ($I_D \sim V_G$) can be modified by acceptor-like traps through carrier capturing, while at off-state donor-like traps serve as recombination-generation centers and they help the electron excitation to the conduction band and hole generation in the valance band, which can be contributed to the leakage current in the $I_D \sim V_G$ characteristic. The subthreshold swing in the device characteristic varies with the trap profile near the middle of the band gap.

Furthermore, the threshold voltage can be related to charges in the gate oxide, which means that the modification of fixed charge concentration in the gate oxide can be used to vary the threshold voltage. In the meanwhile, it can also bring a small variation to the drain current in the $I_D \sim V_G$ characteristic.

Based on previous sections, it should be feasible that acceptor-like and donor-like traps with level distributions are put into the band gap in order to modify the $I_D \sim V_G$ characteristic in the simulator as for SG Si TFTs.

The initial $I_D \sim V_G$ characteristic for n-channel SG Si TFT was measured over the gate voltage range from -7V to 3V with the drain measurement voltage of 0.05V . In the simulator, several acceptor-like and donor-like traps with different concentration and energy level distribution is added and adjusted in the band gap to modify the device characteristics in order to achieve a good fit between the measurement and simulation results.

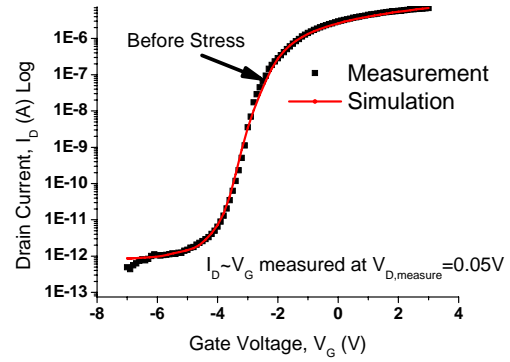


Fig. 5. Fitting between the 2D physical model and measurement result of the transfer characteristic ($I_D \sim V_G$) measured at $V_{\text{Drain}} = 0.05\text{V}$ before stress

It can be seen from Fig. 5 that the physical model in the simulator with a certain profile of trap specifications in the band gap gives a good fit with the measurement result of $I_D \sim V_G$ characteristic at $V_{\text{Drain}} = 0.05\text{V}$, which in the meanwhile means the implementation of SG Si TFT model validation in the simulator as well.

TABLE I
ACCEPTOR-LIKE AND DONOR-LIKE TRAP PROFILE FOR $I_D \sim V_G$ CHARACTERISTIC BEFORE STRESS IN SIMULATOR TO FIT WITH THE MEASUREMENT RESULT

	trap energy level (eV) (from the middle band gap)	trap concentration (cm^{-3}) (specified in bulk region)
Acceptor-like traps	0.455	$2\text{e}18$
	0.25	$8.1\text{e}16$
	0.01	$2\text{e}16$
Donor-like Traps	-0.1	$1\text{e}11$
	-0.01	$9\text{e}15$
	-0.2	$3.6\text{e}16$
Fixed charges in Gate Oxide	$2.75\text{e}17\text{ cm}^{-3}$	

Positive value means above the middle of the band gap
Negative value means below the middle of the band gap

Table I shows the parameters of trap concentration and energy level in the physics section of the simulator which are used to implement the model validation and achieve a fit between the model and measurement.

D. Hot-Carrier Degradation and Reliability Prediction

Since the physical model for the $I_D \sim V_G$ characteristic before stress is implemented, it is expected that with the combination of degradation model parameters this model can accurately simulate the time-dependence degradation performance of $I_D \sim V_G$ characteristic under a linear region bias stress condition ($V_{\text{DS}} < V_{\text{GS}} - V_{\text{T}}$).

The initial $I_D \sim V_G$ characteristic shown in the previous section is applied with a linear region stress condition as follows, gate voltage of 8V and drain voltage of 1V ($V_{\text{Gate}}=8\text{V}$ and $V_{\text{Drain}}=1\text{V}$). Under the bias stress, due to the high electric field and hot-carrier effect, there is some interface trap generation, which gives an obvious shift of subthreshold swing. The degradation model should reflect the practical trap generation in the real device. In order to determine the degradation model parameters accurately to simulate the time-dependence performance under the stress condition, the inverse modeling approach is applied in this section where the device transfer characteristic under the stress for 300sec is used as the input of the 2D device simulator and model parameters used to simulate the measurement characteristic after stress are regarded as the output and parameter extraction.

In the degradation model, the parameters are modified to present the trap generation increase in the band gap with the transient simulation in Sentaurus[7][12][13]. Accurate physical degradation model parameters can be extracted if there is a good fit between the measurement and simulation results of $I_D \sim V_G$ under the stress condition of $V_{\text{Gate}}=8\text{V}$ and $V_{\text{Drain}}=1\text{V}$ for 300sec.

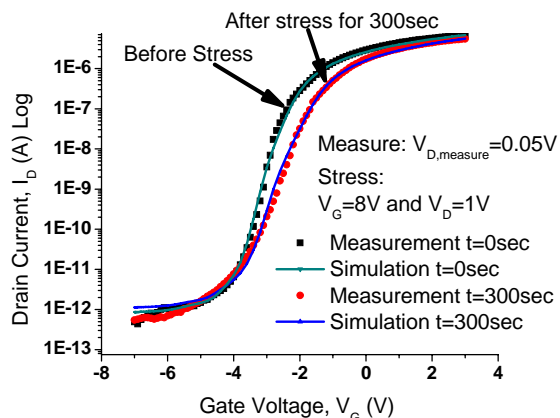


Fig. 6. Fitting between the 2D physical model and measurement result of the transfer characteristic with $V_{\text{Drain}} = 0.05\text{V}$ before and after stress under $V_{\text{Gate}} = 8\text{V}$ and $V_{\text{Drain}} = 1\text{V}$ for 300 sec

It can be indicated in Fig. 6 that there is a good fit between the measurement and simulation results of $I_D \sim V_G$ under the stress condition of $V_{\text{Gate}}=8\text{V}$ and $V_{\text{Drain}}=1\text{V}$ for 300sec, which means the degradation model parameters have been accurately determined and extracted through the inverse modeling approach.

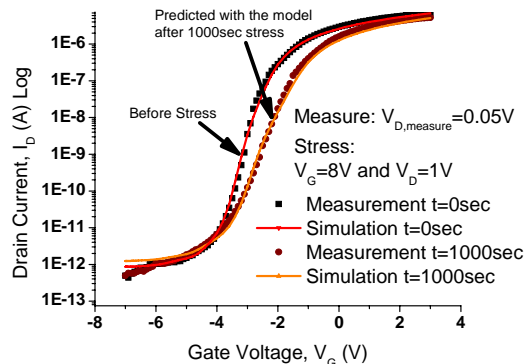


Fig. 7. Device transfer characteristic under the stress condition of $V_{\text{Gate}} = 8\text{V}$ and $V_{\text{Drain}} = 1\text{V}$ for 1000sec can be predicted by the degradation model and show a good fit with the measurement

As soon as the model validation and degradation model parameter extraction are implemented, the reliability performance for the n-channel SG Si TFTs can be predicted under a certain bias stress condition with transient simulation. With this physical degradation model, the measurement result under the stress condition of $V_{\text{Gate}}=8\text{V}$ and $V_{\text{Drain}}=1\text{V}$ for 1000sec can be predicted. Fig. 7 shows a good fit between simulation and measurement after 1000sec stress with the model determined previously, which proves the feasibility of reliability prediction for SG Si TFTs with the 2D physical degradation model. In the meanwhile, the trap generation near the middle band gap in the model is modified in order to simulate the measurement result, which also further confirms that under the linear region stress condition of $V_{\text{Gate}}=8\text{V}$ and $V_{\text{Drain}}=1\text{V}$, many interface traps are generated in the middle of the band gap due to the hot-carrier effect. Therefore, the physical degradation model could give more insights into the device degradation mechanism for reliability use.

III. CONCLUSION

This paper provides an overview of the reliability performance of n-channel SG Si TFTs under a certain stress condition with a 2D physical degradation model in the simulator. The effect of acceptor-like and donor-like traps with different distributions of energy levels and concentration on the $I_D \sim V_G$ characteristic is analyzed. A model validation is implemented through some additional trap profile in the band gap. Accurate model parameters are determined through a good fit between the physical model and measurements. The device reliability performance can be predicted as soon as the degradation model is implemented and in the meanwhile it can give an insight into the device degradation mechanism under the bias stress through the model parameter modification.

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