

Influence of Through-Substrate Vias on Electrical Performance of Bipolar Transistors

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Abstract – In this paper, the influence of laser ablated through-wafer via-holes on bipolar transistors in their vicinity is analyzed. The targeted application is a wafer-level packaged, SMT-compatible vertical power transistor. It requires low density through-wafer interconnect with via diameter in the range of 50-100 μm to be fabricated in silicon substrates with thickness of less than 250 μm . The effect of laser ablation was studied by comparing gummel-plots of n-p-n bipolar transistors before and after via fabrication. Results indicate that the electrically affected zone does not exceed 10-20 μm around the via edge.

Keywords – through-substrate via; silicon substrate; laser ablation; electrically-affected zone.

I. INTRODUCTION

Application of through-wafer vertical interconnects for IC packaging may satisfy the needs of modern wireless communication products, which require more compact packaging solutions and efficient utilization of a footprint area, also referred to as ‘silicon efficiency’ [2]. The through-wafer vertical interconnect provides smaller interconnect lengths resulting in lower parasitics and smaller propagation delays and is therefore highly attractive in RF packaging. Figure 1 shows, as an example, application where through-wafer interconnect in a silicon substrate is utilized to demonstrate a wafer-level packaged, SMT-compatible power transistor developed in the frame of EU project Blue Whale [2].

The key technology for through-wafer vertical interconnects is fabrication of through-wafer vias. Among the number of potential techniques for fabrication of through-wafer via-holes deep reactive ion etching (DRIE) and laser ablation offers incontestable advantages in terms of achievable via diameters, pattern transfer accuracy and mechanical reliability. It has been shown [3] that, next to the DRIE technique, the laser ablation technique is favoured technique in terms of minimal achievable dimensions, influence on wafer mechanical strength, and potential throughput. The laser

ablation process is capable of fabrication of vias down to 20 μm in 240 μm thick substrates. Other advantages of laser ablation are the maskless processing, high flexibility as it is independent on the to-be-processed material.

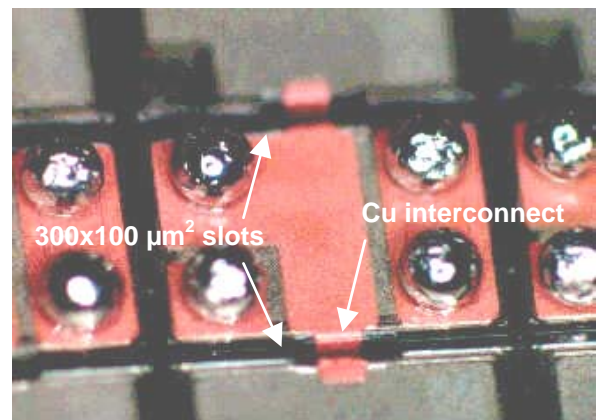


Figure 1: Part of a wafer front side showing an SMT-compatible WLCSP power transistor where through-wafer slots (300x100 μm^2) are used to realize a front-to-backside electrical interconnect.

However, the fabrication of the vias can lead to possible damage introduced to the substrate (e.g. cracks, thermal damage of the silicon around the via, etc.), which can have strong influence not only on the mechanical stability of the silicon wafer but also on the electrical performance of active devices.

II. EXPERIMENT DESCRIPTION

To investigate the effects of laser ablation on active circuitry, vias in different distances to a vertical n-p-n bipolar transistor were fabricated. For the via-fabrication a tripled Nd:YAG laser with wavelength of 355 nm was used. The spot size was as small as 10-30 μm with pulse

duration of 30 ns to achieve the power density of $10^8 - 10^{10} \text{ W/cm}^2$ to completely evaporate material with a negligible amount of melt (Fig. 2). The laser process is maskless and a PVA layer has been deposited on the wafer to prevent the wafer surface from contamination by the ejected material.

The fabricated vias were $50 \mu\text{m}$ in diameter and spaced horizontally (further referred as ‘horizontal vias’, Fig. 3) and vertically (‘vertical vias’, Fig. 4) at a spacing (d_{horiz} and d_{vert} , respectively) of 0, 1, 5, 10, 20, 50, 100, and $200 \mu\text{m}$ measured from the Al metal layer of the n-p-n bipolar transistors. Three types of transistors with emitter areas of $1 \times 40 \mu\text{m}^2$, $10 \times 40 \mu\text{m}^2$ and $40 \times 40 \mu\text{m}^2$ were analyzed.

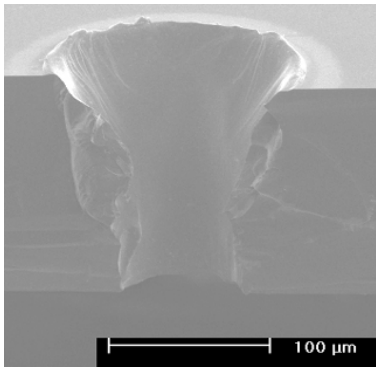


Figure 2: Cross-section of laser-ablated vias.

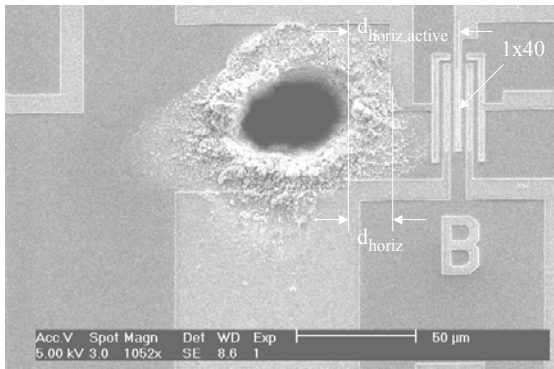


Figure 3: Horizontally spaced via, Emitter area of the transistor is $1 \times 40 \mu\text{m}^2$.

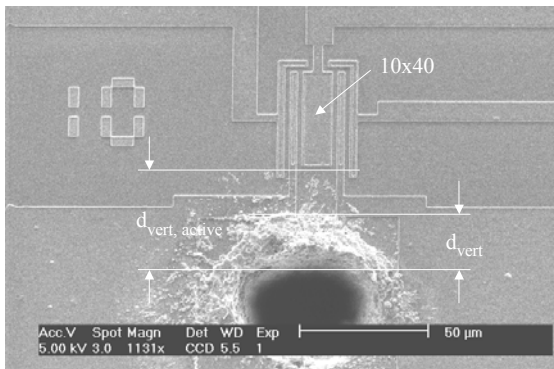


Figure 4: Vertically spaced via, Emitter area of the transistor is $10 \times 40 \mu\text{m}^2$.

Because of the positioning accuracy of the laser ($\sim 15\text{-}25 \mu\text{m}$ in the given setup) the actual position (d_{horiz} and d_{vert}) of the vias was measured with a SEM. The Al metallization was used as a reference point. The actual spacing from the vias to the active region (emitter) of the transistor ($d_{\text{horiz,active}}$ and $d_{\text{vert,active}}$) were $d_{\text{horiz,active}} = d_{\text{horiz}} + 17 \mu\text{m}$ and $d_{\text{vert,active}} = d_{\text{vert}} + 23 \mu\text{m}$.

The gummel plots of selected transistors were measured with an automated Cascade probe system. In total 486 transistors were measured before and after vias were fabricated. The influence of via fabrication was judged by comparing the measured gummel plots of n-p-n transistors before and after the via fabrication. Slope of I_b at $V_{be} = 0.6 \text{ V}$ was used as a figure of merit, and deviations of the $\text{diff } I_b$ from 0 (where $\text{diff } I_b$ is difference in slope I_b after and before via fabrication) was used to evaluate the possible transistor damage.

The transistors with $|\text{diff } I_b|$ outside the standard deviation were referred as degraded transistors. The non-working transistors (slope $I_b = 0$) were not used for calculations of the mean value of $\text{diff } I_b$ and the standard deviation. Final value of $\text{diff } I_b$ was negative (see Table 1) because slopes I_b in the first measurement (before the via fabrication) were always higher or equal to slopes I_b after making vias (second measurement).

Table 1: Comparison of slope I_b before and after making vias, no differences between vertically and horizontally spaced vias is made.

	Before via fabrication	After via fabrication
slope I_b	16.74	16.29
standard deviation of slope I_b	0.8864	1.0335
$\text{diff } I_b$ (mean)	-	-0.462
standard deviation of $\text{diff } I_b$	-	0.913

III. RESULTS

The measured bipolar transistors were divided into three groups: non-working transistors, transistors with $\text{diff } I_b$ outside standard deviation (referred as ‘degraded’ transistors) and working transistors (Table 2). As expected, the performance of the reference transistors without vias was the same before and after the via-fabrication. In total 35 transistors did not work and 53 transistors showed a degraded electrical characteristic after the via fabrication. The fact that the number of non-working transistors and the number of degraded transistors with horizontal vias is lower than with vertical vias, is probably related to the fact that the laser positioning accuracy has a positive offset in lateral

Table 2: Number of non-working and degraded transistors before and after via fabrication.

	Before		After via fabrication		
	Total	Total	w/o vias	with 'vertical' vias	with 'horizontal' vias
Total No.	486	486	18	234	234
No. of non- working	0	35	0	29	6
No. of degraded	0	53	0	43	10

direction, so that horizontal vias were fabricated mostly farther from Al metallization than designed. Significant differences between the three types of transistors (emitter areas $1 \times 40 \mu\text{m}^2$, $10 \times 40 \mu\text{m}^2$ and $40 \times 40 \mu\text{m}^2$) were not observed.

Figure 5 shows the distribution of non-working transistors vs. vertical via spacing $d_{\text{vert,active}}$. This distribution indicates that the affected zone of the vias is not larger than $20 \mu\text{m}$. It should be mentioned that the distances $d_{\text{vert,active}}$ used in Figure 3 are the designed distances, thus not the actual measured ones.

Figure 6 shows the $\text{diff } I_b$ vs. $d_{\text{vert,active}}$ of some decreased and non-working transistors. The distribution of the non-working transistors shows that the affected zone of the vias is not larger than $10\text{-}20 \mu\text{m}$.

preventing the good electrical contact to the measurement pads.

A reason for the decrease in electrical performance could be the partial damage of Al metallization by sputtered material around the vias.

In fact the thermal diffusion depth $h \sim (D\tau)^{0.5}$, where D is the thermal diffusion coefficient of silicon, τ is the pulse duration of the laser, is about $6 \mu\text{m}$ for 30 ns laser pulse, which probably limits the thermally affected zone. Transistors closer than $6 \mu\text{m}$ to the vias could be damaged thermally during fabrication of the via. But this effect is only a minor effect compared to the effect of damage of the Al metallization.

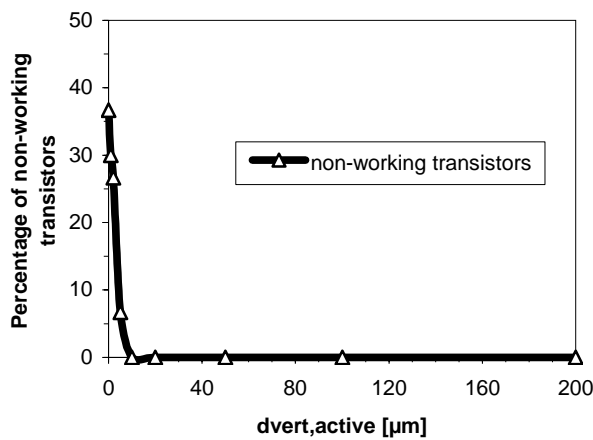


Figure 5: Distribution of non-working transistors vs. vertically distance from the via to the active region of the n-p-n bipolar transistors ($d_{\text{vert,active}}$).

The main observable reason for the non-working transistors was damage to the Al metallization. However, for a few non-working transistors no visible damage of Al on SEM photographs were observed. The presence of sputtered material around the vias could have a negative influence on the measurements due the possibility of

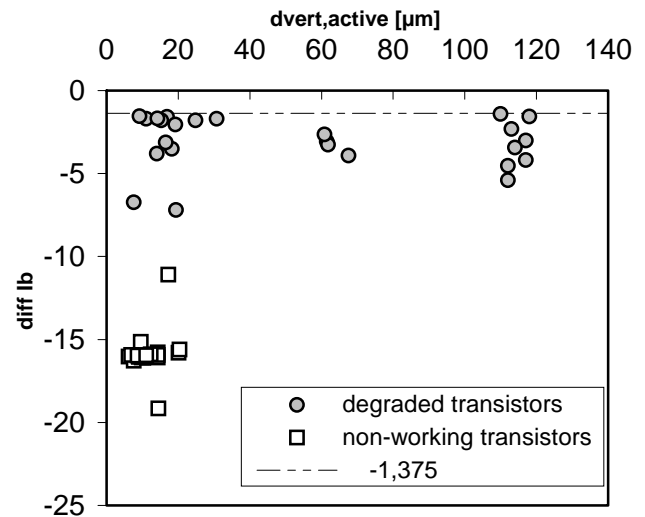


Figure 6: Distribution of $\text{diff } I_b$ for non-working and degraded transistors. The actual distance of the vias to the active region of the n-p-n bipolar transistors ($d_{\text{vert,active}}$) was measured with SEM. $\text{Diff } I_b = \text{slope } I_b \text{ after making vias} - \text{slope } I_b \text{ before making vias}$.

IV. CONCLUSION

The effect of through-substrate vias on electrical performance of bipolar transistors in their vicinity has been studied. For this purpose, vias were fabricated using tripled Nd:YAG laser ablation and were spaced at 0 to $200 \mu\text{m}$ from the Al metallization of the transistors.

The results show that the electrically affected zone at the substrate surface is not larger than 20 μm . The main reason for a non-working transistor after via fabrication is damage to the Al metallization. No significant effects due to thermal damage in the silicon substrate are observed.

V. REFERENCES

- [1] S.F. Al-Sarawi, D. Abbott, P.D. Franzon, "A review of 3-D packaging technology," IEEE Trans. on CPMT, Part B, 21 (1998), pp. 2 – 14.
- [2] Blue Whale project description: <http://hitec.ewi.tudelft.nl/scripts/detail.asp?id=4104>
- [3] A. Polyakov, T. Grob, R.A. Hovenkamp, H.J. Kettelarij, I. Eidner, M.A. de Samber, M. Bartek, J.N. Burghartz, "Comparison of Via-Fabrication Techniques for Through-Wafer Electrical Interconnect Applications," 54th ECTC conference, June 1-4, 2004, pp. 1466-1470.