The Effect of an Electric Field on a Lateral Silicon Light-Emitting Diode

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Abstract— **In this paper, we investigate lateral p$^+$pn$^+$ silicon diodes fabricated on Silicon-On-Insulator. This device distinguishes itself from previous devices by an extra poly-silicon gate electrode on top of the active light-emitting region. The silicon handle substrate is used as second (bottom) gate. When the diode is working under constant current condition, we observe an increased light output as the gate and/or the substrate are biased with negative voltage. The intensity profile across the device is also strongly influenced. In other words, the light emission from a silicon LED can be varied using a MOS gate. To understand the device thoroughly, the structure has also been simulated showing consistent agreement with experimental measurements.**

Keywords— **silicon LED, electric field effect, optical modulation, refractive index, radiative recombination**

I. Introduction

The need for an efficient and fast light emitter that can be intimately integrated with silicon integrated circuitry is unquestionable. The use of silicon itself as the light emitting material is one of the approaches to the problem. However, the indirect band gap of silicon is the fundamental obstacle that requires a workaround to achieve sufficient efficiency and speed of operation.

SOI materials have vastly increased their role in modern IC industry thanks to its clear advantages over conventional silicon wafers. Silicon devices such as microprocessors, photodetectors, OEICs . . . [1], [2], [3] have been fabricated using SOI wafers. An SOI substrate consists of a thin single-crystal, defect-free sheet of silicon sitting on top of an insulator. This isolation of the thin silicon sheet (called device layer) from the bulk by the buried oxide (BOX) layer is very appropriate for realizing novel-concept devices.

The use of this material for realization of silicon light emitters was first based on the idea of introduction of potential barriers into the active light emitting region [4]. The realization of the thin silicon region acting as potential barriers has encountered technological difficulties. Using a vertical electric field to modulate the carriers' profile in the active region to favor radiative recombination is an immediate other solution for realizing an efficient lateral diode. The SOI wafers used in this research have silicon device layer thickness of few hundred of nanometer which can be easily regulated by an electric filed using a MOS gate and/or the handle substrate. Previously reported devices [5], [6], [7] are in fact similar lateral P-I-N diodes, however the advantage of having a MOS gate was not available.

This paper discusses the idea of our approach, then the fabrication of the devices, followed by characterization, observed phenomenon and the explanatory arguments.

II. Experimental details

A. Device fabrication

The starting material is 4-inch SIMOX SOI substrate, with silicon layer and buried oxide (BOX) layer thickness of 190 nm and 350 nm, respectively. The device layer is p-type silicon of resistivity of $20\Omega\ \mathrm{cm}^{-1}$. First a high quality oxide layer of 34 nm was grown in a furnace at 950 °C, followed immediately by deposition of 50 nm stoichiometric $\mathrm{Si_3N_4}$. Then silicon islands were formed on the substrate by a first mask step to etch away the $\mathrm{Si_3N_4}$ and $\mathrm{SiO_2}$ stack, selective etching in TMAH 10% solution will etch the silicon layer into islands. Implantation of BF_2^+ and As^+ with doses of $3.10^{15}\mathrm{cm}^{-2}$, were used to fabricate the highly doped p-type and n-type regions. These heavy doping regions are localized to contact areas. The top $\mathrm{Si_3N_4}$ layer was then remove and 300nm poly-silicon gate were deposited. Phosphorus implantation doping of the poly-silicon layer was done at $4.10^{15}\mathrm{cm}^{-2}$ at the energy of $\sim$ 65 keV. Dopant activation was processed by a furnace anneal at 950 °C for 50 min. Final steps are shaping the poly-silicon layer, dielectric inter-layer deposition, contact hole and metallization.

Metal contact areas were fabricated by sputtering of Ti/W barrier layer and Al (1% Si) on the wafer after contact holes had been opened in the deposited oxide interlayer.

B. *Measurement setup*

The measured device is sketched in Fig. 1. The length of the active region is varied from 3.5μm to 25μm. Compared to a conventional MOSFET fabricated on SOI, the difference is at the source region where silicon has opposite doping to the drain. In operation, the drain is grounded, the source is connected to a current source, the gate and the substrate are separately controlled by two voltage sources. To investigate the influence separately, either gate or substrate is grounded. When a current is supplied to the device, photon emission is observed by means of an infrared camera [8]. An image of photon emission over the active region of the device is shown in Fig. 2. This device has no top polysilicon gate and the active region is a rectangle. The two intense regions at the top and bottom ends are the exposed edges of the device where photons see a larger escaping angle. The right and left edges show the enhanced emission at the junctions p^+/p and p/n^+. It has been known that the p^+/p always shows stronger intensity compared to the other junction. This is understood by the fact that electrons have higher mobility than holes, thus under a certain injection level, the hole concentration at the p^+/p junction is always higher while the electron concentration difference between the junctions is smaller. Device simulation supports this explanation (see III-C).

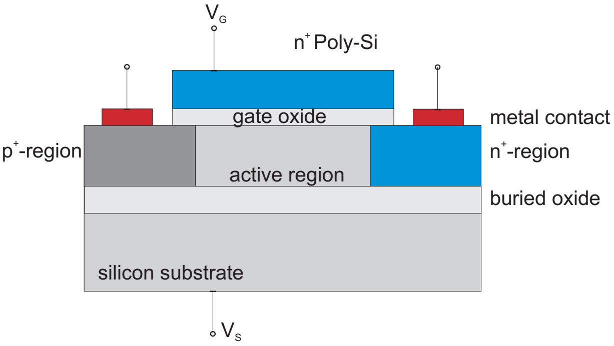

Fig. 1. Sketch of the device structure

III. Results and Discussion

A. *Gate oxide*

Due to the difference in device processing compared to the normal CMOS process (polysilicon gate was not deposited immediately after the gate oxide) it was necessary to check the oxide quality. Capacitance-Voltage (CV) measurements were carried out on MOSFET test structures. Fig. 3 shows two curves for two different type of devices. It is interesting to notice the difference of MOS CV curves on this SOI wafer compared to that on standard substrates [9]. From the characteristics, it is concluded that the gate oxide is of good quality [10].

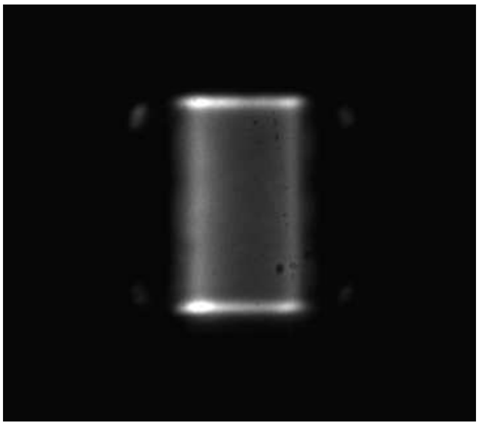

Fig. 2. Emission image of a lateral diode device without gate

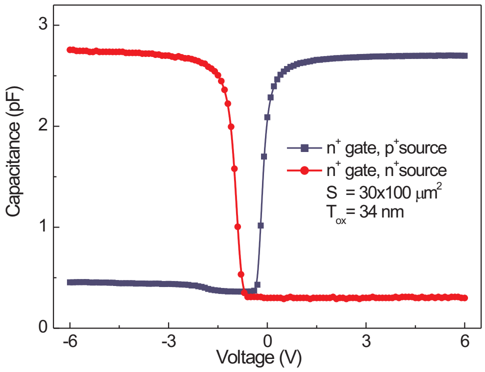

Fig. 3. High frequency CV characteristics at 100 kHz

B. *Influence of gate and substrate biases*

In MOSFETs, the voltage on the gate electrode is to control the conductivity of the channel which determines the operation of the device. Without the MOS gate the device is two back-to-back diodes and would not let direct electrical currents pass. On the contrary, in our structure the gate will only have supplementary role due to the fact that the p^+pn^+ is a diode with a lowly-doped region and would normally allow a forward-biased current. The gate action would mostly modify the interfaces and probably the behavior of the carriers such as mobility. With a standard lateral diode (without the gate) the influence of the substrate bias are shown in Fig. 4. It is clear that a positive substrate bias reduces the emission intensity, while a negative voltage delivers the opposite effect and that happens mostly at the p/n$^+$ junction. The intensity at the p$^+$/p stays constant for the whole range of negative substrate biases. The gated lateral diodes we aim to investigate (Fig. 1) have similar effect when the gate is biased except that the peak at p$^+$/p also show some increase in intensity (see Fig. 5). The increase of intensity at the p/n$^+$ interface is still the dominant. The final investigation is when both gate and substrate are simultaneously biased (Fig. 6). The same behavior are observed as compared to two previous experiments. However, the difference is that the peak at p/n$^+$ strongly surpasses the intensity at the other peak.

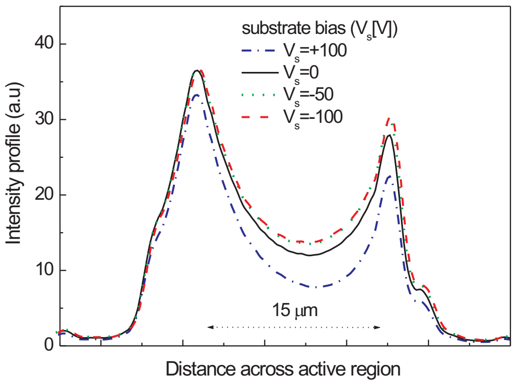

Fig. 4. Field influence on the intensity profile by the bottom gate biases

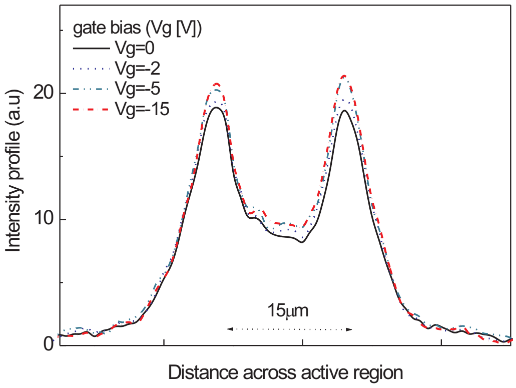

Fig. 5. Field influence on the intensity profile by gate biases

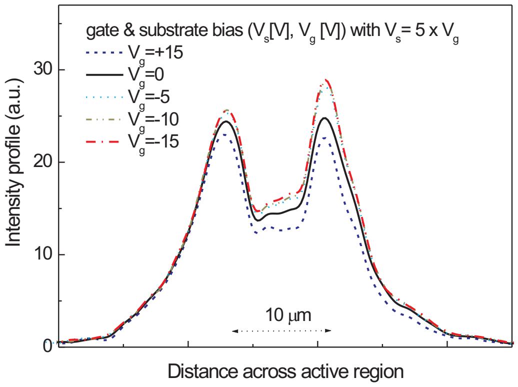

Fig. 6. Field influence on the intensity profile by both gate and substrate biases simultaneously

C. *Simulation and comparison*

To study the trends of the intensity against the applied bias on the gates, we simulate the device structure and its operation using SILVACO 2D device simulation packages [11]. The simulation aims at studying the influence of the electrical field applied on the gate to the change of the total recombination rate. The simulation results are as follows:

- When the gate and substrate are grounded, there are two peaks recombination at p$^+$/p and p/n$^+$ junctions with stronger peak at the former, as previously mentioned.
- When the gate is increasingly biased in the negative direction, both peaks recombination rate increases but at different speeds.

The change of the peak intensity of devices and the simulated recombination rate at junctions are collectively displayed in Fig. 7. Generally speaking the simulation results show a similar trend with the experimental data. At the p/n$^+$ junction, the intensity increases for all devices. The simulation curve shows a similar slope compared to experimental data, the deviation takes place at higher voltages where all experimental curves have a saturation trend. At the p$^+$/p the increase of intensity are less prominent compared to the other junction. There is no change in its intensity for the device without gate under negative biases (see Fig. 4).

D. *Discussion*

It is seen in Fig. 7 that at the p/n$^+$ junction the gate has stronger influence at a voltage of 5 V and below. It is argued that this is due to the steep change of

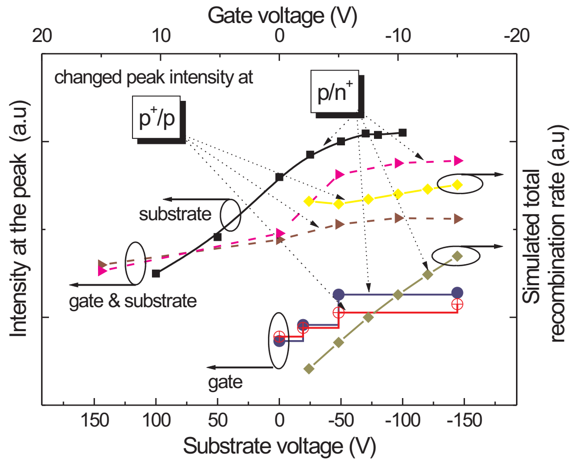

Fig. 7. Trends of intensity peaks and simulated total recombination peaks vs. the applied electrical field at both junctions

the interface at this voltage range (threshold voltage). The increase in intensity in general when a negative field is applied could be explained by the sweeping of electrons away from the non-radiative recombination centers at the interfaces between silicon and oxide. The stronger increase at the p/n^+ junction could just be another result of the negative voltages which cause accumulation of a hole layer under the gate. This channel increases the availability of holes for recombination at the p/n^+ junction.

IV. Conclusion

In conclusions, it is definite that applying an electric field via the gate and/or the substrate influences the light emission properties of the lateral diode fabricated on SOI substrates. It is a gain effect when negative bias is applied. The right combination of gates could introduce the capability to modulate optical processes in the active region of the device. In our current measurement setup it is not yet possible to observe photon emission from the backside of the substrate, thus the optical impact of the polysilicon layer on the emitting profile is still not studied.

Acknowledgment

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