

JFET test structures for monitoring strain-enhanced mobility

L. Shi, G. Lorito, V. Jovanovic, S. Fregonese and L.K. Nanver

Abstract— In this work, a novel method for characterizing the mobility enhancement in strained silicon layers is proposed. The idea is to use the electrical characteristics of a single-gate Junction Field-Effect Transistor (JFET) and, in particular, the relation between the differential transconductance in the linear operation mode and the carrier mobility in the strained channel. Firstly, the JFET test structure has been designed and, then, the efficacy of the above technique has been evaluated by means of Medici electrical simulations.

Index Terms— Differential transconductance, single-gate Junction Field-Effect Transistor (JFET), mobility, strained silicon.

I. INTRODUCTION

FOR several technological generations, the scaling-down of the dimensions has been the main guideline for improving the device speed. Nevertheless, the nowadays miniaturization levels are so extreme that any further reduction poses heavy problems for the process control and reliability, and thus requires significant investments in terms of both, money and time. Since few years, another approach has been gaining acceptance. The basic idea is to increase the device speed by reducing the “resistance” of the semiconductor material to the carrier flow along the active current path. In this regard, strained silicon layers have been recognized as a reliable and low-cost solution [1][2]. In view of this, the characterization of the mobility enhancement versus stress relation in strained silicon layers assumes a relevant importance.

The widely used method for measuring the mobility is the split capacitance-voltage technique [3][4][5], which derives the effective mobility value in the inversion layer of a MOS transistors from the measurements of the gate-to-channel capacitance, C_{GS} , and the drain current, I_D . Beside the issue of the accuracy, this technique allows to analyze the mobility only in the few nanometers thin region of the inversion layer below the gate oxide.

In this paper, an alternative technique for characterizing the strain-enhanced mobility is proposed and validated with MediciTM simulations. The idea is to design a single-gate Junction Field-Effect Transistor (JFET) having the strained

silicon layer as channel and to analyze the electrical characteristics of a such device. More specifically, the mobility enhancement is investigated using the sensitivity to the strain of the differential transconductance in linear operation mode, g_{mL} . Moreover, modulating the channel thickness by the gate voltage, this technique gives the opportunity to monitor the mobility within a relative wide region below the gate.

II. THEORETICAL CONSIDERATIONS

Fig.1 shows a simplified single-gate n-channel JFET structure.

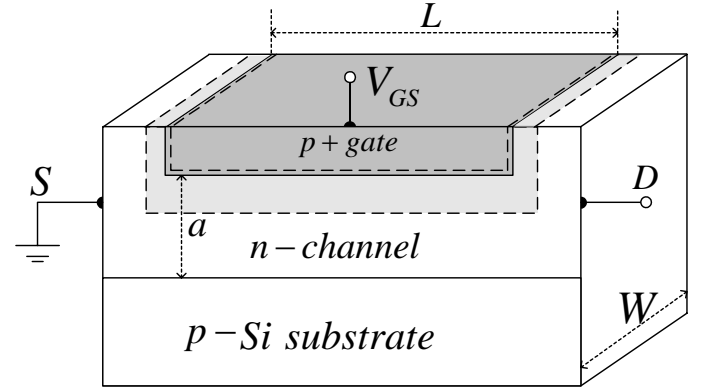


Fig.1. Schematic structure of single-gate n-channel JFET.

In the following analysis it is assumed that the modulation of channel thickness derives mainly from V_{GS} while the changes in the channel-substrate junction depletion region induced by V_{DS} have a negligible effect on it.

Considering uniform dopings and the approximation of complete depletion of the space-charge regions, the drain current in linear operation mode (i.e. with $0 \leq |V_{GS}| \leq |V_P|$ and $0 \leq V_{DS} \leq V_{DS,sat}$, where V_P is the pinch-off voltage and $V_{DS,sat}$ is the saturation voltage of the device) can be expressed as [6]:

$$I_{DL} = \frac{\mu_n q^2 N_{ch}^2 W a^3}{6 \epsilon_s L} \cdot \left\{ 3 \left(\frac{V_{DS}}{V_{p0}} \right) - 2 \left(\frac{V_{DS} + V_{bi} - V_{GS}}{V_{p0}} \right)^{3/2} + 2 \left(\frac{V_{bi} - V_{GS}}{V_{p0}} \right)^{3/2} \right\} \quad (1)$$

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where N_{ch} is the channel doping, V_{bi} is the built-in potential of the gate-channel pn junction and V_{p0} is given by

$$V_{p0} = \frac{qN_{ch}a^2}{2\epsilon_S} \quad (2)$$

Therefore, $g_{mL} = \partial I_D / \partial V_{GS}$ is equal to

$$g_{mL} = \frac{\mu_n q^2 N_{ch}^2 W a^3}{2\epsilon_S L V_{p0}} \sqrt{\frac{V_{bi} - V_{GS}}{V_{p0}}} \left\{ \sqrt{\left(\frac{V_{DS}}{V_{bi} - V_{GS}} \right) + 1} - 1 \right\} \quad (3)$$

Inserting (2) in (3), finally we achieve

$$g_{mL} = \frac{\mu_n W}{L} \sqrt{2q\epsilon_S N_{ch}} \left(\sqrt{V_{DS} + V_{bi} - V_{GS}} - \sqrt{V_{bi} - V_{GS}} \right) \quad (4)$$

Relation (4) is the key relation for following analysis.

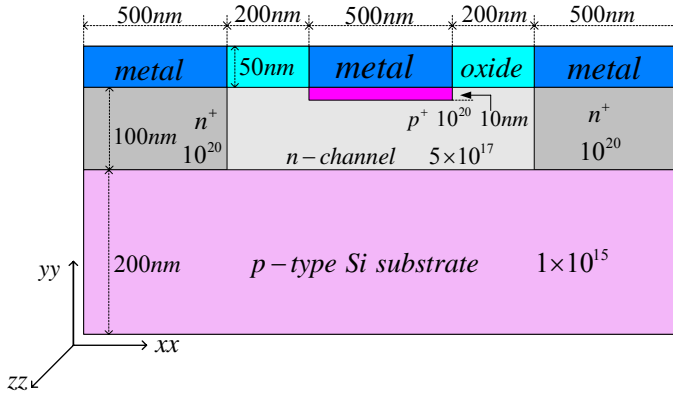


Fig.2. The simulated single-gate JFET test structure.

III. SIMULATIONS

The simulated single-gate JFET test structure is shown in Fig. 2. The gate length is 500 nm and the metallurgical thickness of the channel is 90nm. All the dopings are uniform. The n-channel doping level has been chosen in order to have the higher channel conductance with a negligible leakage current due to tunneling at the gate-channel junction. The p-substrate has been assumed very lightly doped to make the bottom edge of the channel extremely near to the channel-substrate interface.

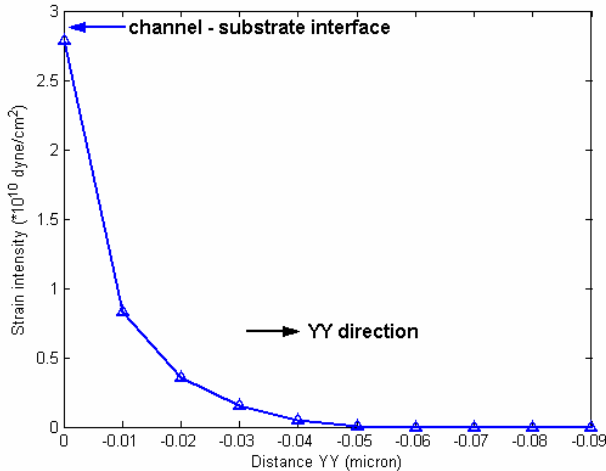


Fig.3. Tensile stress profile in the n-channel.

Electrical simulations of the above test structure have been performed with and without the tensile stress profile reported in Fig.3. The strain is uniform in the xx - zz plane and maximum at the channel-substrate interface. It decreases along the yy direction moving towards the gate and reaches zero at a distance of 50 nm far from the channel-substrate interface. The orientation and the peak value of the strain have been obtained from the Taurus process simulation of the Si-Si_{0.8}Ge_{0.2} layer growth.

In Fig. 4, the simulated I_D - V_{DS} output characteristics for several V_{GS} values of the devices with strained and unstrained channel are compared. Similarly, Fig. 5 shows the effect of the tensile stress in the channel on the I_D - V_{GS} plot for $V_{DS}=50$ mV and on pinch-off voltage V_P [7]. In all the simulations the source and substrate have been grounded.

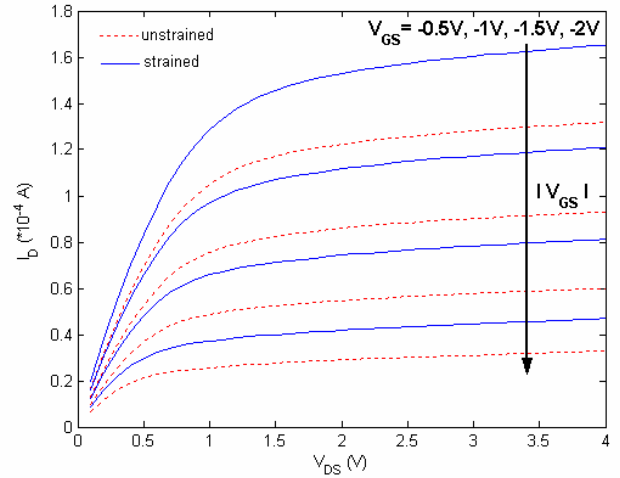


Fig.4. Simulated I_D - V_{DS} output characteristics for $V_{GS} = -0.5$, -1 , -1.5 , -2 V of the JFET test structure with and without the strain profile reported in Fig.3.

IV. DISCUSSIONS

The output characteristics reported in Fig. 4 show that for $V_{DS}=50$ mV and V_{GS} up to -2 V the JFET is working in linear mode with or without the presence of stress in the channel. For a further confirmation, note that in both cases the pinch-off voltage V_P for $V_{DS}=50$ mV is higher than -2.5 V as indicated in Fig. 5.

Fig. 6 reports the simulated differential transconductance versus V_{GS} plots for $V_{DS}=50$ mV when V_{GS} ranges from -0.4 V to -2 V for the device with strained ($g_{mL,S}$) and unstrained (g_{mL}) channel. Fig.7 shows the ratio $g_{mL,S}/g_{mL}$ for the same range of V_{GS} .

Note that it is reasonable to assume that the presence of stress has no effect on V_{bi} since at thermodynamic equilibrium the gate-channel junction depletion region remains confined to the not strained region of the channel, as shown in Fig. 8. Differently, the presence of stress changes the value of dielectric constant ϵ_S of the material; in particular, ϵ_S increases as larger is the lattice constant of the material, that is as closer the depletion region is to the channel-substrate interface and, hence, as higher is the absolute value of V_{GS} . Nevertheless, for

the chosen peak value of the stress, this effect causes an increase in ϵ_s lower than 7% [7] and thus we can assume

$$1 \leq \sqrt{\frac{\epsilon_{s,s}}{\epsilon_s}} \leq \sqrt{\frac{1.07 \epsilon_s}{\epsilon_s}} = 1.03 \quad (5)$$

where $\epsilon_{s,s}$ is the strain-affected dielectric constant.

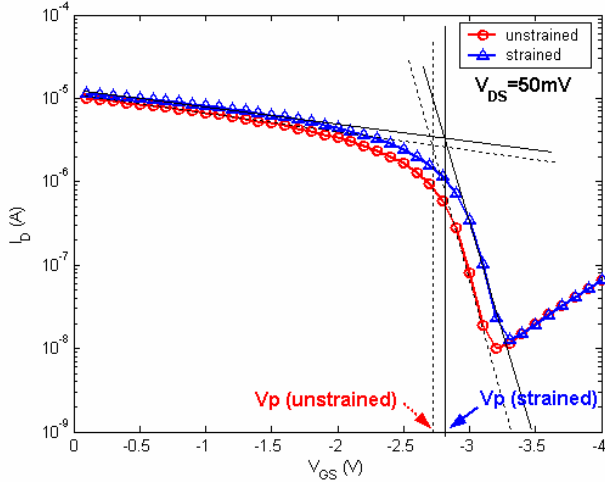


Fig. 5. Simulated I_D - V_{GS} plot for $V_{DS}=50\text{mV}$ of the JFET test structure with and without the strain profile reported in Fig.3.

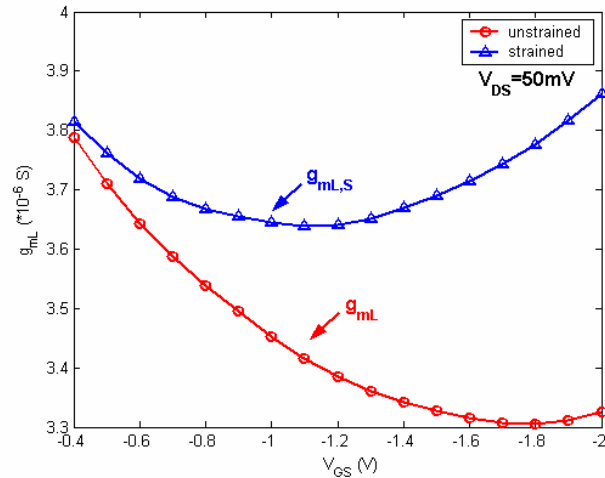


Fig. 6. Simulated g_{mL} - V_{GS} plot for $V_{DS}=50\text{mV}$ of the JFET test structure with and without the strain profile reported in Fig.3.

Therefore, from equation (4) and using (5), we can derive that

$$\frac{g_{mL,s}}{g_{mL}} \approx \frac{\mu_{n,s}}{\mu_n} \quad (6)$$

where $\mu_{n,s}$ is the mobility in the strained channel.

In conclusion, the strain-induced increase of the differential transconductance in linear mode, g_{mL} , can be used to evaluate the corresponding mobility enhancement in the channel.

V. CONCLUSIONS

In this work a new and reliable technique for characterizing

the mobility enhancement in strained-silicon layers is proposed and validated by means of numerical simulations. In particular, it is demonstrated that the differential transconductance in linear mode of a single-gate JFET having the strained layer as channel is a sensitive indicator to the presence of the stress and that, using equation (6), it can be directly related to the mobility improvement in the channel.

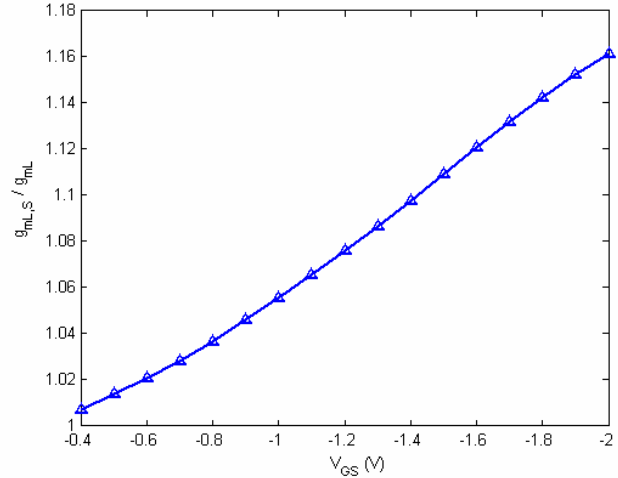


Fig. 7. Simulated $g_{mL,s}/g_{mL}$ plot for $V_{DS}=50\text{mV}$ of the JFET test structure.

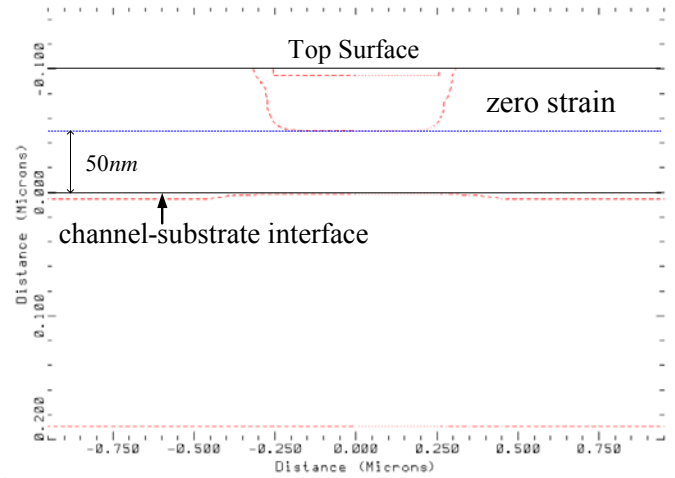


Fig. 8. Simulated depletion region borders at thermodynamic equilibrium.

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