Molecular Tuning of Electrical Properties of Mercury-Insulator-Silicon Diodes

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***Abstract*— The influence of silicon surface modification via Si-C_nH_{2n+1} (n=10,12,16,22) devices on p-type (100) silicon is studied by forming MIS (metal-insulator-semiconductor) diodes via a mercury probe. With the use of current density - voltage (J-V) and capacitance - voltage (C-V) measurements the relevant parameters describing the electrical behavior of these diodes are derived and compared with samples with a native oxide insulator.**

The insulating properties of these MIS diodes can be precisely tuned by varying the monolayer thickness. Insulating layers with n ≥ 12 show better insulating behavior than native oxide. Despite a comparable thickness of the C_{16} monolayer as compared to the native oxide layer, the former showed even a tenfold decrease in leakage current. Evaluation of the average tunneling constant (β) of these monolayers reveals 0.45 $Å^{-1}$. Evaluation of the dielectric constants (ε_r) gave values of 1.7 ± 0.3 and 2.2 ± 0.4 for n = 16 and 22, respectively, whereas for the fixed charge (N_f) low values of $5.4 \cdot 10^{11}$ and $5.9 \cdot 10^{11}$ cm^{-2} were found for n = 16 and 22, respectively.

The results suggest that Si-C linked monolayers on flat silicon may be a viable, alternative insulator for future electronic devices.

Keywords— **Silicon; organic monolayer; mercury; semiconductor; insulator**

I. INTRODUCTION

The ongoing downscaling of MOSFETs in semiconductor industry has strongly stimulated the research of both new insulating materials on silicon and well-controlled Si-insulator interfaces. SiO_2 is now used both as gate insulator and as insulating material between interconnect lines. The thickness of SiO_2, however, has been pushed towards its fundamental limits [1]. This led to an intensive search for insulators with a high dielectric constant, high-K dielectrics [2] for use as gate insulators, and for insulators with a low dielectric constant, low-K dielectrics [3], respectively.

One of the recently explored, new insulating materials on silicon are covalently bound organic monolayers. Since the first papers by Linford et al. [4-5] the research field of organic alkyl monolayers covalently bound to oxide-free silicon surfaces has expanded dramatically. Recent reviews of organic monolayers on oxide-free silicon surface (concerning their non-electrical aspects) can be found in literature [6-9].

From both a chemical and electrical point of view passivation of the silicon surface via directly bound monolayers offers better possibilities as compared to other monolayer preparation techniques, such as Langmuir-Blodgett films or organic monolayers bound to oxidized surfaces [10]. The Si-C linked monolayers are bound via strong, covalent bonds, which provide a well-defined monolayer. It is shown to be stable to hot solvents, acids and bases [5-6]. Thermal stability up to 615K was observed in ultrahigh vacuum conditions [11]. Organic monolayers on oxide-free surfaces offer a promising alternative due to the formation of real monolayer-silicon interfaces and a well-defined surface morphology, and may serve as new insulating materials in molecular, electronic devices. The fabrication method [12] via "wet-bench chemistry" is relatively easy and cheap as compared to insulators made under cleanroom conditions. Moreover, the Si-C linked monolayer has a similar thickness as compared to nowadays gate oxides and has outstanding electrical properties as is explored in a number of studies. One example of such a device is for instance the MIS diode [13-14] in which the monolayer acts as insulating barrier and precisely tunes the desired

current-voltage behavior [15-17].

The study described in this proceeding focuses on Si|C_nH_{2n+1} (n = 10, 12, 16, and 22)|Hg structures made on p(100), moderately doped (10^{15} cm^{-3}) silicon substrates. From J-V and C-V measurements the typical parameters describing the electrical behavior of such MIS diodes are derived using the thermionic emission theory. For the longer alkyl chains (n = 16 and 22) a direct analysis from the C-V curves is possible resulting in an evaluation of the dielectric constant and fixed charge density N_f. As a reference and comparison we used samples with a thin native oxide insulator.

II. Theory

A. Current Voltage behavior

The commonly used transport mechanism that describes the J-V behavior of metal | very thin insulator (< 3.5 nm) | moderately doped silicon structures is the thermionic emission theory [13-14]. In this theory the transport mechanism is governed by a thermionic emission process in which the electrons or holes tunnel directly through the insulator as is generally the case for an insulator thickness < 3.5 nm. The thermionic emission theory in which the series resistance of the device under test does not play a role yet is given in Eq. 1 [14] (for the metal positively biased with respect to n-type silicon):

$$J = A^* T^2 e^{(\frac{-q\phi_{eff}}{kT})} e^{(\frac{qV}{nkT})} (1 - e^{-\frac{qV}{kT}}) \tag{1}$$

where J [$A\cdot cm^{-2}$] is the measured current density, V [V] is the applied bias voltage, A^* the Richardson constant (32 $A\cdot K^{-2}\cdot cm^{-2}$ for p-type silicon [13]), T [K] the absolute temperature, kT/q is the thermal voltage (25.7mV at 298K), and n [-] is the diode ideality factor which accounts for the non-idealities in the diode behavior. In the ideal case n = 1. If the transport mechanism is not exclusively a thermionic emission process n > 1. ϕ_{eff} [V] is the effective barrier height. For metal-semiconductor junctions the barrier height ϕ_B is defined as: $\phi_B = \phi_M - \chi$. ϕ_M is the workfunction of the metal and χ is the electron affinity of silicon (4.05V [13]). In case of a thin insulator an extra barrier term is introduced, hereby increasing the total barrier height ϕ_{eff}. Selzer et al. and Liu et al. expressed ϕ_{eff} as given in Eq. 2 [17,21]:

$$\phi_{eff} = \phi_B + \frac{kT}{q}\beta l \tag{2}$$

$kT/q\,\beta l$ [V] describes the additional barrier height imposed by the thin, organic insulator. β is the tunneling constant [$Å^{-1}$] which is dependent amongst other things on the type of insulator and charge carrier (holes for p-Si or electrons for n-Si); l [Å] is the thickness of the insulator.

Using Eq. 1, ϕ_{eff} and n can be derived. Rewriting Eq. 1 into a function of $\ln(J/(1-e^{-\frac{qV}{kT}}))$ vs. V results in Eq. 3:

$$\ln(\frac{J}{1-e^{-qV/kT}}) = \ln(A^* T^2) - \frac{q\phi_{eff}}{kT} + \frac{qV}{nkT} \tag{3}$$

A plot of $\ln(J/(1-e^{-\frac{qV}{kT}}))$ vs. V should give a straight line from zero bias [14]. The ideality factor n can be derived from the slope and the effective barrier height ϕ_{eff} can be obtained via the $\ln(J/(1-e^{-\frac{qV}{kT}}))$-axis intercept.

B. Capacitance Voltage behavior

In ideal C-V measurements the capacitance in accumulation equals the insulator capacitance and hence the thickness or dielectric constant of the insulator can be calculated via the well-known formula: $C = \varepsilon_0 \varepsilon_r A / d$

where ε_0 [$F\cdot cm^{-1}$] is the permittivity of vacuum, ε_r [-] is the dielectric constant of the insulating layer, A [cm^2] is the surface area and d [cm] is the insulator thickness. For a given thickness and area the dielectric constant can be evaluated.

In case of thin insulators, however, the capacitance in accumulation often does not reach a constant value, which can be attributed amongst other things to a voltage dependent accumulation capacitance in series with the insulator capacitance.

If this causes a tilted capacitance in the accumulation regime of the C-V curve, the series circuit can be written as Eq. 4 [14]:

$$\frac{1}{C} = \frac{1}{C_{ins}} + \frac{1}{C_S} = \frac{1}{C_{ins}} - \frac{2kT}{qC_{ins}} \frac{1}{(V_{bias} - V_{fb} - \phi_S)}$$

$$\frac{1}{C} \approx \frac{1}{C_{ins}} - \frac{2kT}{qC_{ins}} \frac{1}{(V_{bias} - V_{fb})} \tag{4}$$

where C_{ins} and C_s are the insulator and accumulation capacitance, respectively; V_{bias} and V_{fb} are the applied voltage and the flatband voltage, respectively and ϕ_s is the silicon surface potential. The flatband voltage can be determined from Mott Schottky plots. In strong accumulation $(V_{bias} - V_{fb}) >> \phi_s$ and ϕ_s can be neglected. A plot of C^{-1} vs. $(V_{bias} - V_{fb})^{-1}$ should then give a straight line with C_{ins}^{-1} being the C^{-1}-axis intercept.

C. *Mott Schottky relation*

The flatband voltage is a very important parameter in the analysis of metal | insulator | silicon structures since it provides directly measurable, quantitative data on the silicon-insulator interface. The flatband voltage is usually derived from C-V curves. However, since C-V plots of thin insulators are often distorted, it is hardly possible to obtain V_{fb} analytically. Fortunately, the Mott Schottky relation provides an answer since it only considers the silicon in the depletion regime. In this region the voltage drop over the thin insulator is considered negligibly as compared to the drop over the depletion layer. In other words, V_{fb} is not influenced by the presence of a very thin insulator (only by the silicon-insulator interface properties). The dominating depletion capacitance can be expressed in the Mott Schottky form as given in Eq. 5 [13] (mercury positively biased with respect to p-type silicon):

$$\frac{1}{C_{sc}^2} = \frac{2(V_{bias} - V_{fb})}{q\varepsilon_0\varepsilon_r N_A A^2} \tag{5}$$

where C_{sc} [F] is the measured depletion capacitance; ε_r is now the dielectric constant of silicon and N_A [cm^{-3}] is the doping concentration. In the linear part of the C^{-2} vs. V_{bias} plot the doping N_A can be graphically determined from the slope and V_{fb} from the voltage-axis intercept.

III. Experimental

A. *Sample Preperation*

Oxidation

A number of p-type wafers were thermally oxidized with different oxide thicknesses. Samples from wafers with approximately 100 nm thermal oxide were made to check ideal C-V behavior and to determine the area of the mercury dot. Samples from wafers with very thin (< 5 nm) oxides were made to compare the electrical behavior of these insulators with the devices under test. The wafers were first cleaned using a standard wafer cleaning (5 min. in 100% HNO_3, copious rinsing in demiwater, 10 min. in boiling (69%) HNO_3 at 95°C and again copious rinsing in demiwater). Just prior to oxidation the wafers received a HF-dip (1%) and were again rinsed in demiwater and spinned dry. The wafers were oxidized in a Tempress Oven using a dry oxidation process in an O_2/N_2 mixture and a subsequent anneal step in a N_2 atmosphere. Before oxidation the oven was cleaned with an RCA cleaning procedure. After oxidation the oxide thickness was measured with ellipsometry.

Backcontact fabrication and dicing

Before backcontact manufacturing wafers without thermal oxide underwent the standard cleaning as described above and the front side was subsequently covered with HMDS and photoresist (Olin 907/12). After that the wafers were pre-baked at 120°C for 30 minutes. A similar procedure was used for oxidized wafers except that they were processed without cleaning after removal from the oven. Then the wafers received a 1% HF dip to remove the native oxide from the backside. A metal contact was made to the wafer via sputtering. A 1000nm aluminum layer was directly sputtered. Next, a chromium layer was sputtered onto the aluminum on both type wafers to protect it from being etched in HF prior to monolayer formation. This was followed by an annealing step at 450°C in a N_2 atmosphere. The photo resist was removed with acetone. Finally, the samples were diced into pieces of 18mm x 25mm.

Preparation of the organic monolayer

The cut Si samples were first wiped with tissue that was saturated with chemically pure acetone. After that, the samples were sonicated for at least 15 min in demineralized H_2O and acetone, respectively. Then the samples were placed in a plasma cleaner/sterilizer (Harrick PDC-32G) for 1 min. Subsequently the samples

were etched in 2.5% HF for 2 minutes. After removal from the HF solution the sample was dry, indicating that the surface was oxide-free.

A 1-alkene solution in mesitylene (12.5 ml, 0.2 M) was placed in a small, three-necked flask fitted with a nitrogen inlet, a condenser with a $CaCl_2$ tube, and a stopper. The solution was deoxygenated for at least 45 min, by refluxing it, while slowly bubbling dry nitrogen through the solution. Subsequently a freshly etched Si sample was added to the refluxing solution by removing and replacing the stopper quickly. After 2h the solution was allowed to cool and the sample was removed and rinsed extensively with distilled PE 40/60, EtOH, and CH_2Cl_2, respectively.

Preparation of the reference samples

The cut samples were sonicated for at least 10 min. in demineralized H_2O and acetone, respectively. Then the samples were placed in a plasma cleaner/sterilizer (Tepla 300E) for 1 min. Subsequently the samples were etched in 1% HF for 1 minute, rinsed with demiwater and dried using a nitrogen gun. The samples were stored for a week to grow a native oxide in air. All oxidized samples were stored in a vacuum oven for at least 12 hours prior to measurement to make sure that the surface was sufficiently dehydrated. Finally, these samples as well as all samples with oxide were rinsed with hexane before measurements to remove organic contaminants.

B. *Physical Characterization*

Directly after cleaning static water contact angles of the monolayers on the silicon samples were obtained using an Erma Contact Angle Meter G-1 (volume of the drop of demineralized H_2O = 3.5 μl). Two or three drops of water were placed near one of the short edges of the sample. This wetted area was not studied in the electrical measurements. The error of the contact angles is ± 1º. After removal of the water drops the samples were cleaned with EtOH and CH_2Cl_2. The samples were stored under a nitrogen atmosphere or vacuum until the electrical measurements took place.

The thickness of oxide layers was measured with an ellipsometer (Plasmos SD 2002) using a fixed refractive index n = 1.465 for the SiO_2 layers. The thickness of the organic monolayers was determined earlier via infrared spectroscopy. The thickness of the C_{10} layer was too thin to be determined via X-ray reflection measurements and was calculated using a model mentioned in ref 5 [18]. Table 1 gives an overview of the results.

Table 1. Static water contact angle and thickness measurements on different insulators.

Insulator	Static water contact angle [°]	Thickness [Å]	Thickness determined via:
Native oxide	-	17.7 ± 0.7	Ellipsometry
C_{10}	107	12.1	Calculated [18]
C_{12}	109	13.2 ± 0.1	X-ray spectrosc. [19]
C_{16}	109	17.8 ± 0.2	X-ray spectrosc. [19]
C_{22}	102	26.0 ± 1.0	X-ray spectrosc. [20]

C. *Electrical Characterization*

I-V and C-V measurements were performed using a mercury probe (Material Development Corporation (MDC) MDC811-150) connected to an HP4140B pA meter and an HP4275A C-V meter. Before the start of the measurements the mercury was renewed. The set-up is computer controlled by the MDC software package CSM/Win. For the I-V measurements the bias voltage was swept from +1.0V to –1.0V. The mercury is positively biased with respect to the bulk silicon. The voltage was swept with a step size of 0.01V at long integration time to measure exclusively the leakage current. All measurements were repeated at least once and in this voltage range none of the samples with organic monolayers showed breakthrough or increase in current during subsequent measurements. For the C-V measurements the DC-voltage was swept in the same way as in the I-V measurements with a step size of 0.01V. The ac-amplitude was 50mV and the measurement frequency was chosen at 400kHz. This frequency should not be too low to prevent quasistatic behavior and to prevent possible interface states from following the ac-signal. At half of the spots C-V measurements were repeated at 10kHz, 40kHz and 100kHz for comparison purposes. The area of the mercury dot was verified via C-V measurements on samples with approximately 100nm oxide (exactly determined via ellipsometry). From the capacitance in accumulation the area was calculated. This was $A = 3.68 \pm 0.11 \cdot 10^{-3}\ cm^2$.

IV. RESULTS AND DISCUSSION

A. Current Voltage Behavior

The average leakage current density J-V data for different insulators on p-type silicon samples are displayed in Figure 1.

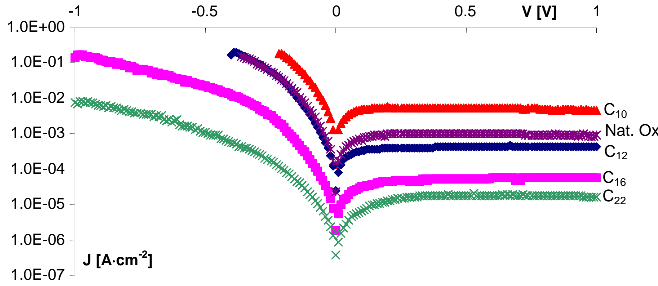

Figure 1. Leakage current density data for different insulators on p-type silicon.

The effect of the monolayer on the J-V behavior is clearly visible. The J-V curves all have the same Schottky diode characteristic shape, indicating a similar transport mechanism through all insulators. The magnitude of the current density can be precisely tuned by varying the length of the 1-alkene as was also observed by various other researchers via electrical means [15,17,21]. Despite the comparable thickness of the C_{16} monolayer as compared to the native oxide (1.78 ± 0.02 nm versus 1.77 ± 0.07 nm) the organic monolayer displays at least a 10-fold increase in insulating behavior. This is a clear indication for the good insulating properties of these layers.

Now the diode ideality factor n and effective barrier height ϕ_{eff} (Eq. 1 and 3) are derived from $\ln(J/(1-e^{-\frac{qV}{kT}}))$ vs. V plots. In this analysis the series resistance R_S is not taken into account so only the part from 0 up to |0.2| V is considered for analysis to exclude any influence from R_S. The results are given in Table 2.

Table 2. Parameters derived from thermionic emission theory.

insulator	n [-]	ϕ_{eff} [V]
C_{10}	1.89	0.525
C_{12}	1.59	0.590
C_{16}	1.67	0.662
C_{22}	2.13	0.708
Nat. Ox.	1.72	0.578

The ideality factors n show that C_{12} and C_{16} layers display more ideal diode behavior than native oxide. The value for the C_{12} (1.59) is larger than the one reported by Liu et al. [17] for p(111) $|C_{12}H_{25}$ samples (1.33 ± 0.10). A direct comparison is not possible, however, since n generally varies over the J-V range of a diode [14] and a different current regime and different method for the derivation of n are used in this study. We used a low current regime for our analysis in which n is normally higher than for high forward currents. The C_{22} layer gives the least ideal diode behavior as can be expected from the fact that thicker insulators often give less ideal diode behavior. The calculated effective barrier height ϕ_{eff} increases with increasing monolayer thickness.

β can be calculated graphically via the combination of ϕ_{eff} vs monolayer thickness plots and Eq. 2 (Figure 2).

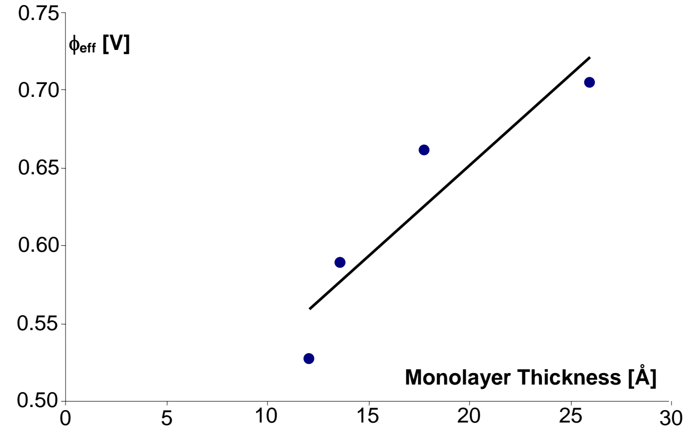

Figure 2. ϕ_{eff} vs monolayer thickness.

From these data and Eq. 2 it follows that $\beta = 0.45$ Å^{-1}. This is in agreement with theoretical values mentioned in literature, $\beta = 0.4 - 0.8$ Å^{-1} [21], for hole tunneling through alkyl chains.

B. Capacitance Voltage behavior

The results for the C-V measurements are depicted in Figure 3.

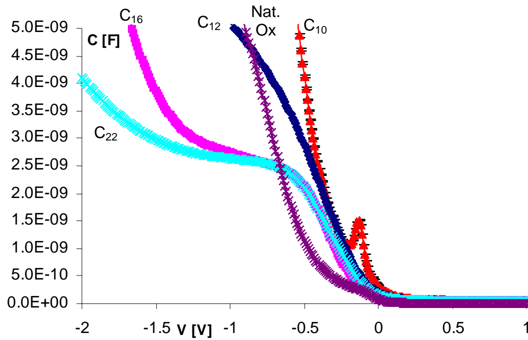

Figure 3. Capacitance voltage plots of different insulators on p-type silicon.

The C-V curves for samples with C_{10}, C_{12}, and native oxide insulators are typical for metal-semiconductor junctions [14] since the capacitance in accumulation increases monotonically with the applied voltage. In Figure 3 a peak in the C-V curve of C_{10} at -0.2V appeared. This peak can be caused by interface charge present at the silicon-monolayer interface. At the voltage where the interface charge is contributing to the total charging current a peak now appears in the C-V plot. The presence of a larger amount of interface charge at the C_{10} sample correlates to the deviating flatband voltage for C_{10} compared to the flatband voltage for layers > C_{10} as will be discussed in the next section. The capacitance curves for samples with C_{16} and C_{22} insulators display a plateau in the accumulation regime around -1V and increases strongly again for higher voltages. The tilted capacitance in the plateau of the accumulation regime is further analyzed via Equation 4. For this, the assumption is made that the tilted capacitance arises from a series circuit of the insulator capacitance and a bias dependent accumulation capacitance.

At first it was verified whether the measured capacitance in the C-V curves displayed any frequency dependency by comparing the C-V plots for different frequencies. During the measurements R_s was compensated for to exclude frequency distortion in the C-V curve as a result of the series resistance. A frequency distortion can occur when measuring on samples with high series resistance while a parallel circuit of a capacitor and resistor is used as C-V impedance model [14]. Figure 4 gives the typical C-V curves for a p-silicon C_{22} sample measured at 10, 40, 100, and 400kHz. No significant capacitance shift occurred in the accumulation regime at any of the samples.

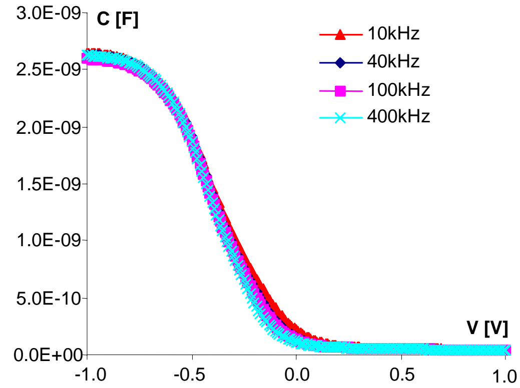

Figure 4. C-V curves of a p-Si|$C_{22}H_{45}$|Hg MIS structure at different frequencies. No frequency dispersion was observed in the accumulation regime.

A typical plot of C^{-1}vs $(V-V_{fb})^{-1}$ for C_{16} and C_{22} insulators is depicted in Figure 5. The linear extrapolation of the curve with the C^{-1} axis intercept yields the inverse insulator capacitance C_{ins}^{-1}.

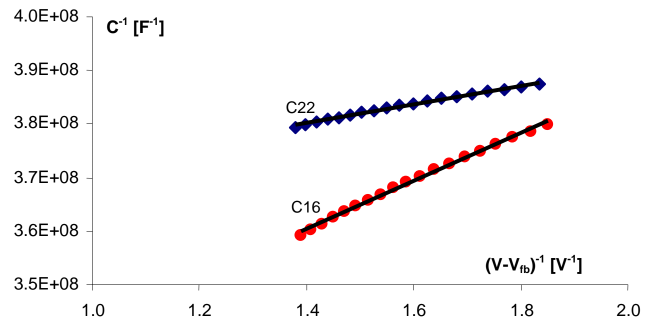

Figure 5. C^{-1} vs $(V-V_{fb})^{-1}$ plot for C_{22} and C_{16} insulators on p-type silicon.

With the thickness and area known the dielectric constant can be graphically evaluated. This rendered ε_r = 1.7 ± 0.3 and 2.2 ± 0.4 for C_{16} and C_{22} organic monolayers.

These values are in close agreement with value ε_r = 2 found for alkylthiolate monolayers on mercury hanging drop electrodes and ε_r = 2.7 ± 0.3 for Hg-alkanethiol/alkanethiol-Hg junctions [22-23]. Kar et al. [24] reported a value of 2.13 for a C_{18} monolayer on Al|$C_{18}H_{37}$|p&n-Si devices, which is within the experimental error of the value for the C_{22} layer. The

values are, however, much lower than the reported value of $\varepsilon_r = 3.3 \pm 0.6$ from Yu et al. [25]. It is expected that a large amount of oxide would increase the effective dielectric constant since $\varepsilon_r = 3.9$ for SiO_2. This implies that there is more oxide present inside the C_{22} layers than the C_{16} layers, which could be an indication for the lower static water drop contact angles on these layers (102° for C_{22} and 109° for C_{16}). Also the low water drop contact angles, 90.6 ± 3.0º up to 101 ± 7.5º, combined with the high dielectric constant found in ref 25 are in line with these observations.

C. Mott Schottky analysis and Interface charge

The C-V data plotted in the Mott Schottky form is given in Figure 6.

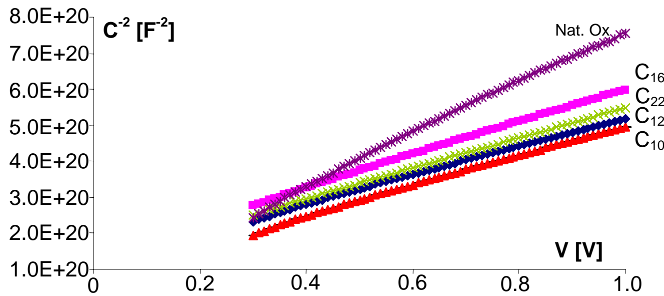

Figure 6. Mott Schottky plots for different insulators on p-type silicon.

The plots for the insulators on p-type silicon were all linear in the region +1.0 V to +0.3 V. The measurements shown here were performed at 400kHz. The measurements were also carried out at 10kHz, 40kHz, and 100kHz to check whether there is a large frequency dependency on the calculated doping and flatband voltage. A frequency dependency in the Mott Schottky plots is often encountered in electrochemistry on semiconductors and can be attributed to numerous causes, like -amongst other- surface states [26]. The calculated doping did not show any frequency dependency for all organic monolayers. The flatband voltage showed a maximum difference of 17% between 10kHz and 400kHz for the C_{12} layer. Flatband voltages compared between 10kHz and 400kHz for the other insulators stayed within an error of 10%. The flatband voltage V_{fb} and doping density are calculated using Eq. 5 and are listed in Table 3. The theoretical flatband voltage is added in the third column for comparison purposes.

Table 3. Parameters derived from the Mott Schottky analysis.

Insulator	V_{fb} [V]	$V_{fb,theory} = \phi_{MSi}$ [V]	N_A [10^{15} cm^{-3}]
C_{10}	-0.22	-0.45	2.0
C_{12}	-0.34	-0.45	2.1
C_{16}	-0.34	-0.45	1.8
C_{22}	-0.32	-0.45	2.0
Nat. Ox.	-0.11	-0.45	1.2

The flatband voltages for C_{12}, C_{16} and C_{22} layers are in close agreement with each other. This indicates that the properties of the silicon-monolayer interfaces are equal for all these monolayers independent of the thickness of the monolayer. An equal flatband voltage for different monolayer thickness was also observed by Hu et al. and Bansal et al. [27-28] who observed this in their electrochemical experiments on n-type (111) Si-electrodes covered with organic monolayers. They ascribed this effect to the neutral character of an adsorbate bound to the silicon surface involving covalent Si-C bonds. The flatband voltage for C_{10} on p-silicon is less negative than the other monolayers on p-silicon, indicating a change in surface properties. All the calculated doping levels stayed within the specifications given by the supplier ($1.4 \cdot 10^{15}$ $cm^{-3} \leq N_A \leq 2.8 \cdot 10^{15}$ cm^{-3}) except for native oxide.

In order to give an analysis of the fixed charge, a comparison is needed with the ideal flatband voltage. In an ideal metal-semiconductor interface the flatband voltage equals (Eq. 6):

$$V_{fb} = \phi_M - \phi_{Si} = \phi_{MSi} \tag{6}$$

The silicon work function ϕ_{Si} (expressed in Volts) is dopant dependent and equals for p-silicon (Eq. 7) [13]:

$$\phi_{Si} = \chi + \frac{E_g}{q} - V_p = \chi + \frac{E_g}{q} - \frac{kT}{q}\ln\left(\frac{N_V}{N_A}\right) \tag{7}$$

where E_g is the silicon bandgap energy (1.12 eV [13]) and N_V is the number of effective states in the valence band ($1.04 \cdot 10^{19}$ cm^{-3} for silicon [13]). All the following calculations depend on the tabulated value of $\phi_M = 4.49$ V for mercury [29]. With the average value of $N_A = 2.0 \cdot 10^{15}$ cm^{-3} it can be calculated that $V_{fb,theory} = \phi_{MSi} = -0.45$ V.

Positive charges in the insulator will shift ideal C-V and Mott Schottky curves to more negative values resulting in a more negative V_{fb} and vice versa.

If these theoretical values are compared with the measured values, the following can be said. All the insulators have their flatband voltage shifted in the positive direction, even beyond the theoretical V_{fb}, indicating the presence of negative charges at these interfaces. The amount of negative charges is the largest for native oxide, then C_{10} and then comparable values for the other monolayers. For the C_{16} and C_{22} layers it is now possible to calculate the total fixed charge in the insulator via Equation 8:

$$N_f = \frac{C_{ins}(\phi_{MSi} - V_{fb})}{qA} \quad (8)$$

where N_f [cm^{-2}] is the total number of fixed charges; C_{ins} [F] is the insulator capacitance as determined from the 1/C plots; ϕ_{MSi} and V_{fb} are the theoretical and measured flatband voltage, respectively. This gives the following values for N_f (Table 4). By definition, however, $N_f = |Q_f / q|$ and is always positive. To show that in all the cases listed in Table 4 negative fixed charges are concerned, this is denoted by $-Q_f$.

Table 4. N_f calculated for different insulators

Insulator	Total insulator charge N_f [cm^{-2}]
C_{16}	$5.4 \cdot 10^{11}$ ($-Q_f$)
C_{22}	$5.9 \cdot 10^{11}$ ($-Q_f$)
4.9nm SiO_2	$1.6 \cdot 10^{12}$ ($-Q_f$)

The values are compared with reference samples with 4.9 nm thermal oxide of which the J-V and C-V data are not given here. Despite better insulating properties than all of the tested insulators, the amount of fixed charge N_f, as calculated in the same way as for the C_{16} and C_{22} layers, was higher for the samples with 4.9 nm oxide.

State of the art MOS-structures have values of N_f in the order of 10^9 – 10^{11} cm^{-2} for (100) oriented silicon [30]. The samples with monolayers showed a remarkably low amount of interface charge, especially if one takes into account that these monolayers were fabricated using wet bench chemistry at low temperatures without any annealing step. The samples with 4.9 nm oxide gave a three times higher amount of N_f.

V. Conclusions

Organic monolayers covalently bound to p-silicon were successfully characterized via J-V and C-V measurements and the results were compared with native oxide insulators. It was demonstrated that all layers showed insulating behavior. The monolayers > C_{10} showed better insulating properties than native oxide. The J-V results showed a clear dependence on monolayer thickness, thereby increasing the effective barrier height ϕ_{eff}. This led to a determination of the tunneling constant for these monolayers which was found to be 0.45 $Å^{-1}$.

Capacitance measurements showed typical metal-semiconductor C-V behavior for samples with C_{10} and native oxide insulator. For C_{16} and C_{22} layers a plateau in accumulation was observed and this indicates the formation of a real capacitance. Analysis of this plateau yielded the dielectric constant of the monolayer, which varied from 1.7 ± 0.3 to 2.2 ± 0.4. Analysis of the Mott Schottky plots gave similar values for the flatband voltage for monolayers > C_{10}. This suggests similar interface properties for these monolayers. For the C_{16} and C_{22} layers the amount of fixed charge has been evaluated. This gave remarkably low values for Si-C linked monolayers on p-silicon ($5.4 - 5.9 \cdot 10^{11}$ cm^{-2}) as compared to samples with 4.9 nm thermal oxide ($1.6 \cdot 10^{12}$ cm^{-2}).

From the above results we conclude that from the electronic point of view, organic monolayers covalently bound to p-silicon offer a promising insulating material for molecular electronic devices. Moreover, given the virtually unlimited possibilities for chemical modification of the properties of the organic monolayers, we believe that such layers are a promising alternative for further downscaling of silicon devices.

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