

Application of PECVD a-SiC Thin-Film Layer for Encapsulation of Microstructures

V. Rajaraman, L.S. Pakula, H.T.M. Pham, P.M. Sarro and P.J. French

Abstract—In this paper, the feasibility of utilising a stress-optimised PECVD a-SiC layer for wafer-level thin-film encapsulation of microstructures is investigated. The concept, design, fabrication process and the results of PECVD a-SiC thin-film encapsulation are presented. Demonstrated results suggest that PECVD a-SiC can be successfully applied for thin-film encapsulation of microstructures. The presented zero-level packaging process is IC-compatible and it enables a smaller footprint and chip thickness compared to wafer-level packaging techniques employing wafer bonding.

Index Terms—Silicon Carbide, thin-film encapsulation, zero-level packaging, MEMS

I. INTRODUCTION

MICRO-ELECTRO-MECHANICAL SYSTEMS (MEMS), can be developed using standard semiconductor technology, that consist of sensors and/or actuators and their control circuitry. Using a carefully developed IC-compatible microfabrication technology, one can in principle integrate the mechanical element(s) and the IC monolithically, onto the same silicon substrate. On the other hand, unlike ICs, MEMS devices contain free-standing and/or moving parts with gaps and feature sizes in the range of a few microns that requires protection against dust, contamination and handling during backend processing such as dicing and assembly. Besides, some MEMS devices also require a stable and controlled environment for reliable operation. These challenging demands are usually fulfilled by means of packaging MEMS devices on the wafer-level using either wafer bonding or thin-film chip-scale encapsulation [1-4].

Although widespread, zero-level packaging using wafer bonding technique suffers from limitations in terms of size, cost and complexity. Hence, thin-film packaging of MEMS is currently being investigated worldwide as an alternative zero-level packaging method. In this technique, typically, a sacrificial material is deposited on top of the microstructures over which the encapsulation material is applied. Later, the sacrificial material is etched through the encapsulation layer to form a microcavity that is then sealed. Advantages of zero-

level packaging of MEMS by thin-film encapsulation are a smaller footprint and chip thickness, reduced process complexity and lower costs.

Several materials and processes are reported in the literature for thin film encapsulation of microstructures [1-4], each having their distinctive pros and cons. This work aims at exploring the feasibility of applying an IC-compatible, stress optimised plasma enhanced chemical vapour deposited (PECVD) amorphous silicon carbide (a-SiC) layer for thin-film encapsulation of microstructures. In the following sections, the process materials, the test structure design, the fabrication process and the results are presented.

II. PROCESS MATERIALS

Owing to the excellent material properties of PECVD a-SiC, such as high mechanical strength, ability to operate at high temperatures, resistance to harsh environment and extreme chemical inertness [5-7], it was chosen as the thin-film encapsulation material in this work. These properties when combined with IC-compatible low thermal budget processing, become even more attractive for thin-film MEMS encapsulation, especially for automotive, industrial and medical applications where devices are often subjected to harsh environments requiring a stable, durable and reliable encapsulation layer. For the encapsulation process, a low tensile stress PECVD a-SiC film devoid of pin-holes was developed in a Novellus Concept One plasma deposition system. The process parameters shown in Table 1 ensured the deposition of a pin-hole free, 65 MPa tensile stressed PECVD a-SiC layer at a post-IC processing temperature of 400 °C.

TABLE I
PECVD a-SiC DEPOSITION PARAMETERS

Parameter	Value
SiH ₄ Gas Flow	0.25 slm
CH ₄ Gas Flow	3 slm
Pressure	2 Torr
Temperature	400 °C
HF Power	450 W
LF Power	150 W

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An etch rate of 110 nm/min was obtained for SiC in Alcatel GIR300 plasma etch system using CF₄/SF₆/O₂:70 sccm/10 sccm/10 sccm, 500 mbar and 60 W. Proper etch selectivity was achieved against inorganic and organic sacrificial materials used in semiconductor technology like PECVD

oxides and polyimide, aluminium and silicon substrate using different etch chemistries.

III. CONCEPT AND DESIGN

The schematic shown in Fig. 1 illustrates the design concept of PECVD a-SiC thin-film encapsulated microstructures. The various parts of a thin-film packaged MEMS device, such as the encapsulation layer, microcavity and the possibility of integrating a top and bottom electrodes are clearly defined. In such a device, the function of PECVD a-SiC layer is two-fold. First, it has to hold the top electrode that is embedded beneath the PECVD a-SiC encapsulation membrane and second, it has to encapsulate and seal the microcavity defining the zero-level packaged environment for device operation. Such an encapsulation is suitable for small area microstructures such as cantilevers, resonators, bridges, etc. that are often used in MEMS devices.

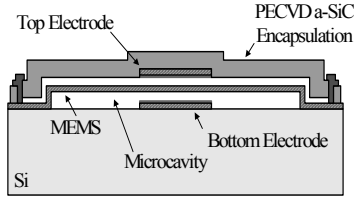


Fig. 1. Illustration of a PECVD a-SiC thin-film encapsulated MEMS structure

There are two major issues in the design and development of a thin-film encapsulation process. Firstly, the residual stress of the material being used for encapsulation need to be minimised and should preferably exhibit tensile stress so that the encapsulating membrane does not buckle/sag and is held intact when suspended. This aspect has been taken care of in the encapsulation process by tailoring the residual stress of the PECVD a-SiC layer. Secondly, the maximum deflection that is caused due to the pressure difference between the sealed cavity and the ambience, which again will introduce stress in the edges and the centre of the membrane, has to be optimised by choosing an appropriate thickness of the encapsulation material and the sacrificial layer, which when removed will later define the microcavity.

It is known from the plate deflection theory that the maximum deflection occurring at the centre of a free-standing, self-supported encapsulation membrane that is fixed on all sides can be obtained from Eqns. 1 and 2, respectively [8]. For a circular encapsulation membrane, the maximum deflection is given by:

$$d_{\max} = \frac{-3r^4 p(1 - \nu^2)}{16Et^3} \quad (1)$$

For a rectangular encapsulation membrane, the maximum deflection is given by:

$$d_{\max} = \frac{5pl^4w^4}{384 \frac{Et^3}{12(1-\nu^2)}(l^4 + w^4)} \quad (2)$$

where,

- d_{\max} – Max. deflection of the encapsulation membrane [μm]
- p – Differential pressure ($p_{\text{external}} - p_{\text{microcavity}}$) acting on the encapsulation membrane [mbar]
- ν – Poisson's ratio
- E – Young's modulus [GPa]
- l – Length of the encapsulation membrane [μm]
- w – Width of the encapsulation membrane [μm]
- t – Thickness of the encapsulation membrane [μm]
- r – Radius of the encapsulation membrane [μm]

This value was both calculated numerically and verified by FEM simulation using COMSOL for rectangular and circular shaped membrane geometries. Simulation results show that the maximum deflection for a $4\mu\text{m}$ thick, $200 \times 200\mu\text{m}^2$ PECVD a-SiC membrane is about 100 nm. This value was taken into account in the fabrication process, described in the next section, to ensure that the PECVD a-SiC encapsulation does not collapse onto the microstructure. In this study, several circular test structures ranging in size from $80\mu\text{m}$ to $150\mu\text{m}$ were designed and fabricated in order to explore the feasibility of applying PECVD a-SiC thin film layer for MEMS encapsulation.

IV. FABRICATION PROCESS

The surface micromachining fabrication process with integrated PECVD a-SiC encapsulation is presented in Fig. 2. In this process, aluminium is micromachined and used as the mechanical material as well as the electrodes. PECVD a-SiC is used as the encapsulation and sealing material. A 4% PSG doped PECVD oxide is used as the sacrificial layer due to the simple processing involved in its deposition and patterning by wet etching in an HF based etchant.

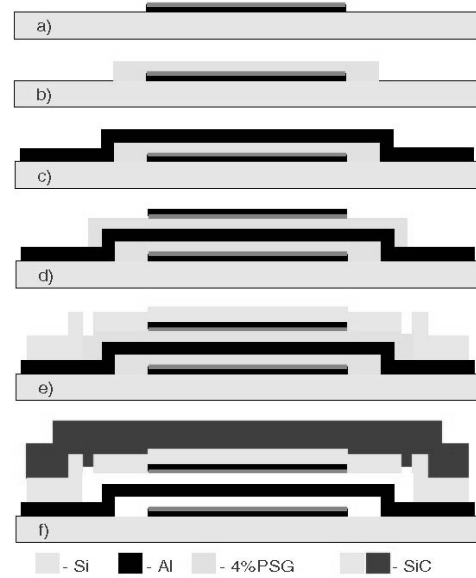


Fig. 2. Surface micromachining fabrication scheme with integrated thin-film PECVD a-SiC packaging

The post-IC fabrication process starts with sputter-coating Al

on a Si substrate isolated with nitride or oxide followed by the deposition of a 100nm PECVD a-SiC thin-film layer and then both layers are patterned (Fig.5a). The PECVD a-SiC thin-film layer is used to prevent stiction and to provide insulation between the electrodes and microstructure. Next, a 1.5 μm 4% PSG doped PECVD oxide sacrificial layer is deposited and patterned (Fig 5b). This step is followed by sputter-coating a 2.5 μm thick aluminium mechanical layer that is micromachined to form the MEMS structure (Fig. 5c). Later, a second 4% PSG doped PECVD oxide sacrificial layer is deposited and patterned (Fig. 5d). On the top of sacrificial layer, again a 100nm PECVD a-SiC insulating layer is deposited that is followed by sputter-coating of a 0.6 μm second aluminium layer. Both layers are then patterned forming a second set of electrodes. A pin-hole free, stress optimised, 4 μm PECVD a-SiC is then used for encapsulation. At first, a 2 μm PECVD a-SiC is deposited and patterned to create the first layer of encapsulation. Simultaneously, the etch-windows for sacrificial layer etching are opened (Fig. 5e). The structure is then released by removing 4% PSG doped PECVD oxide sacrificial layer in 73% HF (hydrofluoric acid) with addition of 2-propanol followed by freeze-drying with Cyclohexane to prevent stiction. Finally, a second 2 μm PECVD a-SiC sealing and encapsulation layer is deposited in order to close the etch-windows and to strengthen the encapsulation (Fig. 5f).

V. RESULTS AND DISCUSSION

Several circular PECVD a-SiC encapsulations ranging in size from 80 μm to 150 μm were fabricated using the presented process. The thickness of the test structures was fixed at 4 μm . In the following SEM micrographs, only the enclosed MEMS cavities are shown. The height of the microcavities was determined by the thickness of the sacrificial layer used.

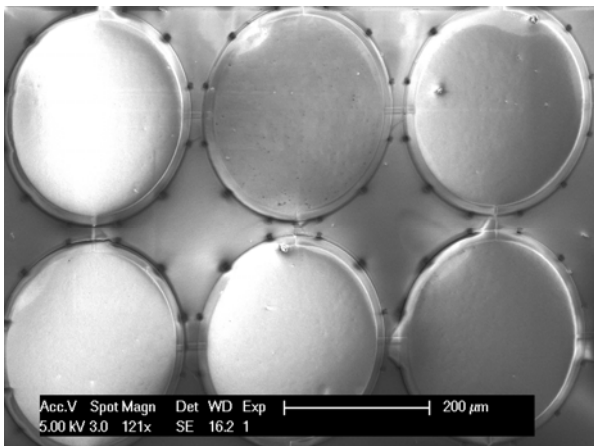


Fig. 3. An array of suspended circular PECVD a-SiC encapsulations

Fig. 3 presents an array of free-standing circular PECVD a-SiC thin-film encapsulation membranes after removal of the sacrificial layer. The release holes that were situated around the periphery of the membrane through which the sacrificial material was etched can also be seen in this SEM micrograph.

Detailed top-view of a cleaved PECVD a-SiC circular microcavity is shown in Fig. 4.

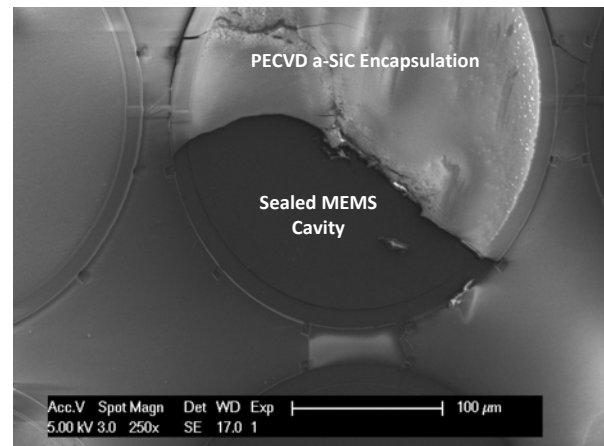


Fig. 4. Top-view of a cleaved circular PECVD a-SiC encapsulation

Fig. 5 presents a detailed cross-sectional view of a PECVD SiC encapsulated MEMS cavity showing the free-standing PECVD SiC encapsulation membrane.

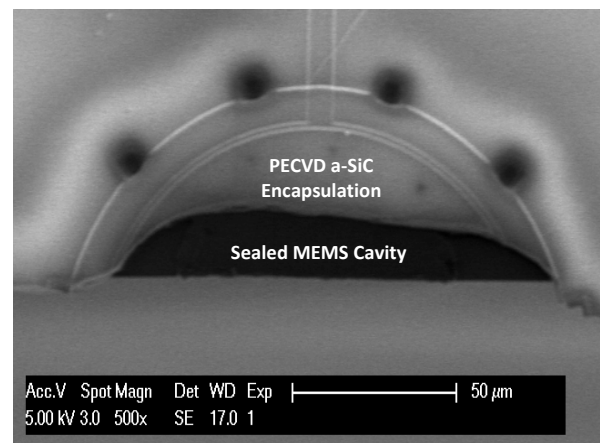


Fig. 5. Cross-section of a PECVD a-SiC encapsulated MEMS cavity

VI. CONCLUSIONS

The results of the feasibility study on the application of a stress optimised PECVD a-SiC layer for wafer-level thin-film encapsulation of microstructures were presented. Furthermore, the promising results demonstrate that PECVD a-SiC layer can successfully be applied for thin-film encapsulation of MEMS structures. The presented zero-level packaging process is IC-compatible and it enables a smaller footprint and chip thickness compared to wafer-level packaging techniques employing wafer bonding.

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