Verification of Mextram 504.6 in Verilog-A and C-code (SiMKit 2.1.1) implementation

A. Kautaniuk, H.-C. Wu, S. Mijalkovic, J. N. Burghartz

***Abstract*— Recently the Verilog-A became the aim for compact modeling standardization language. Provided Mextram implementation in Verilog-A follows all model modifications as well as SiMKit (C-code). Therefore to insure the users in correspondence and reliability of Verilog-A implementation of the model, the testing of equivalence and sufficiency of CPU time and electrical characteristics has been performed.**

***Index Terms*— Mextram model, SiMKit, Verilog-A**

I. Introduction

Verilog Hardware Description language (VHDL) was introduced for specifying and description of digital systems from behavior to structural abstractions [1]. VHDL became an international standard, regulated by the IEEE. Verilog-A is an high level language developed to describe the structural and behavior of analog systems and their components. Language structure is represented in the Language Reference Manual (LRM). Expanded Verilog-A simulation capability for analog and mixed signal systems is realized in Verilog-AMS. Recently the release of the Verilog-AMS LRM 2.2 had been introduced to the electronics community as an industry language standard. Within the LRM 2.2, Verilog-A provides great support to the compact modeling extension and is on the path to become the standard language of compact modeling.

What makes Verilog-A so attractive for compact modeling? The major benefit for preferring Verilog-A over general-purpose programming languages is that it frees the model developer from the burden of handling the simulator interface [2]. The compiler hides all complexities, while the model developers are focussed on getting correct equations. Compiled code is represented in binary format, that creates the protection of user's intellectual property. Ordinary model developer do not need programming skill to implement or modify the model, the language is reasonably simple and has optimized structure. The efficiency of Verilog-A simulators can be demonstrated in a automatical computation of symbolic partial derivatives of current and charges in compact model, whereas in C this work must be done by hand. Commercial, as well as open source interpreters and compilers provide user wide range of optional simulators, which support compiled code or Verilog-A. It has been verified that the compact models written in Verilog-A run as quickly and reliable as those hand-coded in C.

The Compact Modeling Council encourage the developers of candidate models for standardization to release model source code in Verilog-A. Phillips appears as one of those candidates for model standardization with their model for bipolar transistor - Mextram. The Technical University of Delft (TU Delft) had been chosen as support group and provider of Mextram Verilog-A implementation of in the future transition of whole model into Verilog-A. Created Verilog-A code follows all improvements and modifications of Mextram model as well as SiMKit. Taking into account that Verilog-A is relatively new technology and insure the users in correspondence and reliability of Verilog-A model performance, the verification of CPU time equivalence and sufficiency of electrical characteristics has been performed.

II. Mextram Implementation and Testing

A. Verilog-A

The Verilog-A Mextram 504 implementation is done directly following the model description in the Philips documentation [3,4]. With every release of Mextram model, corresponding modifications are performed in Verilog-A code. Current Verilog-A implementation corresponds to Mextram 504.6 release. The new features of Mextram 504.6, for instance introduction of new parameter dAI_S for tuning of Is_T, upper clipping value of Kavl and temperature limiting for self-heating, had been implemented in Verilog-A version. For user convenience by analogy with SiMKit Verilog-A source code consists of four models: bjt504t_va (with self-heating and substrate node), bjt504_va (with substrate node), bjtd504t_va (with selfheating) and bjtd504_va. To compile and convert from Verilog-A to simulator readable code two available compiles are used: the commercial Tiburon Design Automation Compiler which is included in circuit simulator ADS 2004A

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and open-source tool ADMS 2.0. This paper presents results obtained using compiler in ADS 2004A.

B. SiMKit (C-code)

SiMKit is a simulator-independent compact transistor model library. Simulator-specific connections are handled through so-called adapters that provide the right interfacing to Pstar, Spectre and ADS simulators. The SiMKit library contains the most recent versions of the Philips transistor models [5]. At the time of verification of the Mextram 504.6 Verilog-A implementation the C-code of model had been included in SiMKit 2.1.1. The compact transistor model library was attached to ADS 2004A, following instruction of Philips website. As it has been mentioned above, the SiMKit 2.1.1 supports four variations of Mextram 504 model: bjt504t, bjt504, bjtd504, bjtd504t.

It should be noticed that it takes some time between publication of modified Mextram and release of updated SiMKit version. However updating of Verilog-A code requires less effort and time as well as it is independent on a simulator.

C. Verification setups

The n-p-n type model with self heating and substrate node has been picked up for verification. To cover all branches of the model behavior the following set of tests has been created:

1) Capacitances (C_{BE}, C_{BC}, C_{SC})
2) Early forward and reverse (V_{EF}, V_{ER})
3) Gummel forward and reverse ($h_{FE}(I_B)$, $h_{FE}(V_{BE})$, $h_{FC}(V_{BC})$, β)
4) Output (g_{OUT}, $I_C(V_{CE})$, $V_{BE}(V_{CE})$)
5) S-parameters with bias sweep ($f_T(V_B)$, $f_T(I_C)$)
6) S-parameters with frequency sweep (Y_{11}, Y_{22}, Y_{12}, Y_{21})
7) Low frequency noise (noise current spectrum)
8) High frequency noise (noise voltage spectrum)
9) Transient analysis
10) Harmonic balance

The examination of the model respond on temperature has been done in temperature range from 25C to 150C with step of 25C. The sweep of some default parameters, shown in Table I, has been applied in addition to temperature.

The verification has been based on default values of model parameters as well as parameters extracted for DIMES 04 bipolar transistors with thin and thick epilayer at different flags. The tests has been run on commonly used ADS 2004A circuit simulator with established twelve significant digits. The addition tests based on amplifier, oscillator and mixer have been settled in order to avoid unreliable behavior of the model. As a degree of the discrepancy between two implementations, the relative error and CPU time are considered.

TABLE I
PARAMETERS SWEEP

Parameter	Start Value	Stop Value
C_{JE}	73 pF	153 pF
C_{JC}	78 pF	158 pF
C_{JS}	315 pF	495 pF
V_{EF}	44 V	68 V
V_{ER}	2.5 V	4.9 V
β_f	215	315
β_{ri}	7	14
I_k	0.1 A	1 A
τ_e	2 ps	14 ps
τ_b	4.2 ps	8.4 ps

III. RESULTS AND DISCUSSION

The results of verification are represented in this section. As the measure of discrepancy of model implementations the relative error of simulated electrical characteristics is considered. The Fig.1 shows the maximum relative error of simulation results at default, as well as DIMES04 (thin and thick epilayer) parameters sets for listed above test setups.

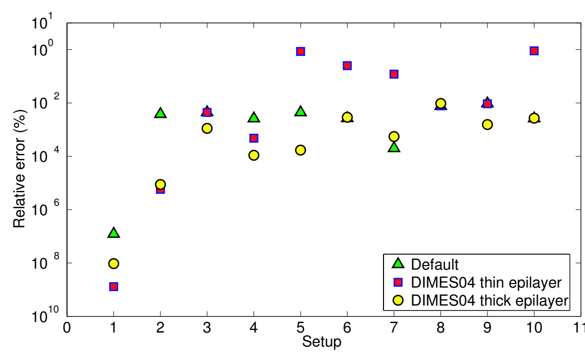

Fig. 1. Maximum relative error at default, DIMES04 thin epilayer and DIMES04 thick epilayer parameters sets at temperature of 25C

Increasing of the temperature and application of parameter sweep (see Table.1) lead to the error rise on 10% of represented values. It should be noticed the error doesn't exceed the value of 0.1%, except the cases when the calculations of first and second order derivatives at high frequency and current level are involved, then error may reach the value of $1 \sim 3$ %. To control Verilog-A implementation respond on simulations with involvement of high order (third and fourth) derivatives, the signal mixer has been tested. On request of designer group, the design of mentioned mixer may not be shown. However the results of mixer simulations are represented on Fig.2. As it can be seen the level of discrepancy in this case is very high and can reach 100%. It is significant do not consider this

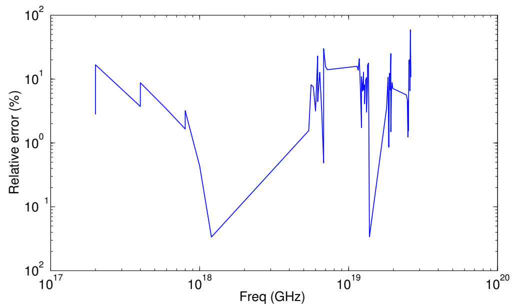

Fig. 2. Mixer output characteristics error

example as failure of Verilog-A implementation. The reason is in the way of derivatives representation in both implementations. In SiMKit all derivatives are hand written, while in Verilog-A version their computation is performed in compiler and not traceable from the outside. For further action, the way of computation of derivatives in Verilog-A version should be reconsidered, as well as comparison of both versions have to be done with experimental results. TU Delft is currently working on this issue. At this point we can be quite convinced in reliable performance of Mextram Verilog-A implementation. Our next step is to take a look at speed of performance of two implementations. Table II represents the CPU time for default parameter set at temperature of 25C. To settle doubt that represented

TABLE II

CPU TIME FOR DEFAULT PARAMETER SET AT 25C

Setup	Verilog-A (s)	SiMKit 2.1.1 (s)
1	1.1	1.5
2	1.0 / 1.0	1.4 / 1.5
3	1.2 / 1.0	1.5 / 1.6
4	1.7	1.6
5	7.6	8.3
6	1.0	1.3
7	2.1	2.1
8	1.2	1.6
9	1.1	1.6
10	2.2	2.4

tests cannot describe real CPU time, the results of running the special setups, provided by Philips, had been taken into consideration. According to obtained results the Verilog-A version shows 38.8 sec versus 45.8 of SiMKit 2.1.1 at 25C and 39.3 sec versus 45 sec at 300C. It has been mentioned that verification setups should cover all branches of the model behavior, therefore the additional high frequency oscillator test has been settled.

The schematic of tested 10GHz oscillator is depicted on Fig.3. Based on obtained results relative error, shown on Fig.4, the conclusion about significant and

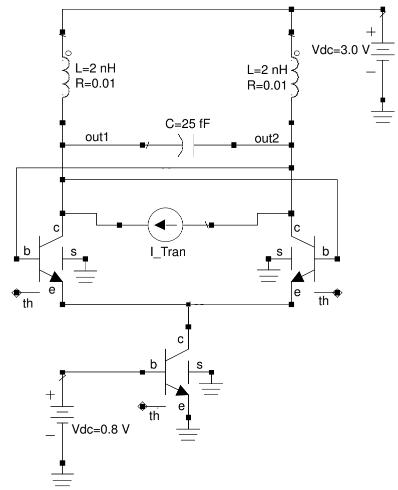

Fig. 3. Oscillator at 10 GHz

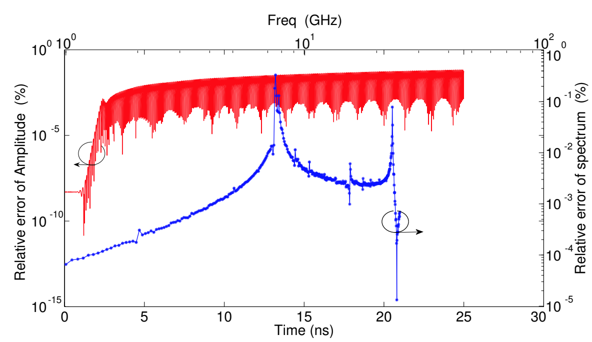

Fig. 4. Maximum relative error for oscillator outputs

reliable performance of Verilog-A implementation at high frequencies can be made. Some attention had been paid to noise implementation and verification. It should be noticed that Verilog-A and SiMKit 2.1.1 noise implementation is different. The fundamental difference lays in implementation of correlation between base and collector current noise sources due to avalanche. Verilog-A correlated noise implementation was done following [6]. Fig.5, 6 and Fig.7, 8 show the low and high frequency noise setup and errors.

IV. CONCLUSION

In conclusion we would like to mention that the result the CPU time is comparable and general discrepancy of electrical characteristics remains in range of $10^{-3} \sim 10^{-1}$ %. Simultaneous updates of Verilog-A code with C-code in SiMKit achieve accuracy in prediction of the Mextram electrical quantities. Therefore adequacy of Mextram 504.6 in Verilog-A code allows users to use Verilog-A implementation on SiMKit 2.1.1 level.

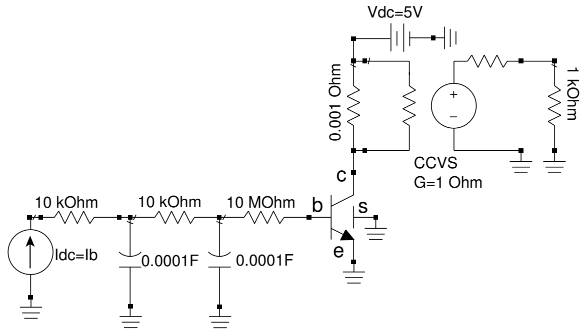

Fig. 5. Low noise frequency circuit

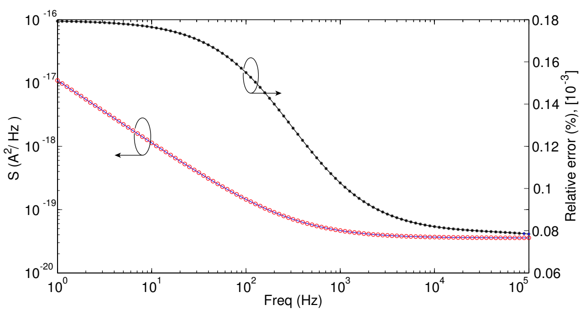

Fig. 6. Low noise frequency output and error

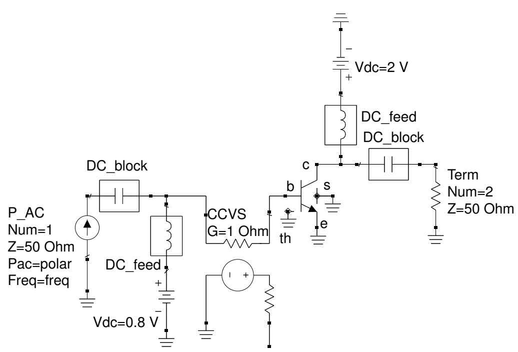

Fig. 7. High frequency noise circuit

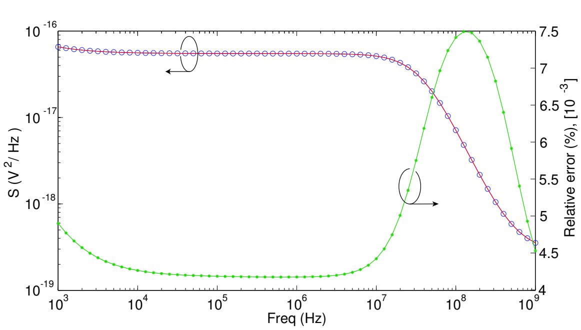

Fig. 8. High frequency noise output and error

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