Translinear Networks from a Combinatorial Viewpoint

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Abstract—**A formal, graph-theoretic perception of translinear circuits is introduced. Based upon this, the exhaustive generation of all possible network topologies for static translinear circuits with a small number of transistors is proposed, leading to a "brute force" synthesis approach.**

Keywords—**translinear circuits, topology generation, analog electronics**

I. Introduction

Translinear circuits form a very special but popular class of analog circuits. A systematic approach to their design has been developed by Mulder et al [6]. One part of the design trajectory is the so-called *translinear decomposition* of polynomials, but only for the case of a single translinear loop do satisfactory algorithms exist (*non-parametric decomposition*) [6][4]. For circuits with more than one translinear loop a similar algebraic approach does not seem possible.

As a replacement, this paper introduces the idea of a complete computer-generated catalog of admissable topologies for "small" translinear networks ("small" meaning "consisting of few transistors"), inspired by the observation that on the one hand translinear networks are almost completely specified by their topology while on the other hand the topology itself must satisfy strong constraints.

A catalog of topologies is easily equipped with prototype network equations for each topology. Along with techniques for automatic searching and matching of polynomials, it can serve as a powerful tool for the synthesis of translinear networks.

This paper is organized as follows: Section II very briefly reviews the functional principle of translinear networks. In Sections III and IV, a combinatorial perception of static translinear networks is developed. Section V contains some additional remarks, in particular on the extension of the developed conceptions for dynamic translinear networks. Section VI reports about successes in the combinatorial generation of topologies, followed by the conclusions in Section VII.

Throughout the paper, the translinear squaring network depicted in Fig. 1 will serve as an example.

II. Review of the Translinear Principle

Every translinear circuit relies on the so-called *translinear principle* [3][2] that applies to certain loops formed by devices that can be modeled by an exponential relationship between voltage and current. In the standard case of bipolar npn transistors, these so-called *translinear loops* are formed by base-emitter branches in such a way that there are equally many branches oriented in each of the two loop directions (called "forward" and "backward", where these notions of course depend on the choice of some "canonical" loop orientation).

The loop marked by heavy blue lines in Fig. 1 is an example for a translinear loop.

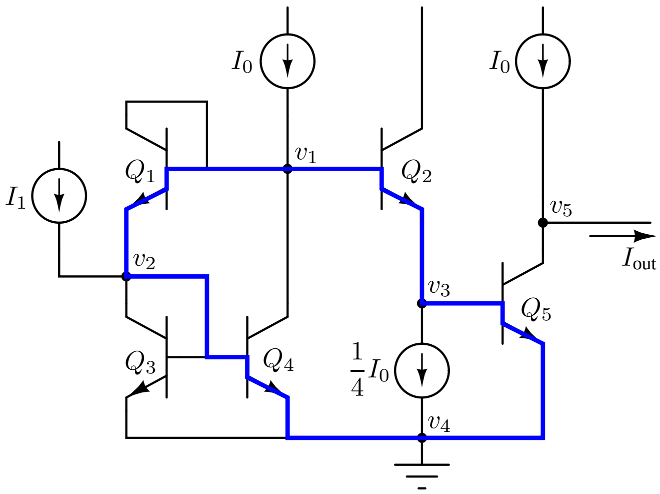

Fig. 1. A translinear squaring network [10].

If the device parameters (saturation current and thermal voltage) are the same for all transistors involved, one can translate the voltage law, using the exponential voltage-current relationship, into an equation of the form

$$I_1 \cdot I_3 \cdot \dots \cdot I_{2r-1} = I_2 \cdot I_4 \cdot \dots \cdot I_{2r}, \qquad (1)$$

where $2r$ is the number of transistors forming the loop and $I_1, \dots, I_{2r}$ are their collector currents. (In eqn. (1) it is assumed that the base-emitter branches of all transistors with an odd index are oriented, say, "forward", and that the base-emitter branches of all transistors with an even index are "backward".)

When considering translinear circuits, it is common to assume that the base currents of the transistors are zero. In the network of Fig. 1, incorporating this assumption into the current law and taking into account the current mirror Q_3-Q_4 (which can be considered as a minimal translinear loop), the equation of the highlighted translinear loop can be written as

$$\frac{1}{2}(I_0 - I_1) \cdot \frac{1}{2}(I_0 + I_1) = \frac{1}{4} I_0 \cdot (I_0 - I_{\text{out}}),$$

so $I_{\text{out}} = I_1^2 / I_0$.

III. TRANSLINEAR GRAPHS

Seevinck [10] introduced the concept of a *translinear graph* to capture the core of a translinear network that consists of the base-emitter branches of the transistors involved in translinear loops. The following is a refinement of Seevinck's definition:

Definition. *A translinear graph is a biconnected directed multi*[1]*graph, each loop of which consists of as many forward branches as backward branches.*

The requirement of biconnectedness is included in the definition because otherwise it is more convenient to consider separate circuits, corresponding to the biconnected components of the graph. (A directed or undirected graph is called *biconnected* if it is connected and remains so after removal of an arbitrary node.)

As an example, Fig. 2 shows the underlying translinear graph of the squaring network in Fig. 1.

The following theorem was implicitely used by Seevinck, but the explicit formulation as a mathematical theorem is apparently new.

Theorem 1. *Let G be a directed graph. The following statements are equivalent:*
1. *Every loop of G consists of as many forward branches as backward branches.*
2. *The node set of G can be partitioned into* level sets *$V_0, \dots, V_R$ such that every branch points from a node in some V_i to a node in V_{i-1}.*

The concept of level sets is illustrated in Fig. 3.

[1]The prefix *multi* is used here to emphasize that parallel branches, reflecting current mirrors, are allowed in a translinear graph.

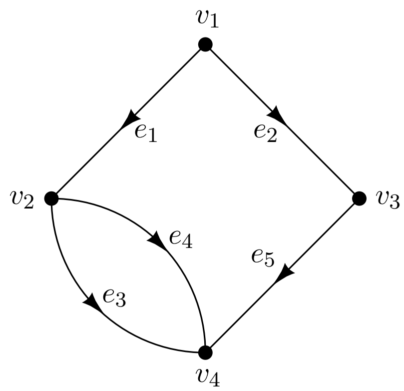

Fig. 2. The translinear graph of the network in Fig. 1. The base-emitter branch of each transistor Q_i is denoted by e_i.

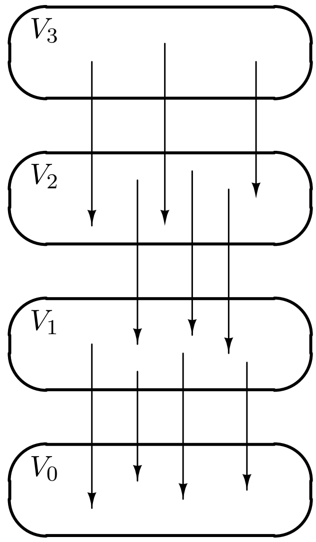

Fig. 3. Illustration of level sets.

Theorem 1 tells that a translinear graph is nothing but a biconnected directed graph having level sets. It can be regarded as a consequence of the fact that the node-branch incidence matrix and the transposed loop-branch incidence matrix form an *exact pair of matrices* [11, p. 41][1, Thm. 2.3 and Thm. 2.4], but a direct proof of Theorem 1 can easily be derived as well.

Obviously, for a node v of a translinear graph G, the unique index i with $v \in V_i$ is called the *level* of v. In Fig. 1 and Fig. 2,

$$\begin{aligned} \text{level}(v_4) &= 0, \\ \text{level}(v_2) &= \text{level}(v_3) = 1, \\ \text{level}(v_1) &= 2. \end{aligned}$$

The level of a node can be interpreted as a kind of abstract potential: If w, v are nodes of G with $\text{level}(v) > \text{level}(w)$, then in any translinear network that employs G as its core topology, the potential of v is always higher than the potential of w. This enables the formulation of the precise condition where collectors can be connected to in a translinear network, as is done in the following subsection.

IV. Connection of Collectors

If a translinear graph G is fixed, the next step towards a complete network description is to specify how to connect collectors. For each transistor Q, there are two possibilities:

- The collector of Q can be connected to a node v of G, if v is of higher potential than the emitter node v_E of Q, that is, if $\text{level}(v) > \text{level}(v_E)$. In Fig. 1, the collectors of Q_1, Q_3 and Q_4 are connected in this way.
- If the collector of Q is not connected to a node of G, it is formally considered as a (current-mode) output of the network. This implies collectors that are actually used as outputs as well as "unused outputs" such as collectors which are directly connected to a power source. In Fig. 1, the collectors of Q_2 and Q_5 are formal outputs, the case of Q_2 is an example for an "unused output".

The inputs of a translinear network are applied (in current-mode) to the nodes of the translinear graph. The actual arrangement, which input is applied to which node, is not considered as a part of the formal network description but as a matter of interfacing the network. The same is true for the selection of a ground node and also for the possible addition of supplementary nodes for output offset compensation, like v_5 in Fig. 1.

Thus a static translinear network is completely specified by

- a translinear graph G, encoding the base-emitter connections, and
- a *collector assignment C on G*, which assigns to each branch e of G either the special symbol v_{out} (which does not need to correspond to an actual node), indicating an output collector, or a node v of G that has a higher level than the terminal node of e. (Note that e corresponds to a transistor, and the terminal node of e to the transistor's emitter node.)

In the example circuit of Fig. 1,

$$
\begin{aligned}
C(e_1) &= v_1, \\
C(e_2) &= v_{\text{out}}, \\
C(e_3) &= v_2, \\
C(e_4) &= v_1, \\
C(e_5) &= v_{\text{out}}.
\end{aligned}
$$

V. Remarks

A. Filters for "relevant" networks

Not every formal collector assignment C leads to a network of practical value. For example, because the base currents are in reality not equal to zero, a node of the translinear graph to which no emitters are connected (such a node can be characterized as a *source* in the translinear graph), requires that at least one collector is connected to it. (Also, an input must be applied to that node, but this cannot be expressed in the collector assignment. Incidentally, inputs must also be applied to nodes where no collector is assigned to, like v_3 in Fig. 1.) Collector assignments not fulfilling this condition can be filtered out automatically.

Obviously, a network without any output is of no use. Therefore, only collector assignments with $C(e) = v_{\text{out}}$ for at least one branch e are to be considered.

For the rest of this paper, collector assignments and the resulting networks fulfilling the two conditions mentioned in this subsection will be called "relevant".

B. Construction of Network Equations

If a formal description of a translinear network is given in terms of a translinear graph and a collector assignment, the system of network equations, consisting of the translinear loop equations and the node equations, is easily written down, by hand or automatically, if for each node v, an independent input current I_v applied to v is assumed.

C. Extension for Dynamic Translinear Networks

In the formal context established by the previous sections, a *dynamic translinear network* [6] is just a static translinear network where one or more capacitors have been inserted between arbitrary nodes of the translinear graph. Thus, the topology of a dynamic translinear network can be formally described by

- a translinear graph G,
- a collector assignment C on G,
- and a *capacitor graph* G_{cap}, which is an undirected graph (containing no parallel edges) with the same node set as G.

Note that while static translinear networks are entirely described by the discrete information consisting of the pair (G, C), the triple (G, C, G_{cap}) is not a complete description of a dynamic translinear network, because the capacitances themselves remain as continous parameters.

D. Independence of Device Model

It is worth to note that the notions of a translinear graph and of a collector assignment are independent of the

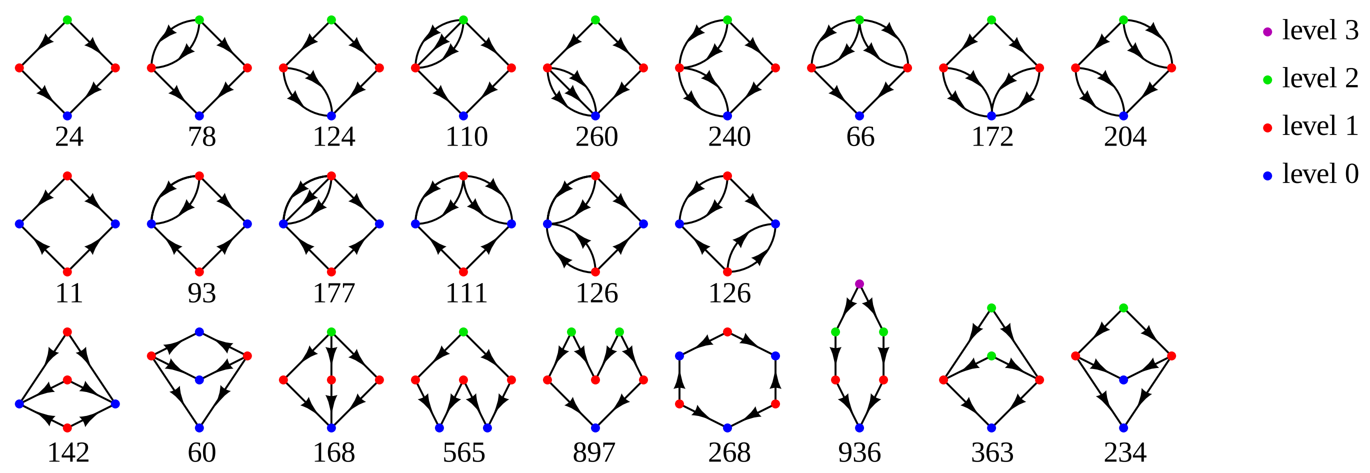

Fig. 4. The translinear graphs with 6 or less branches, and the numbers of "relevant" collector assignments that exist for each of them.

transistor model assumed. So, in principle, these concepts can also be used for the class of *voltage-translinear* circuits [3][7][8] .

VI. Results

Combinatorial algorithms based on *orderly generation* [9] have been developed to generate complete (but non-redundant) lists of topologies for static translinear networks, in terms of translinear graphs and collector assignments as derived in sections III and IV. The algorithms have been successfully applied to list all translinear graphs and collector asignments for up to 9 transistors. Fig. 4 and Table I show some counting results.

number of transistors	translinear graphs	translinear networks	"relevant" networks
4	2	63	35
5	3	418	295
6	19	8231	5189
7	39	144903	97323
8	174	3456428	2210492
9	559	98519914	62325782

Table I. Numbers of translinear graphs and networks with few transistors.

For all "relevant" networks, prototype network equations and netlists have also been generated.

Generation of topologies for dynamic translinear networks has so far not been attempted, because the number of possible topologies seems to be very large.

Systematic methods are under development to search the lists for a network whose behaviour matches a given polynomial of input and output currents and to find suitable arrangments to interface the network.

VII. Conclusions

In this paper, we have provided a precise graph-theoretic formulation of admissible topologies for translinear networks.

Complete lists of these topologies for static translinear networks with up to 9 transistors have been compiled. To turn such lists into a useful design tool, algorithms for symbolic matching of polynomials are in development.

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