

Optimizing Chemical Mechanical Polishing process in 3D-IC

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Abstract—In this paper we describe the optimization of chemical mechanical polishing process in three dimensional integrated circuits project. CMP is key technology in IC fabrication process to avoid lithography limitations, electro-migration problems and limitations in the number of the metal layers. After fabricating first active layer, 1.5 μ m TEOS oxide is deposited on this layer. Then using CMP system the step heights of first layer is polished away very slowly in order to have a complete uniform and smooth layer of oxide. The roughness of surface is less than 5nm confirmed by AFM. Second silicon layer is deposited and crystallized using μ -Czochralski process in order to make TFTs on the second layer. The electrical and physical characteristics of silicon layer and fabricated devices on planarized surface show similar results of first layer.

Index Terms—CMP, TFT, Excimer Laser Crystallization, 3D-IC

I. INTRODUCTION

CHEMICAL MECHANICAL POLISHING IS one of the critical steps in IC processing. The higher resolution of lithography and dry etching, increasing the number of metal layers and also no step coverage concerns are benefits of planarized surfaces [1]. In this paper we will describe the process of CMP in order to polish the step heights coming from previous layers and some hillocks that created during laser crystallization. The results show there are significant improvements in the electrical characteristics of TFTs and in the quality of crystalline silicon layer. The silicon layer is crystallized using μ -Czochralski process [2,3].

In μ -Czochralski process a locally increased thickness of the a-Si film, coated on oxide that have some holes, is used. The structure is irradiated with excimer-laser light, having an energy density above the complete melt threshold of the surrounding thin a-Si film. With this condition, at the end of the laser pulse, a residual fine grain poly-Si will be left at the bottom of the Si column (grain filter). The un-melted Si will subsequently act as a seed for the grain growth. The diameter or the depth of the thick Si will be so narrow or deep that one grain will be selected during the vertical growth phase. This enables us to precisely control the position of a single grain in excimer laser crystallization. [3]

Thin film transistors are made inside of grains. The

mobility of transistors is quite high inside grain. For n-type TFTs, 600cm²/VS and for p-type TFTs, 300cm²/VS mobilities are obtained in bottom layer.[3]

II. EXPERIMENTAL SETUP AND PROCEDURE

A. CMP Process

CMP process is done in MECAPOL E460 system. The calibration of back pressure, down force, rotation speeds, slurry flow rate and polishing times are the main parameters of this system. We have used Suba 500 as a hard and main polishing pad and then to smooth the surface, Politex Supreme as a soft polishing pad is employed. With this polishing process we could obtain the roughness of 5nm that confirmed by AFM. For slurry, diluted Nalco 2350 with 1:20 concentration is used. The average removing rate for poly silicon with 60rpm rotation speeds of both platen and wafer carrier, is 230nm/min and for silicon dioxide is 140nm/min.

The cleaning steps are very important after polishing. Immediately after polishing, the wafers are washed with DI water and are kept wet. We have developed a process to clean the wafers after CMP. It consists of RCA1, brushing and finally RCA2. To keep the wafers hydrophilic, in case of silicon polishing, and remove slurry particles, RCA1 for 40min at 85°C is used. Then after washing the wafers with DI water brushing is used to remove mechanically the slurry particles. During brushing diluted ammonium hydroxide is used to increase the PH of solution. Diluted BHF is also used to help brusher to get rid of particles. Finally to clean the metallic contaminants standard RCA2 for 10min at 75°C is used.

B. Fabrication steps

In this run we want to see the quality of silicon layer on polished and un-polished surfaces.

In figure 1 top left we can see some of the patterns in first layer before top silicon crystallization. The dots in the images are location of grain filters that crystallization starts from bottom of these holes. After Excimer laser crystallization of unpolished surface with 1200mJ/cm² some non-location controlled grains can be seen (Fig. 1 top). On the other hand on polished surface all grains are regular (Fig. 1 bottom). It means at low energy silicon in some area of edges is still solid and acts as a seed for crystallization. While on polished surface there is no un-melted area and all the grains are location controlled.

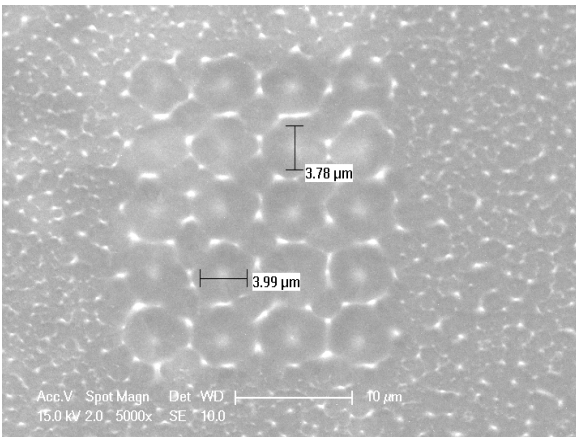
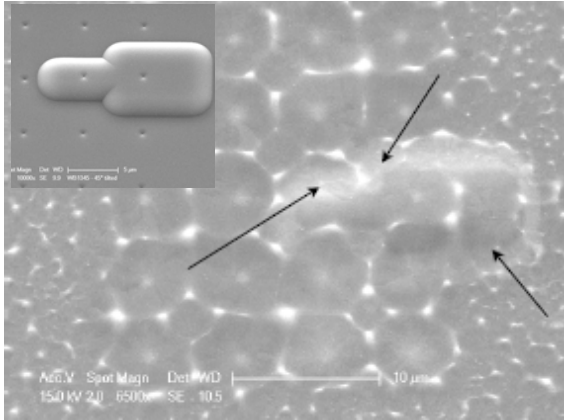


Fig.1: Comparing silicon single grains on polished (bottom) and non-polished (top) surfaces in 1200mJ/cm²

We did a finite element simulation to see the extra heat on bottom devices during laser crystallization of second silicon layer. The simulation shows with 1200mJ/cm² the bottom devices will experience 350°C more heat during top silicon crystallization (Fig.2, 3). In this simulation the laser energy is considered to be as a heat source on top silicon for a limited time.

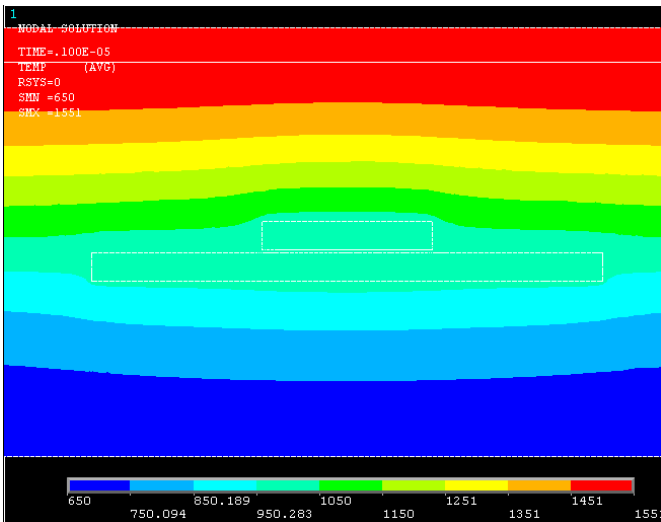


Fig.2: The heat contours: Bottom devices will experience 350°C more heat during top silicon crystallization

From Fig.3 it can be seen that at 1μs from laser irradiation the maximum heat meets the bottom transistors. The silicon thickness is 250nm and silicon dioxide between two layers is 1.6μm.

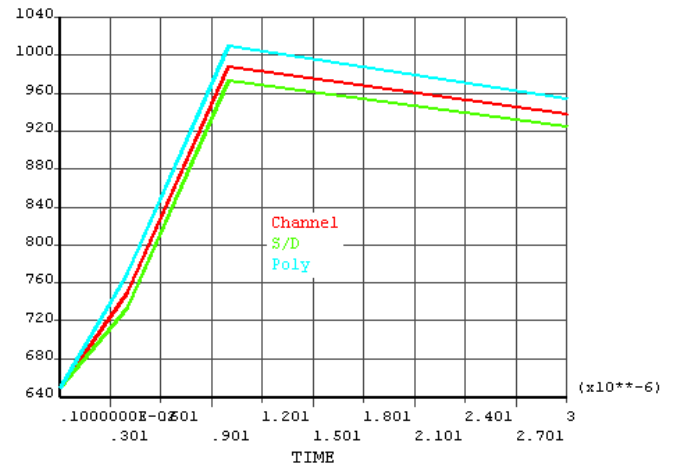


Fig.3: Heat distribution on channel, source and drain regions of bottom devices during top silicon crystallization

With increasing laser energy to 1600mJ/cm² there is no difference between grains on polished and non-polished surface (Fig. 4).

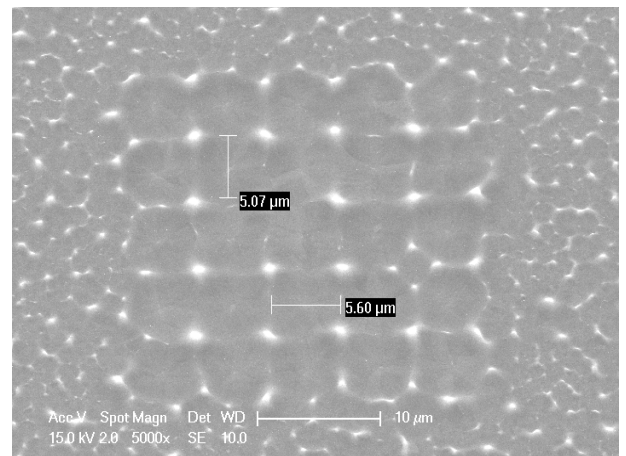
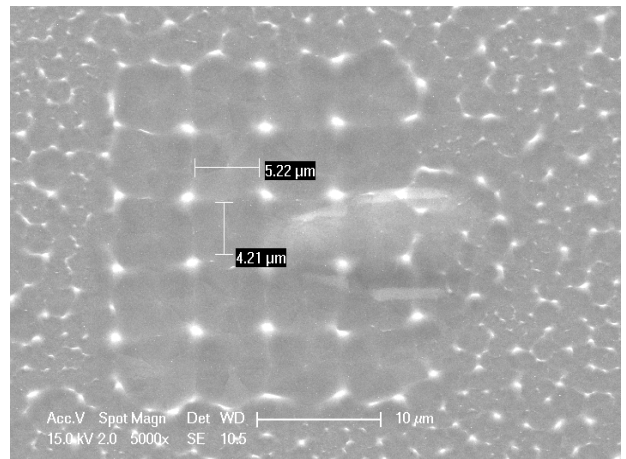


Fig.4: Comparing between silicon single grains on polished (bottom) and non-polished (top) surfaces in 1600mJ/cm²

These results show in order to prevent degradation of bottom devices (including poly gate and source/drain dopants redistribution) lower laser energy is preferred. Therefore CMP is very important step in order to have a regular and location controlled silicon grains.

The fabricated TFTs on top polished silicon layer show similar electrical characteristics of bottom layer. The family of Id-Vg and Id-Vd curves is shown in Fig. 5 for both n-MOS and p-MOS transistors. The effective mobility for nMOS and pMOS transistors is $565\text{cm}^2/\text{VS}$ and $159\text{cm}^2/\text{VS}$, respectively.

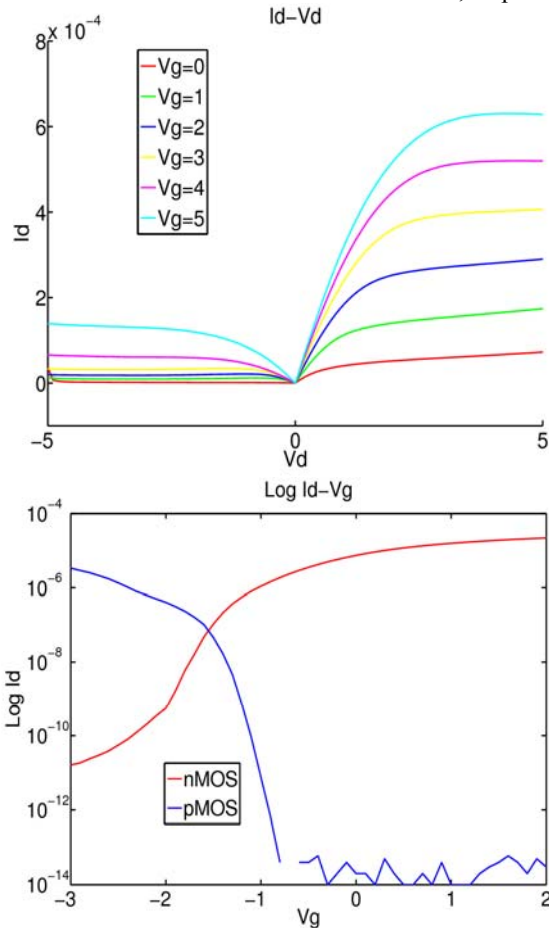


Fig.5: Fabricated TFTs on polished surface show similar performance of bottom devices.

The next attempt is to remove the hillocks of silicon between two grains after laser crystallization. Fig.6 top illustrates these hillocks. Their height is about $1\mu\text{m}$. We tried to polish these hillocks by soft polishing at short time by CMP. The SEM images show these hillocks are removed and illustrated in Fig. 6 bottom. After cleaning of samples and making thin film transistors, the output characteristics show improvement of leakage current and threshold voltage after removing these hillocks. More investigation is under way.

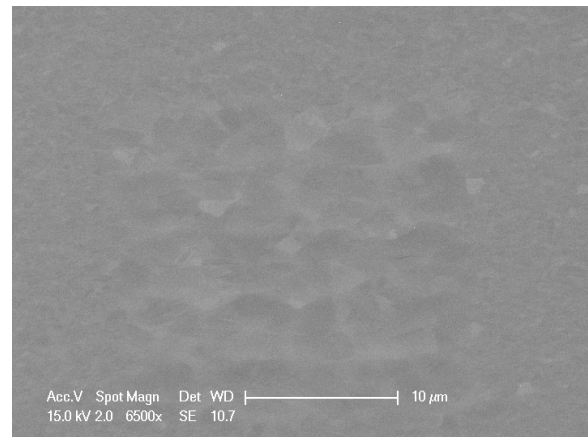
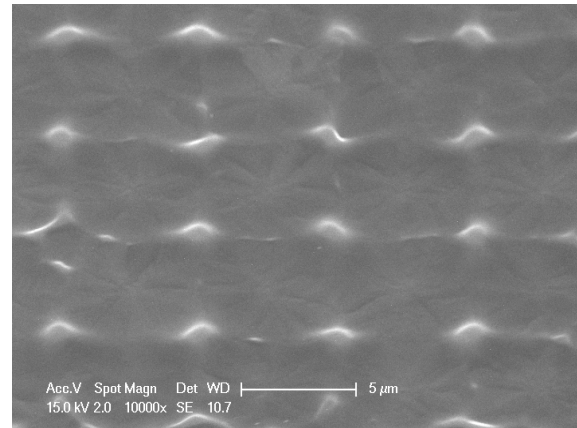


Fig.6: Removing the hillocks from crystallized silicon surface by CMP

III. CONCLUSION

We have investigated CMP process in three dimensional integrated circuits. CMP reduces the energy of excimer laser for silicon crystallization and it gives location controlled growth. It improves the interface between silicon and gate oxide with removing the silicon hillocks after laser crystallization. This improves the threshold voltage and leakage current of TFTs.

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