

# THREE-DIMENSIONAL IC'S PROLONG THE LIFE OF MOORE'S LAW

I. Brunets, A. Boogaard, G. I. Isai, A.A.I. Aarnink, A.I. Kovalgin, J. Holleman, J. Schmitz

**Abstract—** In this work we make steps forwards developing a low-temperature technology intended for the fabrication of 3-D structures. Several technology steps like low-temperature deposition of semiconductor and dielectric thin films, laser crystallization and planarization are described and discussed regarding the process characterization.

**Index Terms—** 3-D memory, ICPECVD, low-temperature CVD, thin film, silicon

## I. INTRODUCTION

One of the challenges in today's semiconductors technology is the problem of densification in integrated circuits. The incredibly growing market for "pocket" electronic products, such as mobile phones, digital cameras, MP3 players, data storage devices, notebooks, etc. creates a great demand for low-cost, low-dimension and low-power consuming memories (SRAM, DRAM, EPROM, EEPROM, flash memories etc.). With decreasing device dimensions, the length and density of interconnects is increasing. So the factors which were negligible in the past (e.g. RC delay), become increasingly important for the functionality of IC's, as well in following the Moore's Law [1, 2]. The number of metal layers extremely explodes in high conducted 2-D integrated circuits and within next years become significantly larger than International Technology Roadmap for Semiconductors projection [3].

One of the solutions is to replace the large number of horizontal long metal interconnects by vertical short ones, i.e. to transform the 2-D structure to a 3-D structure by increasing number of active functional layers. The three dimensional integration offers considerable improvement of speed, power consumption, size, weight, and costs. Such "vertical growth" of IC's could be arranged in different ways. For instance, hybrid manufacturing, wafer stacking (can be considered as an extension of 2-D technology), and using a multilayer thin film network produced on one base substrate (so called "System-on-Chip" fashion). The latter method seems to be very promising especially for producing of memory devices [4].

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I. Brunets, A. Boogaard, G. I. Isai, A.A.I. Aarnink, A.I. Kovalgin, J. Holleman, J. Schmitz are with MESA+ Research Institute, Chair of Semiconductor Components, University of Twente, Hogekamp, P.O. Box 217, 7500 AE Enschede, The Netherlands. Phone: +31 (0)53 489 4394; fax: +31 (0)53 489 1034; e-mail: [i.brunets@utwente.nl](mailto:i.brunets@utwente.nl)

The most important precondition in "System-on-Chip" technology is producing devices with the required quality top layers but without using high-temperature budgets. This is to avoid a strong impact on the underlying structures fabricated in the lower layers. Consequently, the conventional process flows, used to realize the underlying devices, can not be applied for the manufacturing of the upper layers in 3-D structures.

In order to decrease the thermal budget, low-temperature technology steps are required for deposition of silicon, silicon oxide and silicon nitride films. Furthermore, a local thermal treatment of silicon without vertical heat diffusion is required, preventing a degradation of the devices in the underlying active layer.

## II. EXPERIMENT CONCEPT

### A. Low temperature deposition

To satisfy the growing demand on the low temperature technology, new remote plasma enhanced chemical vapor deposition tool was developed and realized.

Our inductively coupled remote plasma enhanced chemical vapor deposition (ICPECVD) reactor is aimed at deposition of poly-Si and  $\alpha$ -Si layers, as well as silicon oxide ( $\text{SiO}_2$ ) and silicon nitride ( $\text{Si}_3\text{N}_4$ ) films. The substrate deposition temperature could be reduced down to 100-150°C. The schematic drawing is shown (Fig. 1) and detailed description of the reactor is given in [5].

In our reactor, the bombardment of the substrate with high energy ions is minimized because the substrate is located outside of the plasma-generation area. This advantage of the system allows us to keep the temperature of substrate comparably low. The additional precise chuck temperature control is realized.

Deposition process could be carried in two modes:

- *first deposition mode*: non-deposition gases (or a subset of the required deposition gases) are flowed through the plasma zone. Excited neutral atoms, radicals, ions, and electrons flow in the downstream direction towards the diffusion chamber, where additional precursors are injected. The energy transfer between the activated neutrals and the precursors results in the dissociation of the precursors. The entire mixture is further transported to the substrate. For example, the deposition of silicon nitride ( $\text{Si}_3\text{N}_4$ ) can be accomplished by flowing  $\text{Ar}/\text{N}_2$

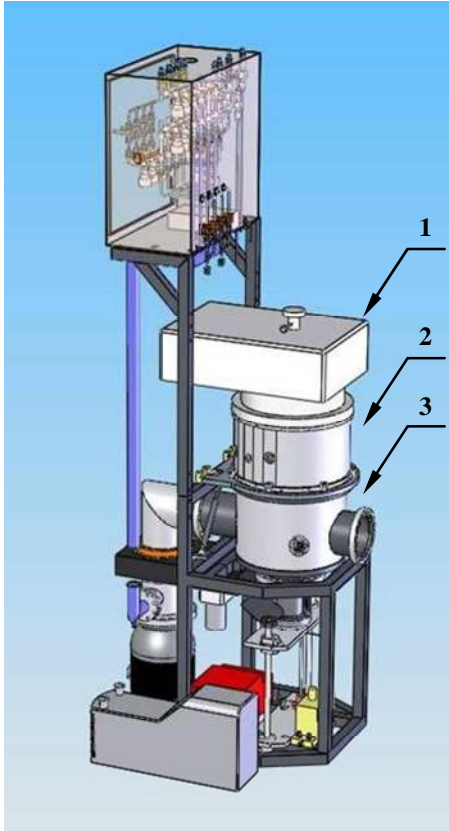


Fig. 1. Remote plasma ICPECVD reactor: (1) ICP source, (2) diffusion chamber, (3) reaction chamber.

mixtures through the plasma zone, and injecting  $\text{SiH}_4$  downstream (i.e. in the plasma afterglow region);

- *second deposition mode*: the system operates as atomic layer deposition (ALD) tool. Gaseous precursors and inert gases are introduced in the plasma subsequently to deposit the thin film layer-by-layer.

The presented reactor construction provides a large number of benefits and gives the possibility of a better control over the radical fluxes compared to a conventional PECVD.

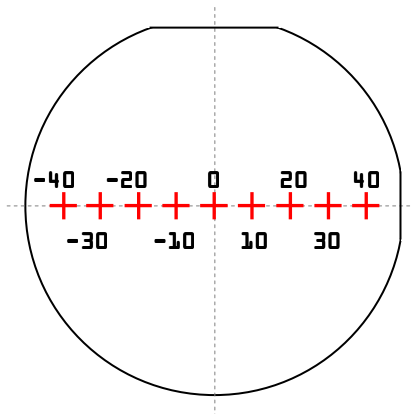


Fig. 2. Location of the test points on the wafer.

TABLE I  
POLISHING PROGRAMS

Polishing program № <sup>a</sup>	Rotation speed of the head with wafer carrier, [rpm]	Rotation speed of the pad, [rpm]
P-01	40	20
P-02	40	20
P-03	40	30
P-04	40	30
P-05	40	40
P-06	40	40
P-07	40	50
P-08	40	50
P-09	40	60
P-10	40	60

<sup>a</sup> Conditions what are common for all polishing programs:

- temperature of the pad: 20°C;
- slurry components: Semi Spere : DI = 1 : 2;
- back pressure on the wafer: 0.20 bar;
- buffer polishing pressure: 0.20 bar;
- buffer polishing time: 10 s;
- working polishing pressure: 0.45 bar;
- working polishing time: 30 s.

### B. Laser crystallization

Because of a low substrate temperature during deposition, the quality of the silicon films (polycrystalline or amorphous) would probably be not sufficient for the fabrication of high-quality thin-film-transistors (TFT). Therefore, further thermal treatment has to be employed to improve the film quality [6]. Due to the very limited thermal budget, only the local laser annealing can be used. It is reported that an advanced lateral-laser crystallization technique can provide high-quality structured poly-Si film [7, 8].

The experiments with excimer laser (308 nm), UV solid state laser (355 nm) and green solid state laser (532 nm) are planned. Furthermore, the crystallization process will be enhanced by using the pre-formed seeds in the  $\alpha$ -Si layers.

### C. Chemical mechanical polishing

For the realization of 3-D structures, the important step in the process flow is the surface planarization using chemical

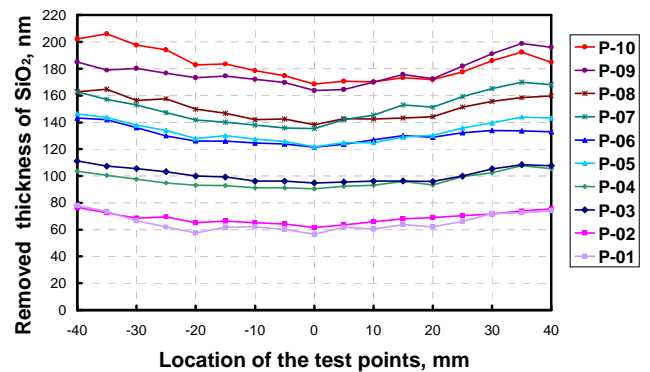


Fig. 3. Cross-section of  $\text{SiO}_2$  layer, removed using different polishing programs (see Tab. 1).

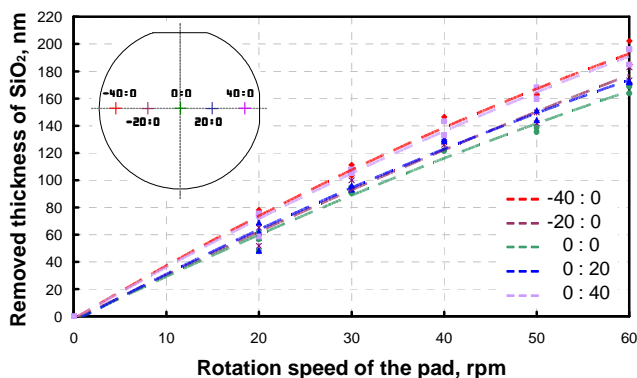


Fig. 4. Removed thickness of SiO<sub>2</sub> as a function of the pad's rotation speed.

mechanical polishing (CMP). CMP has to be applied before starting the fabrication of the next functional layer. In this work, several polishing recipes have been tested (Fig. 3 and 4) and the optimal conditions giving the best results were chosen. The morphology of the substrate with SiO<sub>2</sub> film on top of it was investigated before and after polishing (Fig. 5). The good surface uniformity was observed.

### III. CONCLUSIONS

To fulfill the limited thermal budget during the fabrication of 3-D structured integrated circuits, a new ICPECVD reactor system was realized and a low temperature deposition technique was developed.

To improve the properties of as-deposited silicon film, an excimer laser (308 nm), UV solid state laser (355 nm) and green solid state laser (532 nm) will be applied for the local thermal treatment.

The accurate CMP equipment allows for processing of several planarized layers to realize both the active and passive devices on a one chip.

### IV. ACKNOWLEDGEMENT

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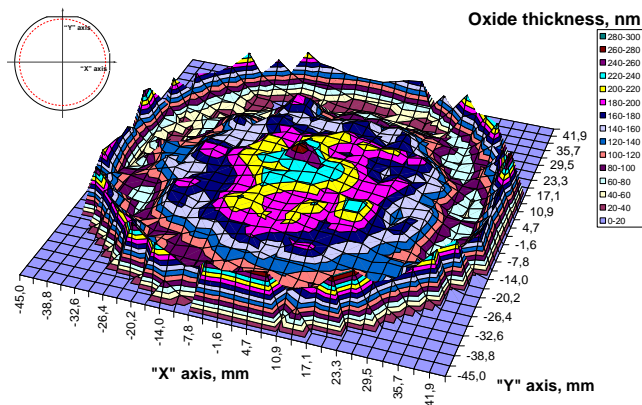


Fig. 5. Surface morphology of the wafer after polishing of 1.5 μm of silicon oxide deposited with TEOS-LPCVD.

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