Electrical Characterization of Layer-Exchange Solid-Phase Epitaxy Si Diode Junctions

Y. Civale, R. Mary-Joy, L. K. Nanver

***Abstract*—This paper describes the experimental conditions leading to fabrication of p^+-n junctions using a recently-reported selective growth of high quality crystalline Si. The controllability of the growth location and dimensions, practically unchanged when the downscale is reduced to the sub-micron range, makes possible the formation of near-ideal junctions, the electrical characteristics of which are presented in this paper. An remarkable ideality factor of about 1.05 is reliably achieved, near ideal saturation current and breakdown voltage were also obtained, demonstrating the high quality of the SPE Si growth obtained at temperature as low as 400ºC.**

***Index Terms*—Al-doping, elevated contacts, elevated source / drain, low-ohmic contacts, low-temperature processing, nanodevices, p-n-p bipolar junction transistors, selective epitaxial growth, solid-phase epitaxy, ultra-shallow junctions.**

I. Introduction

LOW-temperature Si growth techniques [1,2] have received a lot of attention recently due to their potentials for a wide range of applications, such as thin film transistors [3] and elevated source/drain fabrication for CMOS transistors [4]. Different approaches have been investigated such as excimer-laser-assisted recrystallization [5,6], selective solid-phase epitaxial regrowth [7] or, for more aggressive downscaling, semiconducting nanowires formation [8-10]. Many successful studies have been reported. However, many issues are still associated with most of the techniques such as the quality and crystallinity of the as-fabricated Si thin films, the thermal budget in relationship to transient-enhanced diffusion (TED) of already-implanted dopants, or the compatibility with existing process flows. Therefore, innovative high-quality Si formation techniques still needed.

We recently proposed a solid-phase epitaxy (SPE) fully CMOS-compatible process based on Si epitaxial deposition from physical vapor-deposited amorphous Si (α-Si) through aluminum transport layer [11]. This technique is characterized by maximum processing temperatures of 400ºC, which is a temperature range where TED effects are avoided [12]. The technique has been successfully applied for the formation of SPE Si-based nanoscale devices [13].

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In this paper, we present a series of fully characterized p-n diodes, the p^+ regions of which were formed by aluminum-doped SPE Si grown at 400ºC. In particular, temperature-dependent current-voltage and breakdown voltage measurements were performed. The results show a near-ideal electrical behavior, indicating a high-quality crystalline SPE-Si material for a wide range of junction areas.

II. Experiments

A. SPE Si Island Formation

The sequence of the SPE growth of Si islands in contact windows through silicon dioxide (SiO_2) to Si substrate is illustrated in Fig. 1.

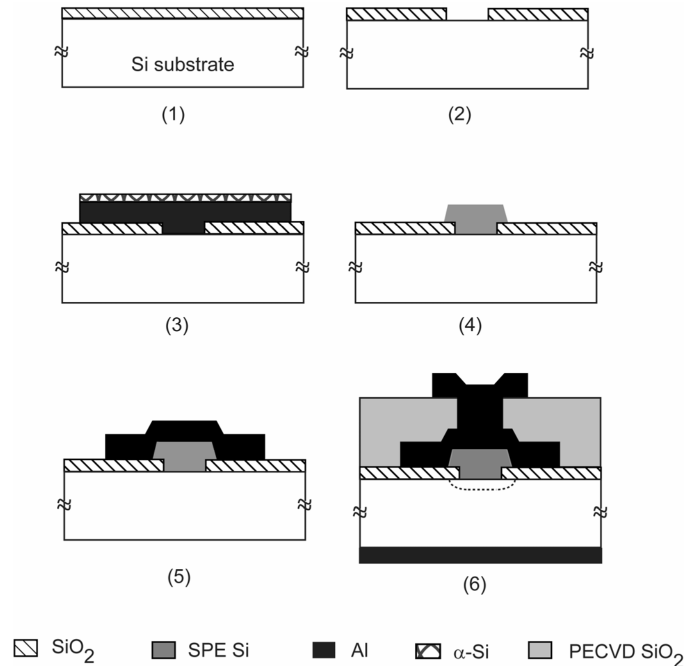

Fig. 1. The solid-phase epitaxy sequence. (1) Thermal oxidation (2) Contact window definition through SiO_2. (3) Al/α-Si PVD deposition and patterning. (4) Crystal growth (5) Coverage of SPE-Si island with Al. (6) Contacting of the SPE-Si based through-wafer diode. The dashed line represents the edges of the depletion region in the lightly n-doped substrate.

A 30-nm-thick layer of SiO_2 was first thermally grown on a mono-crystalline <100> Si substrate. In the case of sub-500-nm-wide contact windows diodes, a silicon nitride (SiN_x) spacer technology [14], mature in our research laboratory, has

been used: a 300-nm-thick low-pressure chemical-vapor-deposited silicon dioxide (LPCVD SiO_2) was formed and contact windows were patterned using conventional optical lithography. Anisotropic plasma etching through the LPCVD SiO_2 to the thermal silicon dioxide was used to obtain contact windows of about 0.7 – 0.8 µm wide. The size of the contact windows was then reduced by using silicon nitride (SiN_x) spacers as follows: a 400-nm-thick layer of low-stress low-pressure chemical vapor deposited (LPCVD) SiN_x was deposited at 850ºC and anisotropically plasma etched with C_2F_6 to leave spacers of about 300 nm wide. This reduced the width of the contact window mask to the region of 200 nm. The SiN_x spacers served as a hard mask to selectively plasma etch the remaining thermal oxide with a mixture of C_2F_6 / CHF_3 and applying a soft landing on the Si substrate. Once the contact windows opened, the native SiO_2 mainly induced by the cleaning and etching steps, was removed by dip-etching in HF 0.55% for 4 min before the transfer to the metallization module. A thin layer of aluminum was then deposited from an Al target containing 1% Si by physical vapor deposition (PVD) at room temperature. Optionally, a thin amorphous silicon (α-Si) layer was then deposited in the same PVD system. Annealing was performed at 400ºC, which is far below the 577ºC eutectic point of the Al/Si alloy. It is a well-known phenomenon in IC fabrication that the Si in the Al precipitates on the underlying substrate during annealing, with a preference for epitaxial deposition on the c-Si rather than poly-crystallite deposition on the surrounding oxide. For sub-200 nm wide contact windows, enough Si precipitates from a 0.6-µm-thick Al (containing 1% Si) layer to fill the window. For larger contact windows, our experiments showed that extra Si for filling the windows could be supplied from the sputtered α-Si that, upon annealing, diffuses into the Al. The resulting SPE island is indicated in Fig. 2, where the Al also has been removed.

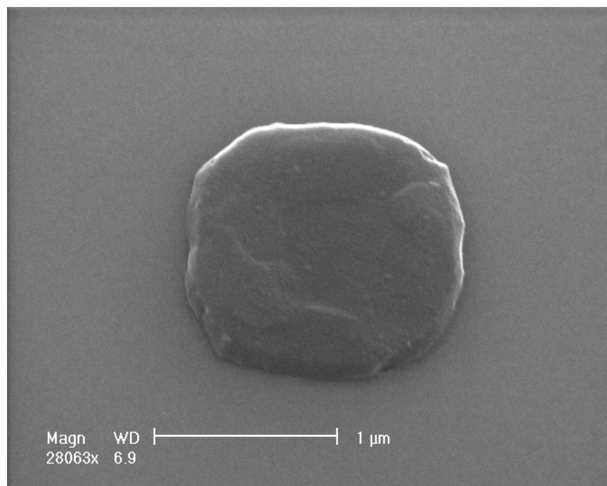

Fig. 2. SEM micrograph of an SPE filled 1.2×1.2 µm^2 contact window. The thickness of the SPE-Si island is 100 nm.

B. SPE-Si p^+-n diode

The p^+-n SPE-Si-based diodes were formed through-wafer using the grounded Si wafer backside. The electrical characterization of the diodes was done using Agilent 4156C Precision Semiconductor parameter analyzer and Cascade probe station with a hot chuck to investigate temperature dependent measurements.

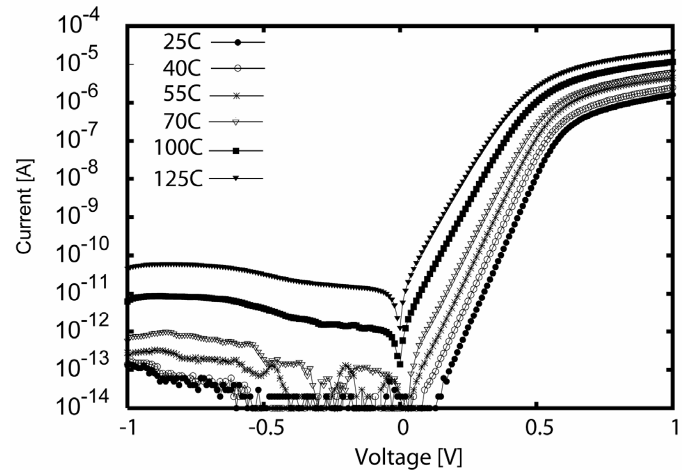

Fig. 3. Current-voltage characteristics for 1×1 µm^2 diode, as the measurement temperature is varied between 25ºC and 125ºC. The slope of the ideal region remains practically unchanged for a large range of temperature.

The reproducibility of the obtained measurements was very good for a large range of junction area, however, for clarity, the results presented below are representative of all the measurements performed on p^+-n devices with junction areas of 1×1 µm^2 and 200×200 nm^2. In Fig. 3 are presented the temperature dependence current-voltage (I-V) characteristics in the case of 1×1 µm^2-wide SPE Si diode. The measured diodes show a low leakage current indicating a low-defect density Si substrate / SPE Si island growth interface.

The I-V characteristics for the 200×200 nm^2 junction area diodes are shown in Fig 4.

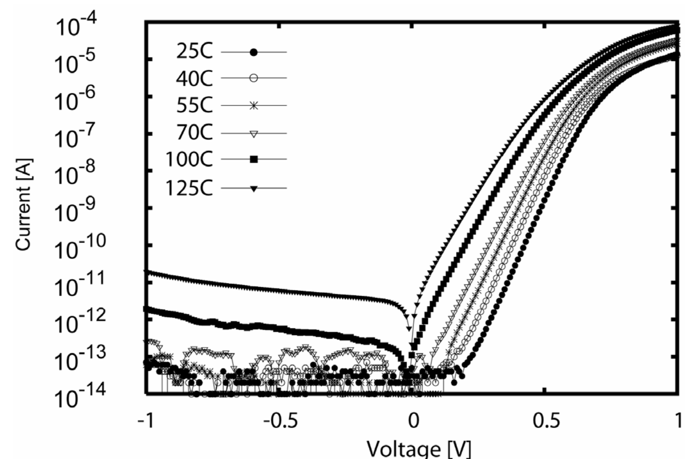

Fig. 4. Current-voltage characteristics for 200×200 nm^2 diode, as the measurement temperature is varied between 25ºC and 125ºC.

It can be clearly seen that the behavior of the diode is not affected by the downscaling of the p^+-n junction area. The ideality factor n, for both junction areas, was then calculated from the slope of the forward-bias I-V characteristics in the linear region and is presented in Figure 5. A remarkable value of 1.05 for the p^+-n diodes has been reliably measured for both 1×1 μm^2 and 200×200 nm^2 wide junction. Temperature-dependent I-V diode measurements also indicate a practically ideal saturation current as function of junction area, with a current ratio of about 5 which is in good agreement with previously reported results on the dominance of perimeter dependence current on the area dependent current for p^+-n diode of similar size [15].

The SPE Si islands are doped with Al at level higher than the solid-solubility reported in the literature corresponding to the growth temperature, i.e., 2×10^{18} cm^{-3} at 400°C [16]. For planar diodes, the breakdown voltage is theoretically mainly dependent of the doping of the lightly n-Si region, in our case 2×10^{15} cm^{-3}. Figure 6 shows the reverse bias characteristics of p^+-n diodes with junction area of 1×1 μm^2. The breakdown voltage at 25ºC was measured to be approximately 70 V which is in good agreement with the expected theoretical value.

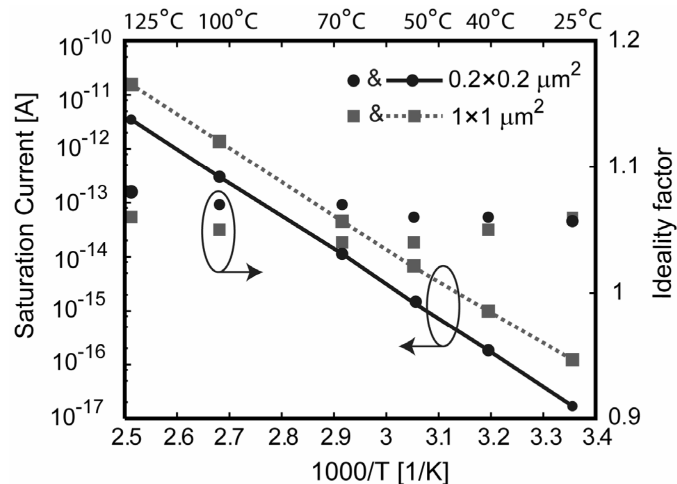

Fig. 5. Measured saturation current for two diode areas versus temperature. The saturation current of the 1×1 μm^2 diode is about 5 times higher than that of the 200×200 nm^2 diode because the junction perimeter current dominates over the area dependent current. A noteworthy low ideality factor of about 1.05 is obtained over the whole temperature range.

III. Conclusion

In this study, we reported high-quality p^+-n diodes characteristics obtained by a low temperature aluminum-induced SPE growth mechanism. Diodes having a junction area of 1×1 μm^2 and 200×200 nm^2 were fully-characterized and showed a near-ideal electrical behavior. Particularly, it was demonstrated that the downsizing of the junction area does not affect the junction behavior and the ideality factor remains remarkably low. Comparison of the saturation current shows near-ideal electrical behavior, the 1×1 μm^2 wide p^+-n junction has 5 times higher value than 200×200 nm^2, which is in good agreement with the electrical behavior of small p^+-n junction, in which the forward current is mainly driven by the perimeter current. The breakdown voltage of 1×1 μm^2 at 25ºC was found to be about 70 V, which is also in agreement with theoretical value expected from p^+-n diodes with such a doping profile.

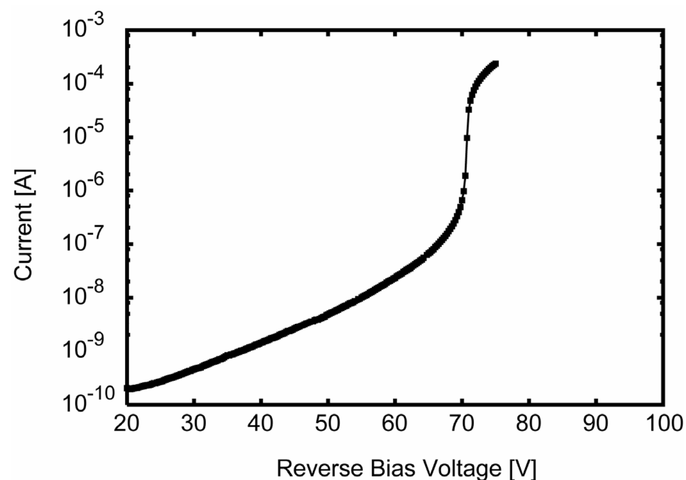

Fig. 6. The measured reverse-bias diode characteristics for 1×1 μm^2 SPE Si device. A breakdown voltage of about 70 V was measured at temperature of 25ºC.

Acknowledgment

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