A SiGe Distributed Limiting Amplifier for 40Gb/s Modulator Driver Design

Michael T. Reiha and John R. Long

Abstract—**In this paper, a SiGe differential distributed limiting amplifier is designed for 40Gb/s applications. Design issues associated with EAM drivers include concurrently achieving at least 3Vpp voltage swing and bandwidth sufficient for 40Gb/s while minimizing DC power dissipation. The output bit-error performance requires operating rise and fall times less than 20psec as well as a minimized group delay (< 10% variation). Input and output return losses are better than 10dB while the power dissipation is less than 0.5W. The limiting mode of the amplifier allows for consistent performance in mass production without trimming as well as an improvement in eye-opening for the given bandwidth.**

Index Terms—**Distributed Amplification, EAM Driver, Limiting Amplification**

I. INTRODUCTION

FORESEEABLE consumer demand for broadband services such as 4G will flood backend optical networks with an increase in data traffic flow. These networks will be forced to operate at higher speeds in order to support the higher demands in multimedia tributaries such as 4G handsets. Optical backbone networks will likely require more electro-optical interface equipment at a lesser cost, while 40Gb/s optical systems like SONET OC-768 offer increased transfer rates. Cost-effective Si-based technologies should be further utilised in the realisation of high yield, highly reliable OC-768 chipsets. This poses a formidable design task for any technology, as fibre system capacity is incremented by a factor of four every 3-5 years generation (current systems operate at 10Gb/s while the fibre capacity is in the THz range).

An electro absorption modulator (EAM) is a circuit that modulates optical signals for long-haul fibre transport. The optical electric-field intensity produced by the modulator is proportional to the output voltage swing provided by the modulator driver. Such drivers were traditionally deployed using transistors made by expensive III-V technologies that boast higher breakdown voltages (i.e. GaAs pHEMT, InP HBT) and therefore could deliver the required 5-6Vpp swings. High-speed Si-based transistors such as SiGe HBTs produce lower output voltage swings due to lower breakdown voltages. These lower breakdown voltages are both a result of device mechanisms intrinsic to Si-based technologies as well as device scaling for the realisation of a high transit-frequency (f_T) transistor [1]. And unlike GaAs technologies, SiGe HBT transistors operate at higher current densities at peak gain-bandwidth biasing conditions; thus leaving IC designers with cautionary design guidelines for both self-heating hysterisis and yield reliability [2]. In spite of these shortcomings, current SiGe HBTs possess gain-bandwidth products in excess of 200GHz, and are a strong candidate for 40Gb/s amplifier design.

II. BROADBAND AMPLIFICATION

A. Gain and Bandwidth Considerations

In amplifying devices, gain and bandwidth cannot be simultaneously increased beyond a certain limit. An amplifying device with a band-pass filter as its load is shown in Figure 1 for purposes of example.

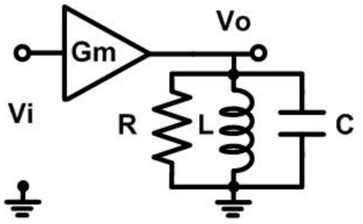

Fig. 1. Band-pass Filter Loaded Amplifier.

The maximum mid-band voltage gain (gmR) is increased with a larger load resistance (R), however the gain-bandwidth product (gm/C) is unaffected because of an equivalent reduction in the bandwidth. Bode concluded that the weighted average of an impedance function (such as the RLC shown in Fig.1.) of a given frequency range is less than or equal to that of its high-frequency asymptotic capacitance evaluated at mid-band [3]. Moreover, the gain-bandwidth product of an amplifier is limited by the parasitic capacitance and hence, any extension in bandwidth for a particular gain would have to result from a reduction in capacitance. This poses in bottleneck to circuit designers as the magnitude of capacitance of an amplifying device (i.e. SiGe HBT) is proportional to its transconductance. Any reduction in capacitance would need to be done external to the device.

B. Distributed Amplification

Cascading amplifying stages will increase the overall gain (and gain-bandwidth product when approximated to a first-order) at the expense of a reduced overall bandwidth. To achieve the highest possible gain given a bandwidth, an output impedance network with a constant magnitude is desirable. Such a network can be realized through the use of transmission lines. Intrinsically, the transmission line may be modeled as a distributed network of capacitances separated by inductances. The physical separation of capacitances by inductance allows for the separation (in time) of the charging of capacitances. This action reduces the rise time of the total transmission line capacitance, which in turn extends the bandwidth of the network.

A distributed amplifier (DA) is constructed with multiple amplifying devices embedded within a pair of transmission lines, as illustrated in Figure 2.

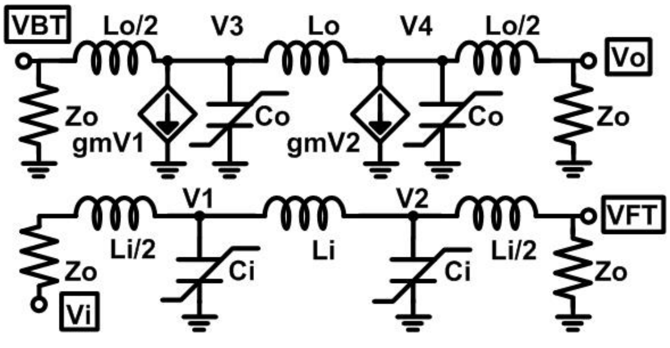

Fig. 2. Simplified Distributed Amplifier.

A signal is injected into the input line via node Vi and terminated at node VFT given that line impedance is matched to Zo. In a similar fashion, the controlled current sources inject current into the output line. The injected current travels forward toward the terminated node Vo. The output line load and termination impedance are matched to Zo. In addition, the phase (or time) delay between node voltages V1,V2 must equal the delay between node voltages V3,V4 in order to avoid output wave distortion at node Vo [3].

III. DISTRIBUTED LIMITING AMPLIFIER DESIGN

A. Limiting vs. Linear

A limiting amplifier can be viewed as a switching-mode amplifier in the sense that the transistor(s) operate while toggling between on (forward-active region) and off (cut-off region) states. In contrast to the linear amplifier (which operates in an acute region surrounding the DC bias point), the output amplitude of a limiting amplifier is insensitive to small-signal perturbations and input amplitude parameters such as ringing, under/over shoot [4]. Minimizing output waveform irregularities due to input amplitude parameters result in a cleaner eye diagram. In addition, the group delay and gain flatness are inherently easier to control than in a linear amplifier.

B. Limiting Gain Cell

The limiting gain cell used in the DA is presented in Fig. 3. The cell is comprised of two emitter followers (Q1,Q2) which are biased by ideal DC current sources and are followed by a differential switching pair. The emitter follower(s) are used to buffer the input capacitance of the differential switching pair while driving the switching pair from a low impedance source.

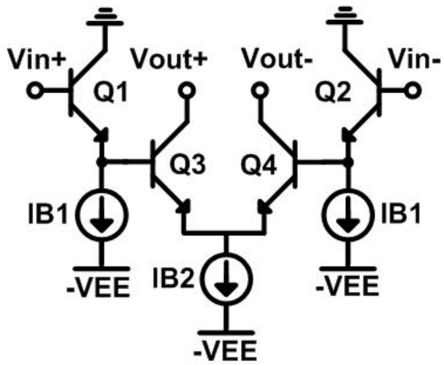

Fig. 3. Distributed Amplifier Gain Cell.

Buffering the input capacitance allows the designer more latitude in synthesizing transmission lines with a larger Bragg cut-off frequency as presented in (1), allowing a faster-switching input pulse to be injected into the DA.

$$\omega_C = 2/\sqrt{LC} \tag{1}$$

Moreover, each device was biased for maximum f_T. The current ratio between the emitter follower and the switching pair was chosen to account for both a high noise margin and minimal power dissipation [5].

C. Limiting Distributed Architecture

The proposed limiting DA architecture (scaled to 2 stages) used in the design is shown in Fig. 4.

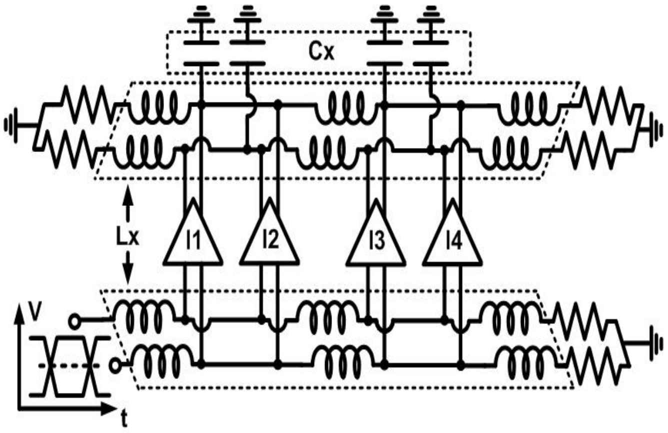

Fig. 4. Proposed Circuit Architecture Scaled to 2 Stages.

I1-I4 denote the limiting gain cells. There are two gain cells per each section to increase the effective transconductance per section while reducing the number of sections. A reduction in transmission line sections minimizes line attenuation due to line resistances and phase delay mismatch between the input and output transmission lines. The practice of lumping multiple gain cells between transmission line sections is restricted by the input capacitance loading the transmission line; which adversely decreases the Bragg cut-off frequency of the transmission line. In this circuit, the Bragg cut-off frequency was calculated to be approximately 200GHz (the fifth harmonic of a 40Gb/s signal). Additional capacitances, Cx, are loaded on the output transmission line in order to equalize the traveling wave velocities between the input and output lines. As previously mentioned, this technique minimizes the phase distortion of the output waveform.

IV. SIMULATION RESULTS

A. DC Characteristics

Distributed amplifiers nominally dissipate a lot of power (in the order of hundreds of mWs). The total power dissipation of the presented amplifier is 446mW from –3.3V, distributed over 14 sections, each section comprising of 2 gain cells. Excluding the power dissipated by the emitter buffers, the amount of power required is dictated by the desired output voltage swing in a 50Ohm environment. A 3Vpp swing demands roughly 60mA or 198mW.

An EAM driver normally produces 3-5Vpp output swing. However, SiGe HBTs inherently posses lower collector-emitter breakdown voltages than its GaAs or InP HBT counterparts. Thus, any significant argument for a SiGe amplifier to meet this stringent demand would require either the design of a distributed architecture using high-breakdown (slower-speed) devices or novel circuit techniques which utilize high-speed devices but are also immune to breakdown mechanisms.

B. Frequency Behaviour

Results that are of interest in distributed limiting amplifiers include the input and output return losses associated with the input and output transmission lines as well as the output eye-diagram and the group delay. Figure 5 illustrates the input and output return losses for the amplifier.

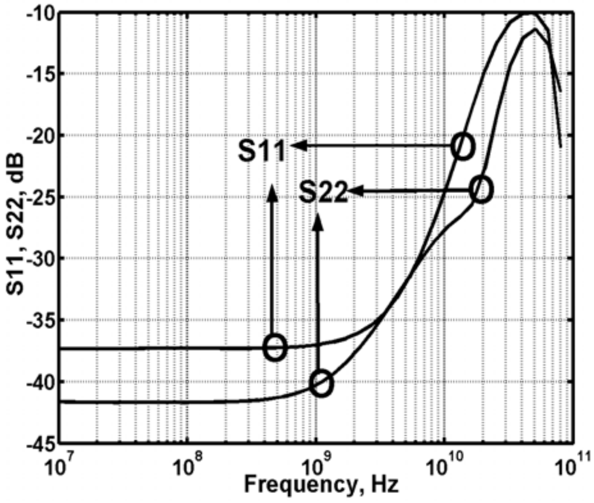

Fig. 5. Input, Output Return Loss vs. Frequency.

Both the input and output return losses (S11, S22 respectively) exhibit less than 10dB return loss while peaking at approximately 40GHz. The peaking is due to an increase of line capacitance at this frequency due to phase inversion of the gain cell input impedance as seen looking into the emitter follower(s).

The group delay of the amplifier is an important figure of merit considering it conveys the deviation of traveling time of a signal from the input to the output. A large deviation would suggest pulse-spreading or dispersion which is undesirable when designing high-speed circuits. Figure 6 illustrates the group delay of the amplifier.

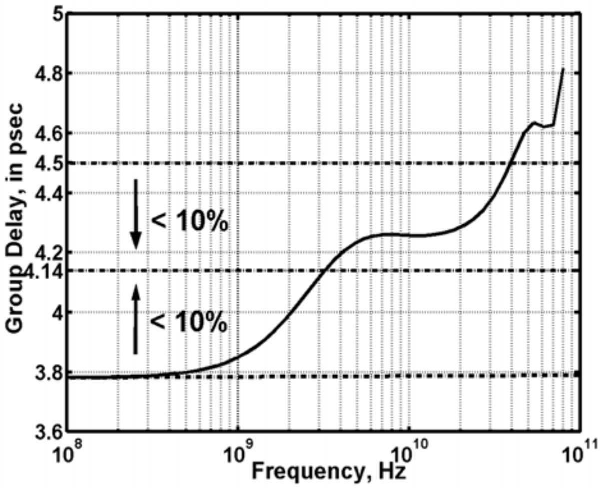

Fig. 6. Distributed Amplifier Group Delay.

Referring to Fig. 6, the injected input signal undergoes group delay restricted to +/- 10% deviation from the mean group delay (as measured between 100MHz and 40GHz).

C. Transient Behaviour

The transient behaviour of a limiting amplifier can be characterised by its output waveform with emphasis on rise and fall times as well as its output peak-peak swing. Figure 7 illustrates the transient output bit waveform.

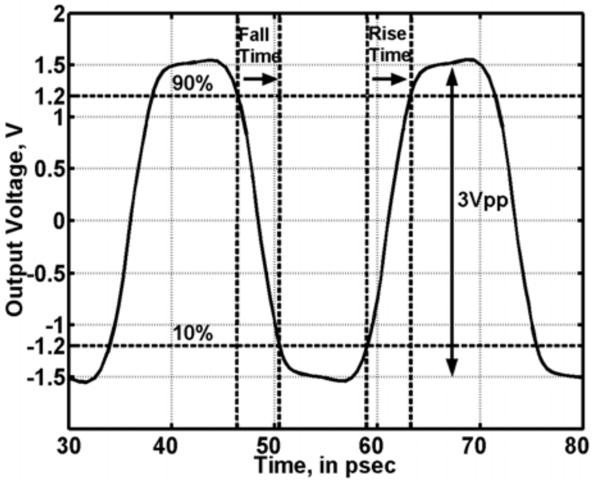

Fig. 7. Output Voltage Waveform.

The rise and fall times are approximately 4.3psec and 4.1psec respectively while the peak-peak output voltage is approximately 3V. The simulation output begins at one cycle (25psec) after the initial start-up to allow for any transient settling. The mechanisms of rise, fall time are mainly attributed to the differential-switching pair and notably the collector-base junction capacitances in tandem with the base resistance, as well as the base-emitter diffusion capacitance in pairing with the transconductance. It is noted that the rise, fall times can be improved by sizing a smaller differential-switching pair. However, this technique would come at the expense of implementing more stages in order to achieve the required output swing, thereby, increasing the circuit area and possibly magnifying any mismatch effects between the input and output traveling waves.

An alternative evaluation of the transient performance for the amplifier can be viewed through the eye-diagram. The eye-diagram of Fig. 8 serves as a measure of the transient performance given a random bit sequence at 40Gb/s.

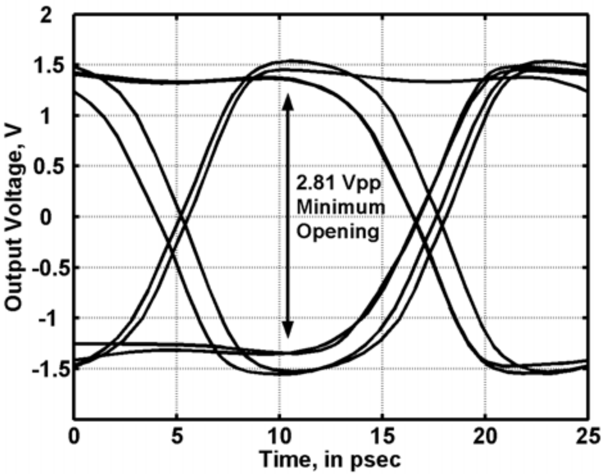

Fig. 8. Output Eye Diagram for Equivalent Bit-Rate of 40Gb/s.

The minimum eye-opening is approximately 2.81Vpp. This constitutes a 6.3% reduction from the 3Vpp depicted in Fig. 7. In addition, overshoot as well as undershoot are negligible, consistent with Fig. 7. To improve the eye-opening, the gain cell should be optimised for faster settling time (minimized output ringing) as well as providing a larger output swing allowing for fewer need stages, shorter transmission lines and shorter input-output time delay.

CONCLUSIONS

A SiGe distributed limiting amplifier was presented as a potential EAM driver circuit for 40Gb/s applications. The amplifier exhibits fast rise and fall times and a coherent eye-opening. An output voltage swing of 3Vpp was demonstrated while dissipating 445mW from a –3.3 V supply. For future integratration, a SiGe EAM driver will have to overcome the limitations of its low junction-breakdown voltages comparable to other III-V HBT's. The amplifier gain cells would need to produce larger output swings with improved transient sequences (faster settling time, faster propagation delay time) for an improvement to the eye-diagram output.

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